Comparing designs and metrics of ten different ALU architectures from 1999 to 2015

Maureen Flintz
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816-2362

Abstract—The object of this paper is to analyze some of the fundamental metrics for selected ALU designs, covering both time and space complexity. Power and energy dissipation, logic operations and shifting operation using FSL and static CMOS logics at 90nm CMOS process. This ALU combines adder, shifter and logical units which are having low power consumption, less delay and uses lesser area.

Keywords—ALU, Clock rate, Memory Capacity, Power dissipation, Energy consumption, Execution time, ALU, Low Energy and Power, Computer Architecture.

I. INTRODUCTION

The ALU is a combinational logic device. It can perform both bitwise and mathematical operations on binary numbers and is the last component to perform calculations in the processor. The ALU uses operands and code that tells it which operations to perform for input data. After the ALU processes the information it is sent to the computer’s memory.

In general, a combinational logic circuit has inputs, which are divided into data inputs and control inputs, and outputs. Control inputs tell the circuit what to do with the data inputs. The control bits tell the ALU which operation to perform on the data inputs. The output of the ALU then heads back to the register file.

Data and instructions are transferred using the data bus. A 64-bit data bus can carry twice as much data as a 32-bit data bus. The more width a data bus has the more data that can be transferred improving system performance. (ITRS) International technology roadmap for semiconductors is the guide to the decrease in node size over the years it is estimated that in 2022 ITRS technology will continue to 5nm. Execution time also known as CPU time or Processor execution time is the sum of time which the processor itself was active during completion of a task so the execution time is equal to the response time minus the CPU idle time. Power dissipation is the watts dissipated at any instant during the workload and it determines the cooling needs of the CPU, and the energy consumption of processors is the joules needed to complete a workload and corresponds to battery life.

In Section 2 there are ten ALU designs spanning from the year 1999 until today that are reviewed. Then in section 3 the data analysis is provided. Followed by section 4 that contains the conclusions of the paper.

II. LITERATURE REVIEW

A. Architectures from the 1999

In 1999 Pandey, B. et al., wrote about the design of a new low power 16-bit ALU that had been designed and implemented with 0.6μm single-poly triple-metal CMOS process. This ALU provides a low power architecture. For low power consumption, we propose a new ALU architecture which has an efficient propagation(P) and a generation(G) block schemes of ELM adder. [9]

B. Architectures from 2003

In 2003 J. Di et al., found a novel method to design high throughput power-aware FIR filter is proposed Based on pipelining multipliers and adders, very high throughput can be achieved. To lower power dissipation and reduce latency, 2-Dimensional pipeline gating technique is applied to improve the power awareness of the designed FIR filter[4].

C. Architectures from 2005

In 2005 Chatterjee, B. et al., found the design of a 32-b arithmetic and log unit (ALU) that allows low-power operation while supporting a design-for-test (DFT) scheme for delay-fault testability. The low-power techniques allow for 18% reduction in ALU total energy for 180-nm bulk CMOS technology with minimal performance degradation [8].

D. Architectures from 2006

J. Huang et al proposed field programmable gate array-based scalable architecture for discrete cosine transform (DCT) computation using dynamic partial reconfiguration. Our architecture can achieve quality scalability using dynamic partial reconfiguration. This is important for some critical applications that need continuous hardware servicing. [5].

E. Architectures from 2009

In 2009 Ramalatha, M et al., noticed the ever increasing demand in enhancing the ability of processors to handle the complex and challenging processes has resulted in the integration of a number of processor cores into one chip. Still the load on the processor is not less in generic system. This load is reduced by supplementing the main processor with Co-Processors, which are designed to work upon specific type of functions like numeric computation, Signal Processing, Graphics etc[6].

Also in 2009 Prakash, P et al., noticed that low power and high speed requirement is a challenging task in design of ALUs. Supply
voltage scaling is promising approach because it reduces switching activities and active power but it degrades the performance and robustness. Recently a new dynamic like static circuit family called Feedback-Switch Logic (FSL) has been proposed. FSL is suitable for high speed and low power because it offers fast switching, reduced capacitance and input-switching dependent activity factor without the need of clock connection. This paper presents design of low power high speed 32-bit ALU based on static CMOS and FSL logics at 90nm CMOS process in CADENCE design tool[10].

F. Architectures from 2013

In, 2013 Pandey, B et al., showed power is directly proportional to frequency. With increase in frequency, there is increase in power consumption irrespective of IO standard. LVCMOS is the only IO standard, which takes less power when we upgrade our design to latest FPGA[7].

G. Architectures from 2014

Energy efficiency and algorithmic robustness typically are conflicting circuit characteristics, yet with CMOS technology scaling towards 10-nm feature size, both become critical design metrics simultaneously for modern logic circuits. This paper propose a novel computing scheme hinged on probabilistic domain transformation aiming for both low power operation and fault resilience[3].

H. Architectures from 2015

Quantum-dot cellular automata (QCA) has been studied extensively as a promising switching technology at nanoscale level. Despite several potential advantages of QCA-based designs over conventional CMOS logic, some deposition defects are probable to occur in QCA-based systems which have necessitated fault-tolerant structures. The functionality and correctness of our design is confirmed using high-level synthesis, which is followed by delineating its normal and faulty behavior using a Probabilistic Transfer Matrix (PTM) method. The related waveforms which verify the robustness of the proposed designs are discussed via generation using the QCADesigner simulation tool[2].

Also in 2015 S. Salehi et al., wrote about the continuous increase in transistor density based on Moore’s Law has led us to Complementary Metal-Oxide Semiconductor (CMOS) technologies beyond 45nm process node. These highly-scaled process technologies offer improved density as well as a reduction in nominal supply voltage. New challenges also arise, such as relative proportion of leakage power in standby mode. In this paper, we present an analysis regarding different aspects of 45nm and 15nm technologies, such as power consumption and cell area to compare these two technologies [1].

III. DATA ANALYSIS

Metrics covered in this paper are:

- Data bus width (bits) vs. Year
- ITRS technology node (nm) vs. Year
- Clock Rate (GHz) vs. Year
- Power or Energy vs. Year
IV. CONCLUSION

Scaling trends such as Moore’s law and ITRS can be seen in the data analysis. A couple different designs such as the carry select adder, ripple carry adder and the add-and-right shift multiplier can be seen in some of these designs.

REFERENCES


**TABLE I.**<br>WRITE A CAPTION IN YOUR OWN WORDS ABOVE EACH TABLE.

<table>
<thead>
<tr>
<th>ALU or Floating Point Architecture Name</th>
<th>Datapath width (bits) or #bits in operands</th>
<th>Time for Operation or Design Type</th>
<th>ITRS Technology Node (nm) or Area or Model of Chip used</th>
<th>Energy/Power Consumption (W or J) else indicate “low” or “high”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy and Area Analysis of a Floating-Point Unit [1]</td>
<td>32 bits (Operands)</td>
<td>N/A</td>
<td>IEEE-754 Single Precision</td>
<td>45nm and 15nm (ITRS Node)</td>
</tr>
<tr>
<td>Ultra-area-efficient fault-tolerant QCA full adder [2]</td>
<td>1 bit (Operands)</td>
<td>Ultra-area-efficient fault-tolerant QCA full adder</td>
<td>N/A</td>
<td>18nm^2 (Cell Area)</td>
</tr>
<tr>
<td>High Throughput Power-aware FIR Filter Design [4]</td>
<td>16 bits (Operands)</td>
<td>FIR Filter</td>
<td>FIR Filter</td>
<td>N/A</td>
</tr>
<tr>
<td>Scalable FPGA-based Architecture for DCT Computation[5]</td>
<td>32 bit (Operands)</td>
<td>N/A</td>
<td>DSP48</td>
<td>N/A</td>
</tr>
<tr>
<td>High speed energy efficient ALU design [6]</td>
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<td>Vedic</td>
<td>Vedic</td>
<td>N/A</td>
</tr>
<tr>
<td>Design of a 1.7-GHz low-power delay-fault-testable 32-b ALU in 180-nm CMOS technology [8]</td>
<td>32 bit (Operands)</td>
<td>CDL</td>
<td>CDL</td>
<td>N/A</td>
</tr>
<tr>
<td>Energy efficient design and implementation of ALU on 40nm FPGA [7]</td>
<td>8 bit (Operands)</td>
<td>ALU design</td>
<td>ALU design</td>
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</tr>
<tr>
<td>Multi-level approaches to low power 16-bit ALU design [9]</td>
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<td>ELM adder</td>
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<td>N/A</td>
</tr>
<tr>
<td>Design of Low Power High Speed ALU Using Feedback Switch Logic [10]</td>
<td>32 bit (Operands)</td>
<td>FSL</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
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