Moore’s Law: The Progression of the ALU and the ITRS Technology Node

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Abstract—The objective of the paper is to evaluate some of the fundamental metrics for various ALU designs, focusing on both time and space complexity. The primary metrics examined include data bus width, time for operation, design time, ITRS technology node size, chip area, model of chip used, energy and power consumption. Using these metrics, the progression of the ALU has been assessed, as well as the trends of the various metrics during 5 year time intervals. This can be seen in the different designs, especially the specifications of the 2-dimensional pipeline gating and its application to FIR Design, the fast ALU design in CMOS for low voltage operation and the fine-grained pipeline multipliers and adders.

Keywords—Clock rate, Memory Capacity, ALU, Floating Point Unit, Data bus width, Execution time, Power dissipation, Energy consumption

I. INTRODUCTION

An Arithmetic Logic Unit (ALU) is a block in the central processing unit (CPU) used for performing arithmetic and logic operations such as addition, multiplication or Boolean instructions. The majority of operations performed by the CPU are executed by ALUs. The ALU receives input along electronic paths referred to as busses. This input is generally an instruction word which provides the ALU with an operation code, one or more operands, function, and other information if needed. Based on the operation code and function, the ALU will perform one operation or another using the given operands. As a result, the function field is a part of the control path as it controls what operation is being performed while the data path consists of the input operands received from the register file and output operands sent to the register file.

The data bus width specifies how much data can be transmitted at one time. The wider the bus, the more data that can be transmitted over the channel. With a 32-bit bus for instance, that means that 32 bits can be transferred at once. International Technology Roadmap for Semiconductors (ITRS) provides an assessment which explores the future of the semiconductor industry. In this future, it is expected that the size of process technology nodes will continue to decrease, reaching 5μm in 2022. Execution time provides insight as to how long a processor takes to perform a certain task or program. Power dissipation is power that is lost or wasted. In reference to processors, this may consist of forms like heat that serve no other use in the system. Power consumption however is power that is used that actually contributes to the function of the system, in this case, the processor.

The following sections provide an in-depth analysis of various ALU designs, focusing on the topics previously discussed. In section two, there are ten ALU designs ranging from the year 2000 until today that are reviewed. Section three provides a visual display of the trends found during these times through the use of charts and graphs. Section three offers a conclusion of the findings in the study, followed by an acknowledgement of used references.

II. LITERATURE REVIEW

During the period of 1999 to 2004, only two designs were analyzed therefore it was not enough to discover any consistencies between them. In fact, almost all aspects of the designs within the period were different, outside of both ALU’s operating on lower power consumption. In 2002, a fast ALU design in CMOS for low voltage operation was analyzed. Results showed that the 4-bit ALU operated with low power consumption using a Ripple Carry Adder [7]. In 2003, fine-grain multipliers and adders were used, this time with a 16-bit ALU instead [4]. Compared to the first design, the node size was dramatically smaller, specifically 500% smaller, going from 1200 nm to 240 nm.

Continuing the trend of decreased node size, the designs within the period of 2005 to 2010 saw ITRS Technology node sizes that were all smaller than those of the previous period. In 2005, a 64-bit integer execution ALU with dual supply voltages was examined [8]. The design featured a 90 nm ITRS node, as well as the only sparse tree semi-dynamic adder found in the study. During the same year, a 32-bit ALU was studied which featured a 180 nm ITRS node and had a low power consumption [9]. The following year, 2006, a design featuring pipelined array multipliers using 2-dimensional pipeline gating was examined [5]. The design using a 16-bit ALU operated on a chip size of very little area and results showed that the 2-D multipliers had 54.4% less power dissipation than 1-D pipelined gate. In 2009, an ALU using Feedback Switch Logic was analyzed [10]. The 32-bit ALU once again featured a 90 nm ITRS node consuming only 0.6 mW in its operation.

From 2011 to 2015, four different ALU designs were analyzed, with only one specifying the size of the ITRS Node. This size of only 45 nm provided more support for the
continued decrease of node size. Similarly to previous periods, no trend was found for other metrics other than the amount of bits in the operands being inconsistent in each period. In 2014, an energy-efficient multiplier-less discrete convolver design was analyzed [3]. The design operated with low power consumption as expected, consuming only 166.63 nJ on a Virtex 6 FPGA device (XC6VLX550t). In fact, this ALU featured the largest operand in the study, a whopping 128 bits. In 2015, three designs were investigated, the first being a 32-bit floating point unit design [1]. This design featured the smallest ITRS Technology Node in the study, only 45 nm, as well as consuming only 2.048 mW. Again in 2015, an ultra-area-efficient fault-tolerant QCA full adder was analyzed [2]. This design had only a 1-bit operand, the smallest in the study. The last design reviewed in 2015 was a 16-bit RISC processor using low power pipelining [6]. The 2-stage pipelined design featured a carry select adder running on a Xilinx Kintex XC7K1607-3fbg676, operating at 0.220W which was in fact the largest power consumption in the study.

III. DATA ANALYSIS

Metrics covered by various papers which are suitable for plotting:
- Data bus width (bits) vs. Year
- ITRS technology node (nm) vs. Year
- Power vs. Year

Fig. 1. Data Bus Width vs. Year

Fig. 2. ITRS technology node (nm) vs. Year
The first table offers a comparison between data bus width and year. As demonstrated by the plot, it is clear there isn’t much of a relationship between the two as there is no trend. The second table displays the relationship between ITRS Tech Node Size and the year. Unlike the previous table, a negative trend is present in this table. It is clear that the node sizes continued to decrease over the years, which supports Moore’s Law as expected. The third table was difficult to interpret as many of the values provided in the table were simply low and as a result could not be included in the plot. Therefore, it was rather difficult to decipher any trends in this plot as there were not many values to assess.

IV. CONCLUSION

After careful analysis of all of the designs, one trend is very clear, the size of the ITRS Node has continued to decrease over the years which is in fact consistent with Moore’s law. A 32-bit ALU appeared to be the most common over the different designs, which was expected, with a 16-bit appearing frequently as well. The Carry Select Adder (CSA) was the most popular design used, and also interesting was the proven effectiveness of the multi-dimensional pipelined gates, with a 2-D offering 54.4% less power dissipation than 1-D pipelined gate [5].

REFERENCES


![Power Consumption vs Year](image-url)
<table>
<thead>
<tr>
<th>ALU or Floating Point Architecture Name</th>
<th>Datapath width (bits) or #bits in operands</th>
<th>Adder</th>
<th>Multiplier</th>
<th>Floating Point</th>
<th>Technology Node (nm) or Area Model of Chip used</th>
<th>Energy/Power Consumption (W or J)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy and Area Analysis of a Floating-Point Unit [1]</td>
<td>32 bits (Operands)</td>
<td>N/A</td>
<td>N/A</td>
<td>IEEE-754 Single Precision</td>
<td>45nm and 15nm (ITRS Node)</td>
<td>2.048mW (45nm) 0.6340mW (15nm)</td>
</tr>
<tr>
<td>Ultra-area-efficient fault-tolerant QCA full adder [2]</td>
<td>1 bit (Operands)</td>
<td>Ultra-area-efficient fault-tolerant QCA full adder</td>
<td>N/A</td>
<td>N/A</td>
<td>18nm²2 (Cell Area)</td>
<td>low</td>
</tr>
<tr>
<td>Improving Power-awareness of Pipelined Array Multipliers using 2-Dimensional Pipeline Gating and its Application to FIR Design [5]</td>
<td>16 bits (Operands)</td>
<td>N/A</td>
<td>2-D pipelined multipliers</td>
<td>N/A</td>
<td>Very little area</td>
<td>54.4% less Power Dissipation than 1-D pipelined gate / low</td>
</tr>
<tr>
<td>High Throughput Power-aware FIR Filter Design based on Fine-grain Pipeline Multipliers and Adders [4]</td>
<td>16 bits (Operands)</td>
<td>N/A</td>
<td>1.25 GHz clockrate</td>
<td>N/A</td>
<td>0.24μm static CMOS</td>
<td>low</td>
</tr>
<tr>
<td>Design &amp; analysis of 16 bit RISC processor using low power pipelining [6]</td>
<td>16 bits (Operands)</td>
<td>2 stage pipeline w/Carry Select Adder</td>
<td>N/A</td>
<td>N/A</td>
<td>Xilinx Kintex XC7K1607-3fbg676 (Model of Chip used)</td>
<td>0.220W (28nm)</td>
</tr>
<tr>
<td>Fast ALU Design in CMOS for Low Voltage Operation [7]</td>
<td>4 bit ALU</td>
<td>Ripple Carry Adder</td>
<td>N/A</td>
<td>N/A</td>
<td>1.2 mm N-well CMOS technology</td>
<td>low</td>
</tr>
<tr>
<td>4-GHz 300-mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS [8]</td>
<td>64 bit ALU</td>
<td>Sparse-tree semi-dynamic adder</td>
<td>Single-rail dynamic source multiplexer</td>
<td>N/A</td>
<td>90nm dual-Vt CMOS technology</td>
<td>9.6mW</td>
</tr>
<tr>
<td>Design of a 1.7-GHz low-power delay-fault-testable 32-b ALU in 180-nm CMOS technology [9]</td>
<td>32 bit ALU</td>
<td>Ripple Carry Adder</td>
<td>N/A</td>
<td>N/A</td>
<td>180-nm CMOS technology</td>
<td>low</td>
</tr>
<tr>
<td>Design of Low Power High Speed ALU Using Feedback Switch Logic [10]</td>
<td>32 bit ALU</td>
<td>Kogge-Stone Adder</td>
<td>N/A</td>
<td>N/A</td>
<td>90nm CMOS</td>
<td>600μW</td>
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</tbody>
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