Analysis of Various High Speed Low Power Adder Compositions and Designs

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Abstract—The objective of this paper is to evaluate some of the fundamental metrics for selected Adder designs. Compositional integrity of the CMOS technologies allow for strategic benefits of programmable logic that will be discussed in this paper. Single-rail, Feedback Switch logic, Compound Domino logic, Single bit, 16 and 32 bit Adders will be compared in terms of cell area size/length and relative power consumption. Generally, we know 16 and 32 bit Adders are low power mechanisms in the ALU design. The Adders discussed are “High Performance” meaning high speed and low power. Along with Adders, power density and area will be discussed in regards to CMOS technologies, alone.

Keywords—Adder, CMOS technology, CMOS design, Low-power, High-speed, High-performance.

I. INTRODUCTION

Investigated in this paper are several Adder designs that obtain functional abilities specific to a purpose. The composition of Adders are unique, whether the Adder is specialized for fault-tolerance, energy efficiency, size management, etc, each one is different. Several Adders will be discussed, comparing and contrasting parameters and metrics alike.

ALUs (Arithmetic Logic Units) are electronic circuits used to calculate arithmetic and bitwise logical operations. Mentioned in [9] the ALU is the heart of the modern microprocessor. We consider the ALU fundamental to the central processing unit of the computer.

Data bus width and clock rate determine the amount (width) of the number of bytes that can be carried per second. On a large scale this determines processing power in terms of execution time. The ITRS technology nodes are common for the circuit connection type. These are semi-conductor devices ranging generally from 10 nm – 180nm. The design of these nodes contribute to its own power consumption.

There is a group of heavily popular ITRS technology nodes used for Adders. We see different forms and shapes of complementary metal-oxide semiconductor (CMOS) technologies used. CMOS is a battery powered memory chip in computers that stores information. There are several CMOS designs, different for particular specifications in an Adder. Adder composition and design will be discussed.

II. LITERATURE REVIEW

Since CMOS technologies are so heavily used in Adder designs, various CMOS will be discussed.

CMOS are preferred ITRS technologies offer improved density as well as a reduction in nominal supply voltage [1]. Hence, lower supply voltage yields lower power consumption via the expression $P = V^2$ (power equals current times voltage). Power consumption is also analyzed in terms of cell area. Power density and area are two important factors for CMOS technologies. As seen in [1], 15nm technology results in 3-4 fold improved energy efficiency than its 45nm technology counterpart, size does matter. As energy efficiency is a mutual concept in almost all of these papers, it is apparent that CMOS technology is extensively useful for algorithmic robustness [3] and power consumption [4]. Similar to Adder designs, FPPs and multipliers are needed to have fault-tolerance algorithms. The FaDRes design [5] utilized input signal characteristics to reduce DCT (discrete cosine transform) size. The power consumption for the FaDRes using the Virtex-4 FPGA was a total of 1541 mW; 591 mW quiescent and 950 mW dynamic.

As mentioned before, whatever the ALU design is, the main goals are energy efficiency, reduced execution time/clock cycle time and small area size. CMOS technologies in these papers work with 1 bit, 16-bit, 32-bit and 64-bit wide. The Adders investigated have several different uses. Two of which are single-rail, one compound domino logic, one feedback switch logic design. Both single-rail Adders in [6] and [7] are CMOS technology both running 64-bit datapath operands. The most significant difference between these Adders are the CMOS size, one being 90 nm and the other 180 nm bulk CMOS technology. The 180 nm contained an Adder core running at 310 ps and after margining provided up to 19% speedup. Several different size nodes were tested, however, the 180 nm provided the largest speedup factor [7]. The single rail Adder in [6] contains dual supply voltages which created a 56% reduction in switching and active leakage energy.

For the FSL (feedback switch logic) ALU another 90 nm CMOS technology was implemented. As seen before, supply voltage scaling reduces switching activities and power [7][8]. Similar to the single-rail Adders, FSL ALU logic is suitable for low power high speed. The FSL logic in [8] works with 32 bit as opposed to the 64 bit and single bit Adders. Here will be a comparison of the 32-bit FSL and the single-bit QCA (quantum-
dot cellular automata) Adders found in [8] and [2]. Both designs promise for switching minimization down to the nanoscale level. The QCA Adder single-bit attributes specialized in high-fault tolerance while maintaining dense structure using only one MG (majority gate) [2]. Fault tolerance is paramount to the system’s algorithmic robustness. Both of these Adders wager fast switching speed and reduced capacitance. The FSL achieves a 14% reduction in delayed as opposed to its static CMOS logic design counterpart [8].

The final two designs investigated here are two 32-bit ALU designs intended to minimize total energy consumption while maintaining high performance on a small chip/CMOS. A CPL-based logic ALU design and the Altera’s NIOS 2.0 soft processor are analyzed. The Altera’s NIOS is implemented on an Altera’s 20KE FPGA architecture. From the start we have the contrasting value of a model chip and a CMOS technology design as seen from previous Adders. The high performance 32-bit ALU contains a dual supply, minimizing total energy consumption [10]. The chip uses a scheme that speculates the value of the carry from the lower 16-bits to the upper 16-bits that only stalls when the ALU result prediction is incorrect [10].

III. DATA ANALYSIS

As discussed in the literature review, these Adders have several different size CMOS technology design, not including the Apex 20KE chip implementation on the FPGA. One metric stood out as very promising. The size of the CMOS has a direct relationship with the total energy consumption. For data analysis, normalized energy and several other energy characteristics were detailed in terms of technology size. Data was collected from [1] and [10]; Figures 1 and 2 display the energy usage of these technologies.

The blue column represents a 45 nm CMOS design while the orange column represents a similar 15 nm CMOS technology design. However, there are 4 sections of comparative data. The numbers below outline the category of energy consumption of these technologies.

1. Cell internal energy
2. Total Dynamic Energy
3. Net Switching Energy
4. Total Energy

As noted in [1] the 45 nm design consumes about 4 times more energy than the 15 nm design. The 15 nm design also offers about 30% less cell area.
Once again we have more quantitative data that solidifies the notion that technology node size directly correlates with Energy. In this case, we are using normalized data as provided in [10]. Figure 2 shows the normalized energy curve in response to 4 different CMOS technology sizes. The sizes used here are popular in ALU design. The trend shows why certain technology sizes would be preferred over others. In the papers studied, the high performance Adders tend to be that of 90 nm size. With the term high performance meaning low energy, the figure below supports the idea of high performance.

Fig. 2. <Technology node (nm) versus Normalized Energy>

![Technology Node vs. Normalized Energy](image)

**IV. CONCLUSION**

In conclusion, we investigated several Adders that accomplished a variety of specifications. An underlying theme was the requirement to maintain high performance. These Adders are considered “low power high speed” ALU designs. Complimentary Metal-Oxide Semiconductors (CMOS) are standard per ALU design. Of the literature I studied about 80% were of CMOS ALU design. An interesting characteristic found within the data metrics is that technology node size is directly proportionate to energy usage in all aspects; whether it be internal cell energy, net switching energy or dynamic energy.
REFERENCES


**Table I. Architectures Used and Base Metrics**

<table>
<thead>
<tr>
<th>ALU or Floating Point Architecture Name</th>
<th>Datapath width (bits) or #bits in operands</th>
<th>Time for Operation or Design Type</th>
<th>ITRS Technology Node (nm) or Area or Model of Chip used</th>
<th>Energy/Power Consumption (W or J) else indicate “low” or “high”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy and Area Analysis of a Floating-Point Unit [1]</td>
<td>32 bits (Operands)</td>
<td>N/A</td>
<td>N/A</td>
<td>IEEE-754 Single Precision</td>
</tr>
<tr>
<td>Ultra-area-efficient fault-tolerant QCA full adder [2]</td>
<td>1 bit (Operands)</td>
<td>Ultra-area-efficient fault-tolerant QCA full adder</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Energy-Efficient Multiplier-Less Discrete Convolver through Probabilistic Domain Transformation [3]</td>
<td>128 bits (Operands)</td>
<td>N/A</td>
<td>N/A</td>
<td>Virtex 6 FPGA devices (XC6VLX550t) (Model of Chip used)</td>
</tr>
<tr>
<td>Self-adapting Resource Escalation for Resilient Signal Processing Architectures</td>
<td>128 bits (Operands)</td>
<td>N/A</td>
<td>Xilinx DSP48 Multiplier</td>
<td>N/A</td>
</tr>
<tr>
<td>Fault Demotion Using Reconfigurable Slack (FaDReS) [7]</td>
<td>32 bits (Operands)</td>
<td>N/A</td>
<td>DSP-48 Multiplier</td>
<td>N/A</td>
</tr>
<tr>
<td>A 4-GHz 300-mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS [15]</td>
<td>64 bits (Operands)</td>
<td>Single-Rail Adder</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Sub-500-ps 64-b ALUs in 0.18-μm SOI/bulk CMOS: design and scaling trends [18]</td>
<td>64 bits (Operands)</td>
<td>Single-Rail Adder</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Design of Low Power High Speed ALU Using Feedback Switch Logic [24]</td>
<td>32 bits (Operands)</td>
<td>Feedback switch logic Adder</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>A high performance 32-bit ALU for programmable logic [26]</td>
<td>32 bits (Operands)</td>
<td>16 and 32 bit Adder</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>A high performance 32-bit ALU for programmable logic [27]</td>
<td>32 bits (Operands)</td>
<td>Compound Domino Logic (CDL) Adder</td>
<td>N/A</td>
<td>N/A</td>
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