ALU Design: Improvement Over Time Analysis

Richard Perdomo
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816-2362

Abstract—The way that technology has been progressing is astonishing— from less than 100 transistors in a computer a few decades ago to several million in the modern era. The following is a look at how far we’ve come in our technological endeavor with a look at a common computer system, the arithmetic logic unit (ALU) including the Floating-point unit. We will also take brief notice of the different technologies and configurations that have been studied of the ALU. Some metrics such as node size, delay speed, and power consumption will be used to convey our progress thus far.

Keywords—CMOS technology, FPGA, Full-Adder, Moore’s law

I. INTRODUCTION

Computers are one of the most important technological items in any household- and a lot of people barely understand them. Over the course of decades computers went from taking up a whole room to sitting snuggly on your lap. Such technological advancement requires persistence and research done by masters and PhD, students and teachers.

A modern computer has numerous systems governing everything from storing to memory to displaying a picture on a screen. A key system responsible for basic functioning of a computer is known as the Arithmetic Logic Unit (ALU). The ALU preforms operations such as: Addition/subtraction, Multiplication/division, Inequalities, Boolean operations and Bit shifting.

The ALU takes in numbers in binary base form from registers and outputs in binary base form to registers. The ALU knows what functions to preform and where to place them based on control inputs from the Central Processing Unit (CPU), which determine such things as logic function, shift function, and function class. The ALUs operation “path” is known as the data path, and the CPU input and outputs are the “control path”. The ALU not only informs the CPU of operation results but also if the result has overflowed or resulted in zero.

Some clarification, some terms used in this paper need definitions for an appreciation of what is going on. The data bus width is the number of wires used to carry information in a computer. In most cases the data bus width will be 32 or 64 as these are most common. The international technology roadmap for semiconductors (ITRS) technology node is a standard as set forth by the ITRS that describes the wire/transistor sizes in computer chips. A component or systems execution time is the time it takes the technology to perform its function, computer systems typically take in the order of nanoseconds for execution.

Power dissipation is the amount of energy wasted per second, usually as heat. Finally, energy consumption is how much energy a component or system requires to perform accurately.

In this paper, improvements, drawbacks, and innovations are discussed to view the progress of the technology and where its going. In section II we will go over some papers that have been reviewed and in section III we will see the results of our dive into these works.

II. LITERATURE REVIEW

Many researchers in the past have done countless experiments and studies to design more efficient ALUs. Even as we speak there are numerous studies and experiments happening all around the world trying to make computers faster and smarter. Research in ALU design is just one of the many ways of improving the modern computer going on right now, and it is the focus of the papers to be reviewed.

One of the main ways that ALUs are improved and computers in general are by making the technology smaller. Moore’s Law governs the rate at which we can make process nodes smaller. In recent years we have surpassed the 45nm process node as we quickly make headway to even smaller ALUs and CPUs [1]. Just 7 years ago node size was at 90 nm using CMOS technology [8] whereas more recently the node size has decreased 6-fold.

Other methods of improved ALU design involve power consumption [6][8].

Data Analysis

After compiling the data, trends are clear. Fig. 1 shows the decrease in technology node length over time. Since 2009 there has been a 9-fold decrease in relative technology node size.
Fig. 1. ITRS node length over time[8][5][3][1]

Fig. 2 has data that is misleading to the untrained eye. The data suggests that the overall data bus width has gone down in recent years but the truth is that data width varies with the technology. Often computer technology has a data width of 64 or 32 bits in the modern era. Less commonly is data widths of 1, 8, or 16 bits.

Fig. 2. Data bus widths of recent years[5][8][3][1]

Today it is common knowledge in the industry to know that power consumption and clock frequency are inversely related. The data from Fig. 3 and Fig. 4 affirm this knowledge. The data shows that as the execution speed of the technology decreases exponentially the power consumption increases exponentially. This is due to the increase in power necessary to increase the clock speed, which determine execution times.

Fig. 3. Power consumption of ALU related components[6][8][10][1][2]

Fig. 4. Delay time in execution for ALU technologies[4][6][8][1]

III. CONCLUSION

From the data shown, over time node length and execution time are decreasing. This decrease in size and speed comes at a price though. The data shows that the power consumption is increasing exponentially. In the modern age this does not only reflect the ALU as power production is a problem in other fields as well. Moore’s Law is in full effect in relation to the technology node length and it is clear to see that power consumption and execution speed are inversely related.

REFERENCES


<table>
<thead>
<tr>
<th>ALU or Floating Point Architecture Name</th>
<th>Device Technology</th>
<th>Datapath width (bits) or #bits in operands</th>
<th>Time for Operation or Design Type</th>
<th>ITRS Technology Node (nm) or Area (µm²) or Model of Chip used</th>
<th>Energy/Power Consumption (W or J) else indicate “low” or “high”</th>
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<tbody>
<tr>
<td>IEEE 754</td>
<td>Single Precision Floating-Point Unit</td>
<td>32-bits</td>
<td>CMOS CLK = .4 ns</td>
<td>CMOS CLK = .4 ns</td>
<td>15 nm Node</td>
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<td>Domain wall nanomagnet</td>
<td>Spintronic device</td>
<td>1-bit</td>
<td>269 ps</td>
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<td>160 µm²</td>
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<tr>
<td>Probabilistic Domain Transformation</td>
<td>Virtex 6 FPGA devices</td>
<td>32-bits</td>
<td>4.09 µs</td>
<td>n/a</td>
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<tr>
<td>Dual-rail pipelined Modified Bough–Wooley MAC</td>
<td>Self-timed multiply–accumulate units (MACs)</td>
<td>Varies</td>
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<td>Fine-Grain Pipelining</td>
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