Analysis of Logical Unit Power Factors from a Circuit Perspective

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Abstract—This paper will compare the technologies behind different ALU (Arithmetic Logic Unit) and FPU (Floating Point Units) from the perspective of the actual hardware implementations. Such as the comparison of different types of transistors, as well the higher level abstract design of these circuits. After review we will compare both the benefits and consequences for the specified designs. As well we will look at these designs in comparison to the data metrics graphed as a whole, to see where they fit on the time lines. Some of these designs covered in this paper will be the BGFB CMOS transistors in ALUs. Reconfigurable CMOS logic designs using MFIG-Mosfets. Along with base CMOS Full-Adders while indicating different implementations with different unique benefits and tradeoffs.

Keywords—Arithmetic Logic Unit (ALU), Floating Point Unit, ITRS Technology Node, Data Bus Width, Execution Time, Power Dissipation, Boolean Logic, Central Processing Unit (CPU), Multi-Input Floating Gate Mosfet (MFIG-Mosfet), Ripple Carry Adder (RCA)

I. INTRODUCTION

ALU an acronym for arithmetic logic Unit is digital circuit which accepts multiple binary operands to represent integer values in order to perform numerous arithmetic and bitwise operations on the given numbers. The ALU is essential to the design of modern technologies such as the CPU or Central Processing Unit. The ALU allows for the calculation of tasks as simple as just calculating the sum of two integers and even more complicated tasks such as graphical processing in your graphical processing Unit. Along with ALUs we also have the FPU within the CPU this is very similar to the ALU, the main difference being the input operands are represented as floating point numbers. When designing these digital circuits in the CPU and GPU they require the implementation of multiple ALUs and thus require a certain space efficiency. This requirement has led to the development of new technologies in ALU design to allow for more complicated faster circuits.

In order to better understand the circuit analysis in this paper and how each circuit has affected different data metrics such as power consumption and bus width, we first must understand the logic units. The ALU has a couple of different input operands as well as a single output. At a high level we have the two integer operands, we will call A and B these are the two numbers we are performing the operations on. We also have the status output/input and opcode input; the status output typical is stored in a register that indicates different flags like Carry-Out, overflow and even the parity. While opcode is an input to indicate the type of operation that should be performed whether it be addition, subtraction or even shifting.

A few key terms to understand for the next section of metric analysis and circuit design are data bus width, ITRS technology node, power dissipation and transistors. The data bus is the channel which data flows over, the width size indicates the number of bits that will be passed over this channel. The ITRS technology was typically a numeric value to represent the half pitch value of a technology, the gap between two metal one lines. Power dissipation is the loss of energy in a unit of time which relates to the production of heat. A transistor is just a semiconductor that can be simply understood as a voltage controlled current source, they are essential to processing unit design.

In the next section this paper will examine some of the data metrics from the table at the bottom of this page as well as look at the specific technologies behind some of these different designs. Examining the differences in the physical circuit design and some of the new designs being implemented and their effects on these data metrics.

II. LITERATURE REVIEW

Due to increased chip density along with the decrease in size of node technology, power dissipation has become a rising issue; Having such a high density of circuits introduces higher risk for factors such as overheating. In order to understand how the technologies are evolving for low power operations with this increase in chip density we first need to understand the power consumption/dissipation of some of the ALU/FPU designs out there. Different power reducing techniques such as reducing voltage, load capacitance or switching frequency of the output node, are being used to design low power, high-performance chips based on CMOS. [13]

The first design we will look at is the ALU design with reconfigurable CMOS logic. This design takes advantage of MFIG-Mosfets which are mosfet’s with multiple gates and thus behave differently from traditional mosfets. An example of the transfer characteristics of a 4-input floating gate-CMOS inverter can be seen in the figure below [21]. The design for this first
ALU uses these inverters in a 4-bit RCA design. The full adder circuit can be seen in Figure B below.

This design when implemented into a fabricated ALU takes of an area of 830 x 935 micrometers; While the circuit takes up 293 x 160 micrometers on its own [21]. This design as well has a power consumption of .5 mW [21]. The design implements a fewer number of transistors as compared to some previous designs to the implementation of the MIFG Mosfets as opposed to traditional transistors thus taking up less space.

The next design is a fast ALU design for lower voltage operation using BGFSB to reduce voltage threshold on the transistors. The BFGSB method reduces the voltage threshold in order to decrease the gate delay and reduce power [13].

The final design we will look at will be an IEEE 754 Single Precision FPU in both 15 and 45 nm in order to illustrate the relation between the technology size and power. Another factor that can be illustrated is the difference in Cell area of these two different technology sizes; with the IEEE 754 we see that the Cell area of the 15nm technology is 30% smaller than that of the 45nm [1]. The same benefit in the 15nm technology can be seen in regards to both power and speed. The total Power of the 45nm with a period of 5 ns was simulated to be 2.048 as compared to the 15 nm with the same clock rate to be .6340 [1]. Reducing the clock period on the 15nm shows there to be a large increase in the total power but also see a drastic increase in speed as compared to what the 45nm technology is capable of at the same clock rate.

III. DATA ANALYSIS

The following section depicts the analysis of data to be found from the numerous sources in the reference. All data has been
shown is illustrated at the bottom data metric chart. The charts depict the relationship of data bus width over the course of years as well as the energy consumption compared to other designs. As well as illustrating the relation between the node size of a technology and the power consumption of said technology.

![Graph depicting the different power usages for multiple designs of both floating point units as well as arithmetic logic units.](image1)

**Fig. 1.** Graph depicting the different power usages for multiple designs of both floating point units as well as arithmetic logic units.

![Graph displaying the relation between the ITRS node size and the power consumption of two adders and a multiplier design.](image2)

**Fig. 2.** Displays the relation between the ITRS Node size and the power consumption of two adders and a multiplier design.

### IV. CONCLUSION

Evidence from the analysis of these four different technologies as well as data metric analysis of over 10 different technologies shows a continuous trend. First of all, Moore’s law is still clearly in affect as technology size decreases as time continues. The overall power and efficiency of the technologies improves as the technologies reduce and new designs are implemented such as the BGFSB transistors. These newer designs have led to higher circuit density but lower overall circuit area for chips. As time approaches and Moore’s law depreciates, we will begin to see a move from the reduction in technology size to instead new innovative circuit designs.

### REFERENCES


<table>
<thead>
<tr>
<th>ALU or Floating Point Architecture Name</th>
<th>Device Technology</th>
<th>Datapath width (bits) or #bits in operands</th>
<th>Time for Operation or Design Type</th>
<th>ITRS Technology Node (nm) or Area (µm²)</th>
<th>Model of Chip used</th>
<th>Energy/Power Consumption (W or J) else indicate “low” or “high”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy and Area Analysis of a Floating Point Unit [1]</td>
<td>C-MOS</td>
<td>32 bits (operands)</td>
<td>N/A</td>
<td>N/A</td>
<td>IEEE-754 Single Precision</td>
<td>45 nm and 15nm [ITRS Node]</td>
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<tr>
<td>A Tunable Majority Gate-Based Full Adder [2]</td>
<td>Spintronics</td>
<td>1 bit</td>
<td>Domain wall nano-base full adder</td>
<td>N/A</td>
<td>N/A</td>
<td>150um²</td>
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<tr>
<td>Ultra-Area-Efficient fault tolerant QCA adder [28]</td>
<td>QCA</td>
<td>1 bit (operands)</td>
<td>Ultra-area-efficient fault tolerant QCA full adder</td>
<td>N/A</td>
<td>N/A</td>
<td>18nm²</td>
</tr>
<tr>
<td>Energy-Efficient Multiplier Less Discrete Convolver through probabilistic domain transformation [3]</td>
<td>C-MOS</td>
<td>128 bit (operands)</td>
<td>N/A</td>
<td>3.08 us energy efficient multiplier</td>
<td>N/A</td>
<td>Virtex 6 FPGA (XC6VLX550t)</td>
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<tr>
<td>Design of a 1.7-GHz Low-Power Delay-Fault-Testable 32-b ALU in 180-nm CMOS Technology[17]</td>
<td>C-MOS</td>
<td>32 Bit</td>
<td>CMT Adders and RCA output adders</td>
<td>N/A</td>
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<tr>
<td>ALU Design using reconfigurable cmos logic[21]</td>
<td>C-MOS</td>
<td>4 bit</td>
<td>RCA</td>
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<td>N/A</td>
<td>Full adder - 293x160um² 4-bit – 830x935um²</td>
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<td>Clock gating based energy efficient ALU design and implementation on FPGA [12]</td>
<td>C-MOS</td>
<td>8 bits</td>
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<td>N/A</td>
<td>90nm spartan-3 FPGA</td>
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<td>Improving Power-awareness of Pipelined Array Multipliers using 2-Dimensional Pipeline Gating and its Application to FIR Design [9]</td>
<td>C-MOS</td>
<td>16 Bits</td>
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<td>N/A</td>
<td>.24um static CMOS logic</td>
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