Abstract—In this paper, I propose research analysis of application-driven ALU designs and algorithms that show advance in technology from 2002 to 2016. I will introduce domain wall nanomagnet based devices which enable designers to be transistorless and overcome low speed switching concerns along with other technology such as a standard IEEE-754 Floating Point Unit and how it used two technology nodes to results show that using 15nm technology can have four times less energy and three times smaller footprint. Along with a study on clock gating based on energy efficient ALU designs and reduction of clock and power consumption where the clock power is 50% of 100 MHz and 41.46% of 1GHz. These studies demonstrate different methodology to show effectiveness in ALU design.

Keywords—high-speed, energy efficient, ALU, Full Adder, CMOS, minority function, fault tolerance, process variation, clock gating, bridge style

I. INTRODUCTION

While technology for cloud computing, laptops, computers and cell phones all have difference variances for power efficiency; microprocessors are needed in every type of technology. The ALU is the fundamental component to the microprocessor. In ALU, arithmetic logic unit is a combinational electronic circuit that is a component to a microprocessor. ALU performs arithmetic and bitwise operations using binary numbers and is typically partitioned into function modules and control blocks (Application-Driven Power Efficient ALU Design) along with being comprised of three modules (arithmetic, logic, bit shift unit): module one adds or subtracts the numbers being inserted, module two bits are shifted in the third module and module three the output is implemented by a multiplexer which controls the instruction sets codes. The modules perform Boolean (such as AND, OR, XOR) or arithmetic (such as ADD, SHIFT) operations (Energy Efficient Technologies for Sustainability (ICETES), 2013 International Conference on, vol., no., pp.93,97, 10-12 April 2013.). The inputted bits then go to the data path and the control path checks each step throughout all the instructions and the output resultants go to the register file which does all the computations and produces the 32-bit result.

The data bus width is the width and clock rate of the data bus which determines the number of bytes per second it carries (Wikipedia). ITRS technology node or International technology roadmap for semiconductors dominates the technology scaling as its used to describe and differentiate technologies used in fabricating integrated circuits (Wikipedia). Execution time or runtime is the time in which the program is running. Power dissipation is when the circuit loses voltage, power becomes dissipated and the power is defined by the inductor multiplied by the voltage (Wikipedia). Energy consumption of processor is when the microprocessor produces heat or wastes energy and to find the power dissipated by the resistor.

In Section 2, the study will show full adders using CMOS technology and the last fifteen years and how clock gating techniques, fault tolerance, energy efficiency and process and algorithms changed to comply for custom driven applications and for other uses of applications to move technology forward. The study will show an array of designs and algorithms achieving the same and different technology results, while also exposing information about the efficiency and application uses.

II. LITERATURE REVIEW

In 2016, a domain wall nanomagnet based device was studied promising alternative technology to CMOS in memory and logic. The results have shown that the physical equations are functional to overcome low speed switching concerns and was verified using SPICE circuit simulators. This is interesting as the device is transistorless and leverages nanowires to get the information in bits for the memory. While in 2015, a standard IEEE-754 Floating Point Unit was analyzed using two different ITRS technology nodes. The results show that using 15nm technology we can have four times less energy and three times smaller footprint. Originally the research was 45nm and 15nm technologies, but as the information was synthesized using HDL 15nm was less in the cell area analysis by 30% and energy analysis by three fold. And in 2013, a study on clock gating based on energy efficient ALU designs and implementations took place. And the results shown that the ALU was able to achieve reduction of clock and power consumption. Clock power is 50% of 100 MHz and 41.46% of 1GHz, etc. and with this clock gating technique, low power ALU design is the next stage (Energy Efficient Technologies for Sustainability (ICETES), 2013 International Conference on, vol., no., pp.93,97, 10-12 April 2013.).

In 2013, a power efficient ALU design made for modern microprocessors methodology was studied to achieve high level power. The results shown that the 8bit ALU gives options between getting power efficiency and operation frequency to achieve high level power as it was found this was made for a custom application. The benchmarks proposed was the 74X-Series and the ISCAS85 based on .35um. Also in 2013, fault demotion using reconfigurable slack or FaDReS proposed a way to approach fault handling while exploiting the memory of the programmable gate arrays. The results shown that the fault detection is accomplished by adding an extra layer of hardware and the testing shows many results leading to advantages with the algorithm. Although according to the study this requires a significant power overhead for FaDReS. A new approach in 2011, a high speed full adder based on minority function and bridge style for nanoscale is proposed to improve speed and processor while reducing sensitivity to the process was studied. The results shown that the full adder is energy efficient and superior to other modern designs as function is used to implement sum signals based on the bridge style.

In 2002, a fast ALU design in CMOS was analyzed for low voltage operation. Results have shown that the four bit ALU has shown a lot of potential as it could be used for low voltage and high speed applications since the ALU has been design in 1.2um, and the BGFSB method is based on latch up action triggering inside the circuit. Also in 2002, a ALU design using reconfigurable CMOS logic where it has been designed for 1.5um and 3-volt operation. The results have shown that using MIFG-CMOS devices is a strong way to achieve reduction in area, power consumption, etc. Both designs use low energy and power consumption and a four bit data path in bits, along with ripple carry adders and 4 to 1 MUX for the operations.

III. DATA ANALYSIS

Figure 1 shows the differences between the selected designs for the ITRS technology node vs the year. The data shows how ITRS node
declined in size as time progressed from 2002. In 2002, the data shows an excessive amount of nodes of approx. 3500 to 1500 nm. This is due to different ALU designs, and space complexity.

Fig. 1. This graph outlines ITRS technology (nm) in the given year

Figure 2 shows the difference between the power or energy differences in the designs chosen vs the year. In the older years in 2002, you can see that the powers design was based off of high and lows, whereas todays current technology has shifted us to watts which depending on the design could be a small amount or a big amount depending on the voltage or GHZ.

Fig. 2. This graph outlines the power or energy supplied in the given year

Figure 3 shows the difference between the data bus width in bits vs the year. The graph shows that between 2002 to 2016 there has been a huge jump in technology for full adders between CMOS technology, algorithms, and power dissipation. During the research it was found that when trying to reduce energy and cell area it was common for the researchers to use a 4-bit ALU design in 2002 and from 2011-2016 it seemed 8-bit adders were more efficient. The researchers were able to make microprocessors for custom and all applications while also lowering power between 3-4 fold. As shown in Module-08 it is shown that computing devices double in capability and halve in cost about every two years while the transistors per chip increase exponentially as in 2014 there was 20 million transistors per chip for the Xilinx XCUV440 compared to the 1980 intel processor which has 29,00 transistors/chip. Also the DRAM based on the trend shows that it will continue to increase exponentially per dollar every five years.

IV. CONCLUSION

It has been found that in 2002 to 2016 there has been a huge jump in technology for full adders between CMOS technology, algorithms, and power dissipation. During the research it was found that when trying to reduce energy and cell area it was common for the researchers to use a 4-bit ALU design in 2002 and from 2011-2016 it seemed 8-bit adders were more efficient. The researchers were able to make microprocessors for custom and all applications while also lowering power between 3-4 fold. As shown in Module-08 it is shown that computing devices double in capability and halve in cost about every two years while the transistors per chip increase exponentially as in 2014 there was 20 million transistors per chip for the Xilinx XCUV440 compared to the 1980 intel processor which has 29,00 transistors/chip. Also the DRAM based on the trend shows that it will continue to increase exponentially per dollar every five years.

REFERENCES


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<th>ALU or Floating Point Architecture Name</th>
<th>Device Technology</th>
<th>Datapath width (bits) or #bits in operands</th>
<th>Time for Operation or Design Type</th>
<th>ITRS Technology Node (nm) or Area (µm²) or Model of Chip used</th>
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