In Depth Analysis of the Progression of Full Adder Devices Over Time

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Abstract—The main objective of this paper was to analyze the general progression of full adder design technology over the past 10 years. Several metrics were evaluated over eight papers. Technology node or feature size was measured in order to observe the state of fabrication technology at the time a design was published. Operation time and power consumption were also measured to determine the performance of the device. The die area of each design was also measured to account for the progression of space complexity. Of the full adders analyzed, two in particular utilize unique technologies in their design: the ASL adder with its use of spintronics and the carbon nanotube adder.

Keywords—Technology node, data bus width, power dissipation, clock rate, ALU, full adder, feature size, power-delay-product

I. INTRODUCTION

An arithmetic logic unit is an electronic device which performs bitwise operations using binary digits and outputs the result. The inputs of an arithmetic logic unit generally consists of 2 operand buses (or lines) and a control path (bus). The control path of an ALU is used to choose the operation performed on the operands. An ALU has an output path (bus) used to carry the result of the performed arithmetic operation. ALUs act as the central building blocks of modern devices such as computer processors and IOT technologies.

Several keywords are used to describe the chosen systems. These keywords include, but are not limited to: execution time, ITRS technology node, processor energy consumption and power dissipation. ITRS technology node is a metric which represents the minimum spacing distance between two metal lines achievable by a fabrication process. Processor energy consumption is the measure of energy a system requires to complete a calculation. Execution time is the total time needed for a system to complete its intended operation. The width of a data bus (data bus width) is the number of bits that are transferred per clock cycle on the bus. Power dissipation is a measure of the Watts dissipated by a system at a given time. It consists of both the power used by the switching elements in the system and the power wasted as heat by the system.

Section 2 consists of an in depth analysis of 8 full adder designs proposed from 2005 to present. In section 3, a series of metrics relationships are shown and briefly discussed. The conclusion section 4 provides a summary recap of the report and a few closing statements regarding the trends observed.

II. LITERATURE REVIEW

In 2005, a hybrid full adder architecture was proposed. The design utilized a 180nm technology node and had a minimum power consumption of 0.918 microwatts. Maximum operation time of the device occurred at its lowest power mode and totaled 1.4 ns. This longer operation time is most likely a result of the feature size of the device. The full adder cell analyzed consisted of 3 inputs and 2 outputs.

A new nonvolatile full adder design was proposed in 2008. The device was based on Logic-in-Memory architecture and had a feature size of 180nm. A primary goal of the design was low power consumption. Using magnetic tunnel junction a minimum power consumption of 16.3 microwatts was achieved. The design had a normalized delay of 219ps which was relatively close to the CMOS counterpart while still maintaining a significantly lower power consumption.

A carbon nanotube full adder cell was published in 2009 which consisted of carbon nanotube based transistors. The design was created with the goal of overcoming traditional performance trade-offs that affected electronic devices at the time. Using CNT based technology, a low power high performance cell was constructed. The technology node of the device was 180nm. A top execution speed of 12.184ps was achieved by the device with a power consumption of 3.41 microwatts.

In 2011, a minority function bridge style full adder was proposed. The cell was based on CMOS technology and was tested using multiple technology node sizes. At a node size of 32nm the MBFA reached an operation speed of 109.32ps. At these metrics, the device had a power consumption of 0.7668 microwatts. The delay time of the device decreased as the supply voltage increased. However, the power consumption was increased as the supply voltage increased and vice versa. This trend showed an inverse relationship between the power consumption of the device and its speed.

A new hybrid full adder circuit was proposed in 2015. The goal of the design was to achieve low power consumption and
delay using 2 modified XNOR modules and a Carry Generation Module. The feature size of the analyzed design was 90nm. The proposed design was found to have a delay of 224ps and a power consumption of 4.1563 microwatts at this feature size.

In 2015, an All-spin Logic based full adder design was proposed and analyzed. The design used graphene based all-spin logic gates in order to decrease operation time and power consumption. A primary advantage of this design was that it had no standby power. The design sacrificed power consumption (400 microwatts) and speed (1.2ns) in favor of low standby power and a smaller die area (0.69 square micrometers).

The last device analyzed was a domain wall nanomagnet based full adder. Device had an area of 160 micrometers squared and operated in two modes. In low-power mode the device sacrificed speed (877ps) for power consumption (85 microwatts). In high speed mode the device sacrificed power consumption (1364 microwatts) for speed (269ps). Since the full adder is a spintronic device, it had a significantly low standby power consumption.

III. DATA ANALYSIS

Figure 1 shows the progression of die area for the analyzed full adders over time. The area of the units generally decreased over time.

In figure 2, the trend of the power consumption over time can be observed. Data gathered from the papers showed power consumption of full adder design generally increasing over time.

IV. CONCLUSION

Of the designs measured, a general trend of power-consumption vs operation time was observed. As the operation time decreased, the power consumption increased to compensate. Power consumption of the adder designs also shared a relationship with their publishing year. As time progressed from 2005 the power consumption of the full adders increased. These relationships show a shifting
focus on adder designs of increasing performance and energy consumption. While there were a few outlier values, the die area of the designs tended to decrease over time. This is most likely due to decreasing fabrication costs of integrated electronics over time.

REFERENCES


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