Survey of Techniques for Continuing Improvement of Fundamental Computing Hardware

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Abstract—Various full adder design techniques are surveyed, with performance comparison made by their execution time and energy consumption. A design incorporating Magnetic Tunnel Junction technology operates without static power dissipation. A design incorporating carbon nanotubes displayed impressive speed and lower power consumption. A 32-bit ALU design based on feedback switch logic and a 32-bit FPU design based on the 15-nm ITRS technology node are also examined to demonstrate the scaling effects of the data bus width on delay and power consumption. The ITRS technology node a design incorporates is shown to greatly influence the performance of both delay and energy consumption of any design.

Keywords—Full Adder, ALU, CPU, Beyond CMOS, ITRS Technology Node, Magnetic Tunnel Junction, Feedback Switch Logic

I. INTRODUCTION

Arithmetic Logic Units (ALUs) and Floating Point Units (FPUs) are fundamental to computing. All software is composed of instructions which are executed through ALU and/or FPU operations.

ALUs enable integer calculations, including addition, subtraction, multiplication, and division. ALUs also enable logical tests including AND, OR, and XOR.

FPUs enable the equivalent floating point calculations to those performed by ALUs. Conventional FPUs implement the IEEE 754 Floating Point Standard unit [1].

ALUs and FPUs operate on values stored in registers and on immediates, values which are specified during run time and/or compile time. They perform the operation specified by the control path. They output their values to along data paths for storage in registers or external memory, or transmission across a network. Additionally, ALUs can

ALUs and FPUs receive their input from and pass output along the data bus. ALUs and FPUs can be designed to take advantage of various data bus widths, but are conventionally designed for data buses with a width that’s a power of 2.

ALUs and FPUs are constructed with arrays of full adders. Optimization of the constituent full adders is essential to continuing the performance gains charted by Moore’s law. The performance of full adders is considered by competing metrics of execution time, how quickly addition occurs, and power dissipation, how much energy is expended during the execution of the operation. Both metrics are heavily influenced by the ITRS technology node, the precision of fabrication of the integrated circuit. Smaller ITRS nodes enable smaller devices which consume less energy and allow greater density.

Various techniques to improve full adder designs are reviewed in the next section. An example of both a complete 32-bit ALU and a complete 32-bit FPU are reviewed as well to demonstrate the different performance profiles of the two devices.

II. LITERATURE REVIEW

In 2008, a full adder design utilizing magnetic tunnel junctions was analyzed in comparison to a conventional CMOS design [2]. It achieved a 219 ps delay at 16.3 μW dynamic power, compared to the conventional 224 ps delay at 71.1 μW dynamic power. This design also eliminated any static power requirements, compared to the 0.8 nW required for the CMOS design. In 2009, a full adder design incorporating carbon nanotubes in its construction achieved a 12.2 ps delay with 3.4 μW of dynamic power consumed [3].

In 2011, a full adder based on CMOS bridge style and minority function achieved a 151.3 ps delay and 0.68 μW power consumption [4]. That adder design was produced at the 45-nm ITRS technology node. A 2013 design produced at the 22-nm technology node incorporating double-gate controllable-polarity FETs possessed a 171.18 ps delay and 87 nW power consumption [5].

In 2015, a 90-nm technology full adder design based on CMOS and transmission gate logic is shown to possess a 91.3 ps delay and [6].

In 2009, one 32-bit ALU design based on feedback switch logic
III. DATA ANALYSIS

Fig. 1. Comparing the power consumption per bit between two relatively high power devices.

Fig. 2. Comparing the power consumption per bit between two relatively low power devices.

Fig. 3. Comparison of the publication’s year published and the ITRS node used for the design.

Fig. 4. Comparison of the publication’s year published and the adder delay per bit.

IV. CONCLUSION

The techniques presented enable designers to optimize their products by selecting the appropriate tradeoff of speed and energy/power consumption for their particular application. Designers are typically best served by incorporating devices constructed with the cutting edge, smallest ITRS technology node.

REFERENCES


<table>
<thead>
<tr>
<th>ALU or Floating Point Architecture Name</th>
<th>Device Technology</th>
<th># of bits in operands</th>
<th>Time for Operation or Design Type</th>
<th>ITRS Technology Node (nm)</th>
<th>Energy/Power Consumption (W or J) else indicate “low” or “high”</th>
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<tr>
<td>Fabrication of a Nonvolatile Full Adder Based on Logic-in-Memory Architecture Using Magnetic Tunnel Junctions</td>
<td>magnetic tunnel junctions</td>
<td>1</td>
<td>219 ps</td>
<td>N/A</td>
<td>N/A</td>
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<td>Two novel ultra high speed carbon nanotube Full-Adder cells</td>
<td>CNFET</td>
<td>1</td>
<td>12.188 ps</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>High-speed full adder based on minority function and bridge style for nanoscale</td>
<td>CMOS bridge style and minority function</td>
<td>1</td>
<td>151.3 ps</td>
<td>N/A</td>
<td>N/A</td>
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<td>Power-Gated Differential Logic Style Based on Double-Gate Controllable-Polarity Transistors</td>
<td>double-gate controllable-polarity FETs</td>
<td>1</td>
<td>171.18 ps</td>
<td>N/A</td>
<td>N/A</td>
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<td>Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit</td>
<td>CMOS</td>
<td>1</td>
<td>91.3 ps</td>
<td>N/A</td>
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<td>A Tunable Majority Gate-Based Full Adder Using Current-Induced Domain Wall Nanomagnets</td>
<td>domain wall nanomagnet</td>
<td>1</td>
<td>269 ps</td>
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<td>Design of Low Power High Speed ALU Using Feedback Switch Logic</td>
<td>feedback-switch logic</td>
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<td>349.5 ps</td>
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<td>Energy and Area Analysis of a Floating-Point Unit in 15nm CMOS Process Technology</td>
<td>multi-input floating gate (MIFG) CMOS</td>
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<td>N/A</td>
<td>1.6 ns</td>
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