Time Eclipsing Changes of the CMOS and Other Device Technologies in ALU and Full Adder Devices

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Abstract—The objective of this paper is to evaluate some of the fundamental metrics of Arithmetic designs. It compares the changes in the Data bus width, power, and ITRS technology nodes over time. Some of the ALU designs examined are: 4-bit ALU design with the back forward gate forward substrate bias(BGFSB) method used in a 1.2 μm N-well CMOS technology, novel ultra-high speed carbon nanotube full-adder cells, and 15nm CMOS process technology in an IEEE 754 single floating point unit.

Keywords—Full-adder, data-width, CMOS, ITRS Technology node, ALU, Floating point unit, power dissipation.

I. INTRODUCTION

ALU or Floating Point Unit produce different results in different size node technology [1]. Design advances result from a balance between speed and power consumption in devices [11]. Calculation of operands is important to the performance of technology devices. Successful calculations of operands provide speed and efficiency. As speed and efficiency of the calculation of operands increases, technology device use can expand. Operands are used in ALU operations, such as addition, multiplication and other Boolean instructions.

Arithmetic Logic Unit(ALU) is digital electronic circuit that performs number and bitwise operations on integer numbers represented by ones and zeros(wiki). A Floating Point Unit is a similar circuit that performs operations on floating point numbers [1]. The input of ALU or Floating Point Unit are generally two 32-bit long operands [1]. Additional inputs can be a carry in from a previous operation. The output of ALU or Floating Point Unit is of a 32-bit width.

The data bus width is the number of bytes of data the data bus can transfer at one time [17]. The ITRS technology node is a metric used to describe and differentiate the technologies used in fabricating integrated circuits [1]. Execution time is the time it takes for a program to execute. Power dissipation occurs when an electronic device produces an unwanted product that wastes energy, such as heat [13]. Energy consumption of processors, also, is defined as a loss of energy. The energy consumption of processors is from switching devices contained in the processor [13]. These devices include registers, transistors, and gate capacitances [11].

In Section 2 of this paper, there are eight ALU or Floating Point Unit designs spanning from the year 2002 until 2015 that are reviewed. These designs include several ALU designs in CMOS and with Full Adders. The ALU designs in CMOS, include a Single Precision Float Point Unit in 45nm and 15 nm CMOS technology devices [1], an 18 nm CMOS technology [17], a CMOS with low operation [13], a reconfigurable CMOS logic [21], and a 0.18 μm CMOS technology [28]. The ALU or Floating Point Unit designs with Full Adders features a two novel ultra-high speed carbon nanotube technology [11], a design with magnetic tunnel junctions [25], a design based on an all-spin logic device [26], and a design for energy-efficient arithmetic applications [28].

II. LITERATURE REVIEW

The resources published in the years ranging between 2002 through 2005 focus on ALU design in CMOS. In a 4-bit ALU design discussed, the back forward gates forward substrate bias(BGFSB) method was used in a 1.2 μm N-well CMOS technology [13]. In this ripple carry adder design, the BGFSB improves the circuit delays, resulting in low power [13]. The gate width in the NMOSFET used had a width of 1.8μm and a length of 1.2μm [13]. In another 4-bit ALU, the MIIG-CMOS inverter design required capacitors at the input stage, that caused a delay in the circuit [21]. Because of this, transistors had to be resized. The P-MOS and N-MOS transistors had ratios of 13.6/1.6 and 8.4/1.6 in the full adder circuit. The ratios had to be increased for the cascaded stage, to reduce the delay in the SUM and CARRY bits [21]. In the 32-bit ALU in 180-nm CMOS technology discussed in source 17, the low power operations allowed for reduction in ALU total energy for the CMOS technology and reduction in leakage power, without sacrificing performance. A circuit supporting a design-for-test(DFT) showed more delays, than a non-DFT design [17]. With an area of 800 µm x 600 µm, the technology used for the 32-bit ALU resulted in lower power usage [17].

Between the years 2008 through 2013 full-adder designs were common in technology discussed in resources published. Tradeoffs in speed and power were being looked at, such as in the two designs for novel ultra-high speed carbon nanotube full-adder cells. The carbon nanotube- based transistors (CNFETs) in the design for Full-Adders resulted in high performance and low power arithmetic circuits. The low-power design was a result of its low ON current and super cutoff [11]. In source 28, the full-adder cells were designed with an alternate internal logic structure and pass transistor logic styles. This design reduced power-delay product. The simulation results for the 1 bit full-adders showed average power ranging from 60.6 µm to 293.8 µm [28]. In source 25, a full-adder was designed with magnetic tunnel junctions(MJT). Magnetic tunnel junctions are close in comparison with a two valued resistor [25]. The MJT combined with MOS transistors result in switching of order ns or less [25]. This design reduced the dynamic power dissipation of the circuit [25].

Two of the resources being discussed in this paragraph were published in the year 2015. They in source 26, the replacement or combination of CMOS 40 nm technology with all-spin logic device technology in full-adders is discussed. The design would
result in low power consumption and high switching speed [26]. In source 1, 45nm and 15nm CMOS process technologies were compared of a floating-point unit. The cell area in 15 nm technologies was significantly less than 45 nm technology [1]. The 45 nm design showed power consumption of 3.15 fold to 4.56 fold larger than the same design that used 15 nm technology [1]. The floating point unit was seen to be faster and consume less energy in the 15 nm technology [1].

III. DATA ANALYSIS

As the years have progressed there has been a trend in the metrics of devices with ALUs or Full Adders discussed in this paper. The data bus width studied has increased overtime. The ITRS technology node has decreased during this same time. Furthermore, the power consumed by the devices studied has decreased over the years. Over a span of thirteen years, devices with improved CMOS and other device technologies have become more efficient.

![Year vs. Data bus width](image1)

![Year vs. Power](image2)

![Year vs. ITRS technology node](image3)

Fig. 1. <Write a Caption in your own words below each Figure.>

IV. CONCLUSION

The results in these sources show scaling trends of 130 nm to 14nm process technology nodes in 2002 to 2015, with a few lingering process technology nodes in the unit of μm. Moreover, the Ripple Carry Adder design grew in popularity according to the published papers in the early 2000s. Minimizing the bit-width, and reducing the supply voltage in the ALU or floating point unit can result in the reduction of energy used. In
all the technologies discussed the tradeoff between speed and energy consumption of the processor is still being modified and changed, along with new technology designs.

REFERENCES


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