Analysis of Techniques Designed to Ensure Data Reliability for Emerging Technologies and Memory Cells

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Abstract—Emerging technologies continue to enhance the electronics field as devices and circuits increase in complexity and necessity. The onslaught of real time devices controlling and interfacing in every day devices and safety critical applications call for reliable and efficient circuit design while decreasing the area and energy requirements of the design. Prominent techniques have been developed to help keep data consistent and to avoid soft errors happening in Single Event Upsets (SEU) and Double Node Upsets (DNU) where, for various reasons, one component or wire’s logical state on the data path is toggled (SEU) or even two components simultaneously are upset (DNU). The goal for this paper is to analyze a few techniques designed to ensure data reliability in memory cells and to describe some of the challenges and trade-offs that each technique has. At the conclusion of this work it is determined that Spintronic devices are the best designs to use with respect to energy consumption as this design’s energy consumption is the least in regards to the other proposed designs.

Keywords—Modular Redundancy, Magnetic Tunnel Junction (MTJ), Complementary Metal Oxide Semiconductor (CMOS), Soft Error Rate, Reliability, Non-volatile, Spintronics, Radiation Immunity, Single Event Upset (SEU), Double Node Upset (DNU)

I. PROJECT DESIGN

To analyze the techniques to ensure data reliability in memory cells, a plan was created to come up with a program written with machine code to calculate the energy cost of using different memory cell designs.

The program was designed to count the number of words found in a string of text based on a user defined query that is case insensitive. The program also finds the query inside words, even if the word is longer than the query. To accomplish this task, the MIPS processors instruction set was utilized and the dynamic instruction count was determined after running the program. The program flow can be visualized in Figure I. A string of text was stored in memory and then the program prompted the user for an input. After the query was defined, the program “purifies” the query i.e. removing any new line characters and forcing every uppercase letter to be lowercase. The program then loaded the first character of the string into a register and did checks against it. If the character is null, the program terminated and if the character is capitalized the program forced it to become lowercase. Then the character of the string is checked against the query. If the first character of the query matched the first character of the word in the string, the program will check the next character of the query. If the next character is null, then the end of the query was reached and the word matched. Increase a counter register to count the words. Otherwise, load the next character for the string and repeat this process. If the string character does not match and the character is a space, then the word is done so reset the query and continue. If it’s not a space, continue checking the next letter and continue this process.

The inputs chosen to test the program was a 103-word sentence that was given to contain 6 instances of the word “knight.” To test the program input was given as “knight” and “kNIgHT” which should result in equivalent answers if the program worked as expected. A separate case was tested as well, “knights”, to demonstrate that changing the input slightly can change the results. The results are shown in Figure II.
II. MEMORY Bit-CELLS

IIa. Redundancy and its effectiveness

To ensure a circuit’s reliability and ability to withstand SEU and DNU scenarios, certain methods are used to compensate for the various conditions in which the upsets occur. The simplest method to utilize is Triple Modular Redundancy (TMR). TMR is achievable when each bit of information is in triplicates. Each triplicate goes through a voter circuit to determine the bits which hold majority. The majority bits are then utilized as the final result and passed along. For TMR, the voter circuit is represented by the Boolean logic equation

\[ \text{Bit}_{\text{Result}} = (\text{Bit}_A \ast \text{Bit}_B) + (\text{Bit}_A \ast \text{Bit}_C) + (\text{Bit}_B \ast \text{Bit}_C) \quad (1) \]

Therefore, if any two bits are logical high, the result bit, Bit_{Result}, will become logical high. This is useful should any one bit experience a SEU the resulting bit will not be affected. This design is useful for SEU but is prone to error in a DNU scenario since two bits are flipped: the result bit will not maintain the correct state. In short: for any \( n \) bits “protected” by TMR, \( n \) bits can be protected against SEU [5] but not DNU. This can be mitigated by using N-modular Redundancy (NMR). The NMR technique uses \( N \) number of copies of the state/logical value and passes all \( N \) copies into a voter. To determine how many copies are needed to correct \( E \) number of errors the following equation can be used:

\[ 2 \ast E_{\text{Errors}} + 1 = N_{\text{copies}} \quad (2) \]

Using the modular redundancy approach may not be the most efficient way to protect against upsets when a frequent number of errors are expected due to the increasing number of copies required to ensure reliable data. To utilize NMR the energy and area requirements must allow for the extra copies. Essentially, a TMR hardened data path has an increased size and energy consumption 3-fold that of the standalone circuit. It stands to reason that an NMR approach will increase N-fold.

It is imperative, for this reason, that the voter used in a TMR approach is radiation hardened and is as reliable as possible. If the voter circuit were to experience an SEU, then the input logical values are moot and do not matter, as the result bit could be corrupted. All data that uses the corrupted result bit could contain corrupted results down the chain. The probability of the voter failing, resulting in the result bit to be flipped, must be taken into account when using the TMR approach. If one can afford the cost of TMR, it proves a simple and effective approach to reliability within a circuit, though it’s ineffectiveness in resolving DNU scenarios may cause issues if the circuit is to experience upsets frequently. A technique can be used with a hardened cell in which extra transistors are used to avoid the instance of an upset [5] as well as the use of Temporal Redundancy [1] (TR) can assist in the avoidance of DNU. TR utilizes sampled data at three different time intervals and votes on the results. Combined with TMR, a hybrid method was developed in [1] in which the resulting data is further hardened to protect against DNU. The rare event in which two DNU happen at the same time (the actual and hardened registers are upset simultaneously) is difficult to protect against and the hybrid technique does not protect against this kind of upset [1].

IIb. Emerging technologies

The use of emerging technologies is increasing the reliability and utilization of circuits in ways that were previously difficult. MTJ cells are a prime example of this as they use magnetic fields to create resistance in a circuit. This resistance is used to represent logical values. A drawback of MTJ cells, as of right now, is the fabrication process is prone to error: producing faulty MTJ cells as discussed in [2] which can cause low resistance values [6] in the cells and defects become apparent. As MTJ cells become more widespread, the defect rate should decrease as manufacturing processes are perfected [2].

By utilizing MTJ cells in the creation of non-volatile memory interfaces, a circuit becomes, intrinsically, radiation hardened since MTJ cells are generally not affected by radiation. Since this is the case, TMR can be used to fully harden a device but the overhead of TMR is drastically reduced since the standard CMOS overhead of TMR is avoided. This implies less energy spent and less area reserved for reliability’s sake while still maintaining a low Soft Error Rate [1] and the added benefit of radiation protection. The utilization of MTJ and spintronic technologies appear to increase performance (higher speed, lower heat) and decrease energy cost as well as highly increasing the reliability and effectiveness of fault correction techniques compared to CMOS devices and standard memory cell techniques.

Not only is it important to radiation harden the device, but energy could also be saved by using MTJ-based non-volatile storing devices as it reduces the amount of power leaked when storing devices [2]. Generally, there is static dissipation of power due to currents drawn continuously from a power supply. The use of non-volatile circuits could reduce the leaked power and increase the life of batteries used on a device or the amount of power necessary to run a circuit.
Overall, MTJ devices solve many of the complicated challenges proposed by using CMOS devices.

III. RESULTS AND DISCUSSION

To determine the effectiveness of lowering energy consumption when utilizing emerging technologies, the program created to count word occurrences was used. The dynamic instruction count was used to evaluate the energy cost in each design for reading from different memory interfaces. In this example all other instruction types used a constant energy cost including the energy used to store values/write to the memory interface. The following equation was used to calculate the energy cost where $E_i$ is the energy consumed, $I_i$ is the number of dynamic instructions and $x$ is the instruction type.

$$E_{Total} = I_{ALU}E_{ALU} + I_{Branch}E_{Branch} + I_{Jump}E_{Jump} + I_{Write}E_{Write} + I_{Other}E_{Other} + I_{Read}E_{Read}$$

(3)

$E_{Read}$ is determined from Table I.

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [2-4].

<table>
<thead>
<tr>
<th>Design</th>
<th>Energy Consumption For Each Bit-cell’s Read Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>3MR [2]</td>
<td>0.366 pJ</td>
</tr>
<tr>
<td>Spintronic [3]</td>
<td>0.15 pJ</td>
</tr>
<tr>
<td>Spintronic [4]</td>
<td>0.8 pJ</td>
</tr>
</tbody>
</table>

Using different methods from [2-4] and [7] to calculate energy consumed, the benefit of spintronic-based memory cells is shown to consume less energy than the other methods as shown in Table II.

Table II: Total Energy consumption for the assembly program using designs provided in [2-4].

<table>
<thead>
<tr>
<th>Design</th>
<th>Total Energy Consumption</th>
</tr>
</thead>
</table>

IV. CONCLUSION

Based on the proposed circuits in [2-4] and [7] it is shown herein that different methods can be used to enforce reliability in the transfer of data along the data path and protect against SEU and sometimes DNU consistently by TMR/NMR and TR methods and MTJ memory cells. As with all emerging technologies (as discussed in [2] and [3]) there are specific challenges that will be overcome as the frequency of use of these technologies increases. Some of these challenges like manufacturing defects will inevitably decline as manufacturers continue to perfect creating these small, yet effective, devices. Some topics learned from this project are:

- Basic spintronic concepts.
- CMOS and MTJ memory cells.
- Modular Redundancy and it’s uses.
- Use of the MIPS processor and its ability to analyze energy usage with different techniques.
- Writing an IEEE format paper.

As discussed in section III, the best design with respect to energy consumption is the Spintronic device proposed in [3] as it has the least energy consumption than the other designs at 130pJ.

REFERENCES


