Abstract - This paper is meant to evaluate the advancement of technology in memory. The main contributions of this paper will be analyzing the code for highspeed operations, research on reducing the bit error rate, and exploring the vast options on memory. It will cover the basics for different types of memory such as, SRAM, STT-RAM, and DRAM all the fabrications and design will be focused throughout this paper. More detailed in how lowering energy consumption with new design of memory is the future, and also increase the reliability of ram and lost memory bits. Spin Transfer Torque Magnetic Random-Access Memory has been discovered as a post Cmos technology for embedded and data storage, it is seeking for a near zero energy and high density. Static random-access memory (SRAM) is a type of memory that can be employed in processor-based computer systems. SRAM can store data without the need to refresh every so often compared to DRAM.

Keywords— STT-MRAM, SRAM, Non-Volatile Memory, Spin Transfer Torque Magnetic Random-Access Memory, DRAM

I. PROJECT DESIGN

The code is designed to search for a word inputted by a user to count the amount of times it has appeared in the string. In order to implement this design, we will have to input our string first in order for our program to know what string to look for. The code then does a conversion of the letters in lowercase, by doing so it would make our search and code run more optimized. Therefore, lowering our MIPS/mW and the amount of instruction count required. This allows the user to search all the words in the string and accounting all the cases if there were a mixture of lower and uppercase variants. This will wrap up the word search implementation needed for the problem. The program will transverse through the string looking for the letters inputted by asking the user. We then go to a true and false statement condition where if the letters continue to match the users desired word, the code will continue to loop until the full word is apparent. Once the code looks and detects the users letter that is not related to the users input, the code moves to the next string of letters, we then the code will loop and start the process again. Lastly, the code will store the number of times the letter has been appeared from the string.

The testing phase for the code is inputting words knight, KNIGHT, UcF, 43, and lastly bakery. We then put our first input that is used to generally check to see if the code works, the second input will be used to test an all caps letter word to see weather if the code works. Our second input is used to test the capitalized letters, to check if the code will convert it back to lowercase. The third input is a mixture of uppercase and lowercase to check if the code will react and sort the uppercase and lowercase, all to lowercase. The third input will prove if the code functions and searches properly for the desired word. The fifth input is used to see if the code will properly display the amount of the times a word that doesn’t appear in the string is used.

![Design Flowchart](image-url)
Sample Output:

```
Please input first word: knight
knight: 6
-- program is finished running (dropped off bottom) --

Please input first word: K N I G H T
knight: 6
-- program is finished running (dropped off bottom) --

Please input first word: UcF
ucf: 3
-- program is finished running (dropped off bottom) --

Please input first word: 43
43: 0
-- program is finished running (dropped off bottom) --

Please input first word: bakery
bakery: 0
-- program is finished running (dropped off bottom) --
```

Figure 2. Sample output of the testing of the inputs.

II. MEMORY BIT-CELLS

In today’s modern computer memory, the sense amplifier is one of the elements which makes up the circuitry on the semiconductor memory chip, also known as a integrated circuit. In modern electronic systems there are made up of two categories which are data and processing [6]. Data is stored in the memory for access in order to be used in processing and interactions with other devices, the performance of the memory is related to the performance of the electronic system. [1] A sense amplifier is the part of the read circuit that is use when the data is read from the memory. [4] A sense amplifier circuit uses two to six, but usually four transistors. There is one sense amplifier for every column of memory cells, therefore there is hundreds and thousands of the same amplifier on a modern memory chip.

The memory operation is the data in a semiconductor memory chips is stored in these tiny circuits called a Memory cell. The memory cells are only in two types, SRAM or DRAM cells where they are in rows and columns on a chip. The SRAM operation is to read the bit from a specific memory cell, the worldline along the cell’s rows is turned on, and activating the memory in the row. For any given row in the SRAM data array, each columns of the SRAM data array includes a covet SRAM bit cell row is controlled by the word lines corresponding to read and write operations. [5] The Stored value using 0 or 1 from the cell comes to the bit lines associated with it. The Dram Operation is very similar to SRAM; However, DRAM operation performs an additional function, its data in the DRAM chip is stored as an electrical charge in tiny capacitors in memory cells. The main advantages of DRAM cells is that the basic DRAM memory cell requires only a single transistor and a capacitor, thereby making DRAM cells very small and less expensive than SRAM cells.[5] The first problem with Dram Cam cells are that in order to refresh the dynamic storage nodes at a and b, a refresh cycle must be inserted between in order to match the operations. The second problem associated with DRAM cell is that, if separate bit lines are provided to allow simultaneous refresh and match its operations, the reading paths of the refresh operation can be disturbed by the simultaneous match operations. [5] When decreasing the amount of resistance in a magnetic tunnel junction it increases the SM and also the Voltage headroom [1]. Which will decrease the amount of error it gets, as the supply voltage is reduced. By using Transmission Gates, it can give use the maximum amount if full swing switching, therefore it will reduce our amount of reliability in these circuits. A Body voltage sensing based on its short pulse reading circuit in short terms called BVSC, approaches the issues of reliability and improved performance that are expected from other devices that are scaled. Since the process variation increases with a decreased scale it will reduce such issues. BVSC allows for a much larger read margin while reducing its disturbances, this is done by current pulse to MTJs.

Another Memory has been researched called Spin Transfer Torque Magnetic Random-Access Memory in short is called (STT-MRAM). [2] STT-MRAM is very practical for everyday use in embedded systems and data storage, it has zero volatility, near zero standby energy, and high density. The high reliability and very high energy efficiency is sought after in the memory area. The problem is faces is the reliability challenges of reading and writing failures. The Bit errors can be influenced by PV, and also it can also be affected by its thermal randomness. A STT-MRAM consists of using two ferromagnetic layers divided by a thin nonconductive barrier. [3] The Magnetic Tunneling Junction has two resistive states, it is determined by the magnetization direction of the fixed and free layers, if a parallel orientation is present it will produce a low resistance. If a anti parallel orientation it will result into a high resistance state.

The Pre-read and write of the sense amplifier combines the read and write functions in a single circuit. The circuit is responsible for writing the Magnetoresistive Random Access Memory which also stands for MRAM. [6] The bits using in speed of Gigahertz and magnetic tunnel junction, by using these design aspects in the PWSA will provide us with a high speed, lower power consumption memory, and lower our bit rate error. However, the sensing margin is due to a small low TMR of the 1T-1MTJ memory architecture. The series bit line resistance decreases the ratio of MTJs seen by the circuitry. [2]
III. RESULTS AND DISCUSSION

Calculating energy consumption using the program I have created. We are using the below energy consumption per instruction values:

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

<table>
<thead>
<tr>
<th>Design</th>
<th>Total Energy Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>EASA [1]</td>
<td>45.9pJ</td>
</tr>
<tr>
<td>VISA [1]</td>
<td>208.1pJ</td>
</tr>
<tr>
<td>PWSA [2]</td>
<td>4470.9pJ</td>
</tr>
</tbody>
</table>

1) $ALU = 1 \text{fJ}$  
2) $Branch = 3 \text{fJ} \times 10^9$  
3) $Jump = 2 \text{fJ}$  
4) $Memory = \text{Read Energy (Refer to Table I)} + \text{Write Energy (50fJ)}$  
5) $Other = 5 \text{fJ}$

The below table lists the required energy consumption to perform each memory write operation using the different circuits proposed in [1-3].

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [1-3].

<table>
<thead>
<tr>
<th>Design</th>
<th>Energy Consumption For Each Bit-cell’s Read Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>EASA [1]</td>
<td>0.23 fJ</td>
</tr>
<tr>
<td>VISA [1]</td>
<td>1.86 fJ</td>
</tr>
<tr>
<td>PWSA [2]</td>
<td>36.0 fJ</td>
</tr>
<tr>
<td>BVSC [3]</td>
<td>195.5 fJ</td>
</tr>
</tbody>
</table>

II) Formula used:

$E = (A * E) + (B * E) + (J * E) + (M (Read + W)) + (O * E) = Energy\ Consumption$

Variable definition:

A = Alu Instructions  
E = Energy consumption  
B = Branch consumption  
J = Jump instruction  
M = Memory instruction  
Read = Read energy  
W = Write energy  
O = Other instructions

IV. CONCLUSION

I have discovered the vast types of memory that has been innovated. We have only two types of memory cells DRAM or SRAM. The SRAM operation is to read the bit from a specific memory cell, the worldline along the cell’s rows is turned on, and activating the memory in the row. DRAM operation performs an additional function, its data in the DRAM chip is stored as an electrical charge in tiny capacitors in memory cells. They both are very good at what they do, one has advantages verses the other vice versa. It all depends on preference of memory type. Various read circuits and sense amplifiers seeking high reliability and lower energy cost includes EASA, VISA, PWSA, and BVSC. This shows that there are many types of read circuits and sense amplifiers that are efficient in full switching and reducing energy leakages. I also learned about the issues that brings along with the low error rate and low energy, which is the amplifiers ability to alleviate its reliability issues caused by process variation. As technology grows every day and we advance the process variation is essential for developing current and future advances to better memory, with higher reliability, lower energy consumptions and cost. Energy Aware Sense amplifiers shows a promising solution to the shrinkages of integrated circuits. By using our table 2 we show that EASA is the most energy efficient out of all the others which gave us a total of 45.9pJ for EACH Bit cell read operation.

REFERENCES


