Variation-Immune Resistive Non-Volatile Memory using Self-Organized Sub-Bank Circuit Designs

Navid Khoshavi, Soheil Salehi, and Ronald F. DeMara, *Senior Member, IEEE*

***Abstract*—While technology scaling enables increased density for memory cells, the intrinsic high leakage power of CMOS technology and the demand for reduced energy consumption inspires the use of emerging technology alternatives as Non-Volatile Memory (NVM) including STT-MRAM, PCM, and RRAM. However, their narrow resistive sensing margins exacerbate the impact of Process Variations (PV) in high-density NVM arrays, including on-chip cache and primary memory. Large-latency and power-hungry Sense Amplifiers (SAs) have been adapted to combat PV in the past. Herein, we propose a novel approach to actually leverage the PV in NVM arrays using *Self-Organized Sub-bank (SOS)* design. SOS engages the preferred SA alternative based on the intrinsic as-built behavior of the resistive sensing timing margin to reduce the latency and power consumption while maintaining acceptable access time. Our experimental results indicate that the PV effect in our case study may perturb around 27.5% of the data sensing operations from which 21.5% are classified as extremely vulnerable. SOS alleviates the sensing vulnerability by 40% on average to reduce the risk of application's contamination by fault propagation. Additionally, new categories of resistive read sensing dependability are defined for broad adaption.**

***Index Terms*—Magnetic Tunneling Junction (MTJ), Spin-Transfer Torque storage elements, STT-MRAM, Self-referencing schemes, Reliability, Process Variation, Read/Write Reliability, Sub-banking.**

I. Introduction

Emerging Non-Volatile Memory (NVM) technologies such as Resistive RAM (RRAM), Phase Change Memory (PCM) and Spin Transfer Torque Magnetic RAM (STT-MRAM) have received significant attention as promising approaches to overcome the CMOS-based memory storage challenges such as volatility and high static power consumption [1]. Even though the utilization of NVM technology in the overarching system can significantly reduce the leakage power issue, the PV effect has still remained as a limiting factor for NVM applicability and scalability. In particular, the PV in Magnetic Tunnel Junction (MTJ) devices utilized in STT-MRAM organization, manifests itself as variation in MgO thickness and MTJ geometry which in turn results in deviation of MTJ resistance [2]. Furthermore, the threshold voltage, V_{th}, and gate length, L_{eff}, of CMOS access transistors in STT-MRAM organization exhibit delay and driving current variations under PV, which negatively impacts the performance consistency of memory operation [3]. As the results of PV effect on both conventional and emerging semiconductor technologies, the difference between the sensed bit-line voltage and the reference voltage which is referred as *sense margin* can severely fluctuate, resulting in possible false detection scenario and increased bit error rate [4]. This issue has increased the demand for designing advanced low-power and reliable sensing circuits which can be integrated into PV-resilient system architectures while providing required sensing margin.

The work herein is motivated by the observation that around 27.5% of the sensed data in the PARSEC suite when utilizing a STT-MRAM based Last Level Cache (LLC) has the potential to be read incorrectly due to PV. Even though up to 6% on average of the incorrectly sensed data will be overwritten prior to be consumed by processor or to be committed to the main memory, which reduces the urge of their accommodation, there is still a significant portion of incorrectly sensed data that must be handled before manifesting themselves as wrong output, or application crash, or prolonged program execution [5]. This observation inspired a redesign of the schematic of SAs array in STT-MRAM data arrays to provide improved sensing margin.

To provide reliable sensing operation while taking the energy budget into consideration, we propose a circuit-architecture cross-layer solution suitable for multi-core processors as well as IoT devices. Our proposed technique, referred to as *Self-Organized Sub-bank (SOS)*, partitions STT-MRAM data arrays into several sub-banks to directly access requested data while introducing individualized sensing resolution. Sub-banks are evaluated and tagged during an initial *Power-On Self-Test (POST)* phase to identify the preferred SA for that particular sub-bank. To be specific, if the error rate of the impacted NVM cells in a sub-bank exceeds the predefined threshold, a High Resilience SA is assigned which is an adapted SA from the proposed SA in [6]. Otherwise, a Low Power Delay Product SA offering reduced delay and power consumption is assigned which is adapted herein from the proposed SA in [7]. SOS alleviates the sensing reliability of incorrectly sensed data by around 40% on average which results in reducing the risk of contaminating the application's data structure by fault propagation.

The remainder of the paper is organized as follows: The STT-MRAM organization is introduced in Section 2. Section 3 demonstrates the intuitive idea behind SOS design. Section 4 presents the experimental results. Section 5 concludes the paper.

II. The Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM)

As illustrated in Fig. 1, STT-MRAM utilizes MTJ device as storage element in which a thin insulating oxide later, e.g. MgO, is sandwiched by two ferromagnetic layers [6]. Moreover, the upper ferromagnetic layer is usually aliased as the free layer having a polarity of magnetic field which

N. Khoshavi, S. Salehi, and R. F. DeMara are with the Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL, 32816.

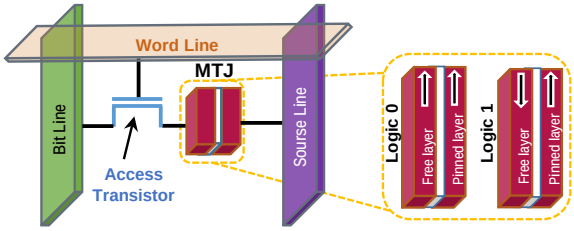

Fig. 1. An illustration of a 1T1R STT-MRAM cell embedded in the cache organization.

can be flipped during a write operation. Meanwhile, the lower ferromagnetic layer usually referred to as the pinned layer is designed to have its magnetization fixed. Thus, MTJs have a low (high) resistance distribution if the magnetization of the free layer and the fixed layer are parallel *P* (anti-parallel *AP*). Accordingly, low (high) resistance distribution is stored in MTJ, instead of traditional electronic charge or current flow [8], [9].

For a read operation, a small current is required to be driven from bit-line to source line. On the other hand, a successful write operation requires a current flow drive either from bit-line to source-line or vice versa, depending on the differential voltage between these two lines. Although STT-MRAM does not suffer from significant write endurance, however the advent of long write latency and high energy consumption exacerbate the reliability implications of STT-MRAM [10].

A. Process Variations in STT-MRAM

The imprecise fabrication process in nano-scale technology results in Process Variations (PV). The impact of PV on CMOS-based logic circuit and memory storage is a combination of *systematic variations* which are mostly caused by lithographic aberrations [11] [12] and *random variations* induced by random doping fluctuations [12] [13]. The effect of systematic variations is spatially correlated among the effective gate length, L_{eff}, while the threshold voltage, V_{th}, is influenced by random variations. The MTJ resistance is primarily changed due to PV impact on MgO thickness and MTJ shape [2]. In our PV model, we assume that the cache tag and peripherals (e.g., row decoder, column decoder, row buffer and SAs) are fabricated at the CMOS layer while memory cells are realized through MTJ devices. Since the MTJs are vertically stacked on top of the CMOS layer and these components are tightly coupled to realize the function of STT-MRAM, but the read sensing margin varies readily based on the effect of PV on that particular region of the die. Accordingly, we consider the same PV parameters to model both CMOS and MTJ variations in VARIUS [14] which is based on static analysis tool R and geoR package.

B. Extracting the PV Parameters

As listed in Table I, we choose our σ/μ for L_{eff} variation to be 10% to align with the previous measurements reported in [15]. We consider $\phi = 0.5$ based on [11] which means the gate length has a spatial correlation range close to half of chip's width [16]. We randomly select one map among a large pool of maps which are generated by VARIUS with resolution of one million (1000×1000) sample points. The degree of variation is shown by a range of colors. Each color corresponds to a specific value of sample points as shown in Fig. 2. In our simulation, we consider the amount of PV for each site based on the location of the LLC components within the floorplan and their associated sample points. Thus, VARIUS generates a relatively accurate estimation of the impact of PV on the read sense margin of each sub-bank data array.

C. Power-On Self-Test (POST)

As shown in Fig. 2 (a), the cache bank floorplan of STT-MRAM layer is superimposed on the map. In our SOS approach, each cache bank is partitioned into 16 sub-banks. The size of each sub-bank is matched with the word size to maintain the energy consumption of the tag to be as low as possible, e. g. 32-bits in our case study. We consider one additional bit per each sub-bank to identify the preferred SA for that particular sub-bank during post-fabrication resiliency assessment to PV. The POST phase is basically a March Test that targets PV-induced faults in STT-MRAM [17]. We assume the proposed SRAM March Test with *O(n)* test length can be utilized for our purpose because the tag and peripherals of STT-MRAM are considered to be implemented in CMOS layer. Thus, variation-induced delay fault in both SRAM and STT-MRAM manifests itself as the same fault model such as insufficient pre-charge time, insufficient sense time, insufficient amplify time, disturbance of sense operation, and simultaneously activation of multiple word lines.

In this regard, PV-aware March Test traverses all STT-MRAM data arrays and performs a sequence of operations (e. g., exhaust all pair-wise address transitions) to identify PV-induced delay faults in each cell [17]. If the error rate of the impacted STT-MRAM cells in a sub-bank exceeds the predefined threshold, the extra bit is set to '0' indicating that an array of reliable SAs are required for sensing data array of this sub-bank. Otherwise, the extra bit is set to '1' which indicates that an array of low-power SAs offering reduced delay and power consumption can be considered for that particular sub-bank. Since POST is a one-time operation, then it will not impact the performance of the memory as a whole resulting in incurring a negligible overhead. Taking advantage of this feature, we will be able to analyze memory cells before initiating the main stream operation, which identified those cells suffering the most from PV.

III. Self-Organized Sub-banks (SOS)

A. SOS Schematic for SAs Array Assignment to each Sub-bank

Among the contemporary proposed low-power and reliable SAs, we select two promising SAs that exhibit remarkable improvement in either reliability or energy consumption: 1) PCSA: the low-power SA circuit that incurs very low energy consumption compared to other designs [7], and 2) SPCSA: the high reliable SA circuit that offers approximately 2.5-fold reduced error rate compared to PCSA [6]. Herein, we call the ensemble of PCSA, SPCSA and MUX as a Merged Sense Amplifier (MSA) which utilizes each device's properties to increase the performance and reliability of the memory.

The schematic of SOS design is depicted in Fig. 3 (a) and the process of assigning preferred SA to each sub-bank is

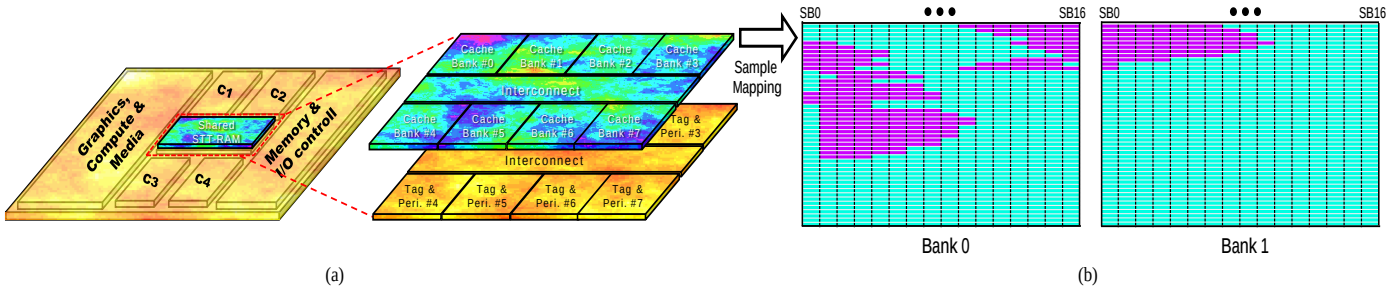

Fig. 2. (a) PV map of a 4-core CMP die, (b) Determining the preferred SA circuit based on post-fabrication sub-bank resiliency assessment to PV.

shown in Algorithm 1. After POST process and determining the preferred SA for that particular sub-bank, a select input is used in the circuit called **MODE** to choose between the two SAs based on assigned bit set value as shown in Fig. 3. Since PCSA consists of fewer CMOS transistors, it offers enhanced performance in terms of sensing delay and Energy Delay Product (EDP) compared to SPCSA. In the branch containing the main MTJ in PCSA, we have four transistors namely MP0, MP1, MN0, and MN4 and in the branch that includes reference MTJ we have also four transistors MP2, MP3, MN1, and MN4 as depicted in Fig. 3 (c). However, the main MTJ branch in SPCSA consists of two transistors MP0 and MN4 and two transistors MP5 and MN4 in the reference MTJ branch which makes it less vulnerable to PV, as shown in Fig. 3 (b). This redesign of the SA introduces an elevated sense margin which in turn results in decreased Bit Error Rate (BER). Nonetheless, the reduced BER comes with the cost of utilizing greater number of transistors in SPCSA design which incurs higher EDP.

The **MODE** signal controls the operation mode of the circuit to either operate in PCSA mode or SPCSA mode. If the input **MODE** is asserted then the circuit will operate in PCSA mode. On the other hand, if **MODE** is de-asserted will change the operation of the circuit to SPCSA mode. In order to further reduce the PV effect on the reference cell, we use the configuration shown with red dotted region in Fig. 3 (b) and (c) for MTJ0 which consists of (MTJ_P+MTJ_{AP})||(MTJ_P+MTJ_{AP}) that will result in an ideal reference cell in terms of resistance which is (MTJ_P+MTJ_{AP})/2 and in terms of process variation immunity [18]. The transition waveforms of the output of all the designs are provided in Fig. 4 in which the two operations of the proposed SOS design are shown.

Algorithm 1: SOS Approach to Assign Preferred SA to Sub-bank

```
   Function SOS() /*SOS Approach for SA Assignment*/
1  for ∀ cache line ∈ LLC do
2      for ∀ sub − bank ∈ cache line do
           begin
3              POST() /*Power-On Self-Test*/
4              Analyzer() /*Evaluate the correctness of the outputs*/
   Function POST() /*Power-On Self-Test*/
   begin
5      set SEN = 1 /*start the sensing state*/
6      if output != expected-value then
7          ++number-wrong-outputs /*increase number of wrong
           outputs*/
8      set SEN = 0 /*keep the sense signal in pre-charge state*/
   Function Analyzer() /*Evaluate the correctness of the outputs*/
   begin
9      if number-wrong-outputs > threshold then
10         set MODE = 0 /*assign SPCSA to sub-bank*/
           /*MUX takes sensed data from SPCSA to output*/
       else
11         set MODE = 1 /*assign PCSA to sub-bank*/
           /*MUX takes sensed data from PCSA to output*/
```

B. Distribution of Bit Errors in a Sub-banks

If we assume that the sensing operation of a bit follows the binomial distribution, the probability distribution of exact number of incorrectly sensed k bits in a sub-bank can be calculated by the probability mass function, pmf. Herein, we incorporate pmf into Sub-Bank Bit Error Rate (*SBER*) which can be calculated as following:

$$SBER(k) = \binom{SB}{k}(BER)^k(1-BER)^{SB-k}, k = 0, ..., SB \quad (1)$$

where SB is the number of bits in a sub-bank, k is number of incorrectly sensed bits, and BER is the probability that a bit is sensed incorrectly. However, since SOS considers the total number of incorrectly sensed bits in a sub-bank to determine which type of SAs array must be assigned to that particular sub-bank, the cumulative distribution function, cdf, is considered for decision making as follows:

$$SBER(X \le k) = \sum_{i=0}^{k}\binom{SB}{i}(BER)^i(1-BER)^{SB-i}, i = 0, ..., SB \quad (2)$$

For example, if we assume that BER is 0.5 for each bit in sub-bank and the number of bits resided in each sub-bank is 32, we have $SBER(X \ge 16) = 0.56$ which means the probability of incorrectly sensing more than 16 bits in a sub-bank is 0.56. The calculated SBER for sub-banks which are equipped with different versions of SAs are listed in Table III and Table IV. This theoretical assessment can be leveraged to estimate the proportion of BER in a sub-bank prior to running workloads for practical examination.

C. Fault Models Associated with Sensed Data

Independent of alternative fault models that can impact the stored value in STT-MRAM cell, overlooking PV effects during SA design may result in the sensed data differs from actual stored logic value while the read operation is taking place. This work concentrates on the faults that are caused by

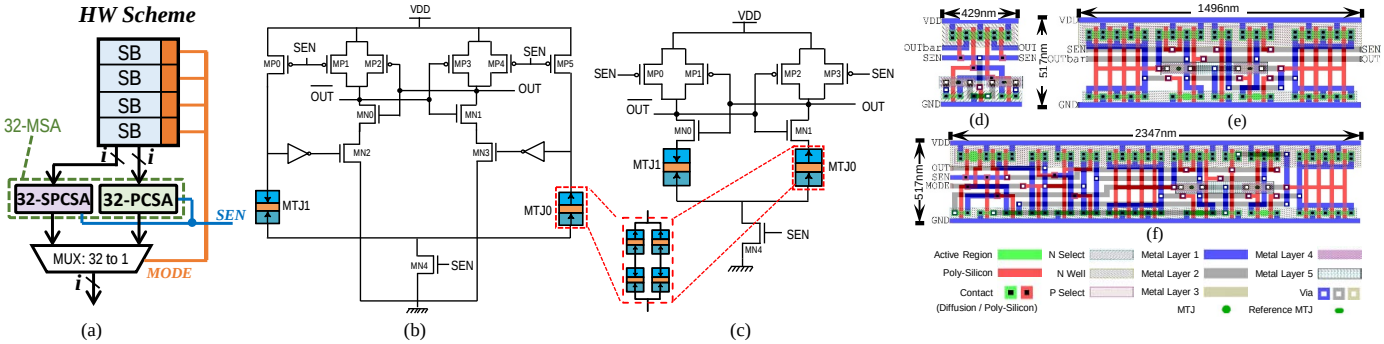

Fig. 3. (a) Proposed SOS, (b) SPCSA circuit (based on [7]), (c) PCSA circuit (based on [6]), (d) PCSA Layout, (e) SPCSA Layout, (f) MSA Layout.

incorrect sensed data. To be specific, we classify the outcomes of SA operation to the following categories for broad adaption:

- **True Data Sensing (TDS):** The sensed data value is identical to the value stored in the STT-MRAM cell.
- **False Data Sensing (FDS):** The sensed data value differs from the value stored in the STT-MRAM cell. FDS can be further classified to vulnerable FDS (VFDS) and non-vulnerable FDS (NVFDS).
  - **Vulnerable FDS (VFDS):** The sensed false data propagates out of cache, either consumed by the process or committed to other levels of memory [5].
  - **Non-Vulnerable FDS (NVFDS):** The replica copy of the sensed false data in the upper levels of cache will be overwritten by a write operation prior to being consumed. During a block eviction, replica data becomes written back to the lower levels of cache because it is a dirty victim block. Thus, this benign fault does not threaten the semantic correctness.

IV. Experimental Results

To comprehensively evaluate SOS efficacy, we analyze the SOS on both circuit- and architectural-level simulators. Experimental results are presented in Section IV-A and IV-B whereby the evaluation parameters are listed in Table I.

A. Circuit-Level Simulation Results

Simulation results have been extracted using HSPICE based on the 22nm Predictive Technology Model (PTM) to calculate the power and performance of a 1-bit PCSA and SPCSA. The design parameters and PV values are listed in Table I. Every design has been analyzed in an ideal case without PV, as well as Monte Carlo simulation [19] in the presence of PV. The results for the analysis of ideal case are listed in Table II.

Furthermore, 10,000 Monte Carlo simulations were performed considering different standard deviations for CMOS transistors' threshold voltage (V_{th}) and also MTJ's MgO thickness, shape, and area in order to cover the range of cases that may occur in the fabricated device. In particular, variation of 1% and 10% for the MTJs' resistance is assessed via Monte Carlo simulation. Based on the results listed in Table II, it can be concluded that MSA operating in PCSA mode, outperforms MSA operating in SPCSA mode, however, it suffers more from PV. On the contrary, MSA operating in SPCSA mode offers improved performance in terms of reliability and PV immunity

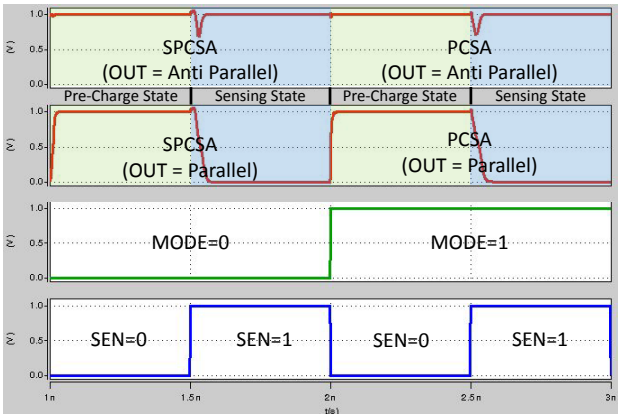

Fig. 4. Transition waveforms of PCSA and SPCSA.

compared to MSA operating in PCSA mode due to its reduced BER.

Based on the results listed in Table II, Table III, and Table IV, it can be concluded that MSA operating in PCSA mode attains 6-fold improvement over MSA operating in SPCSA mode on average in terms of Energy Delay Product (EDP). This is due to an improvement of 2.43μW and 8.7ps on average offered in PCSA. On the contrary, MSA operating in SPCSA mode increases the relibility by having 6% reduced BER considering TMR=100% on average due to PV, compared to MSA operating in PCSA mode.

Furthermore, it is observed that by optimizing the reference MTJ and using (MTJ$_P$+MTJ$_{AP}$)||(MTJ$_P$+MTJ$_{AP}$) configuration, the BER can be reduced by 15% on average (for TMR=100%). In addition, based on the results of Monte Carlo Simulation, it is clear that larger MTJ resistance, reduces the impact of variation on sensing output.

B. Architecture-Level Simulation Results

The latency and energy usage associated with read and write operations for SRAM and conventional SA cache accesses are provided by NVSim. However, we integrate the obtained results from Section IV-A for 1-bit PCSA/SPCSA into NVSim to extract the power and performance parameters for the cache accesses in SOS design. PARSEC 2.1 benchmarks suite executed on modified MARSSx86 which supports asymmetric cache read and write from distinct cache banks to extract the evaluation parameters of different cache designs during

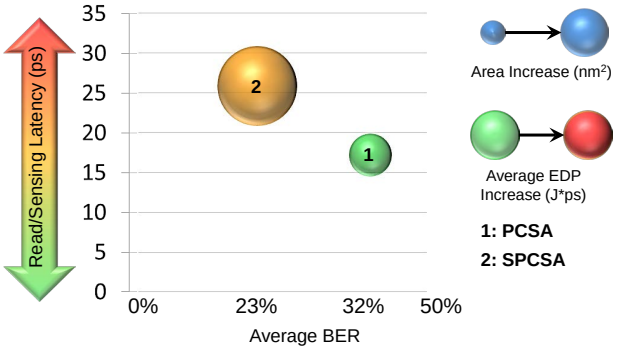

Fig. 5. PCSA and SPCSA design space for TMR=100%.

TABLE I
EVALUATION PARAMETERS

Architectural Parameters

chip	4-core CMP
core	3.3GHz, Fetch/ Exec/ Commit width 4
L1	private, 32 KB, I/D separate, 8-way, 64 B, SRAM, WB
L2	shared, 4 MB, 8 banks, 8-way, 64 B, STT-MRAM, WB
memory	8 GB, 1 channel, 4 ranks/ channel, 8 bank/ rank

4MB L2 cache bank configuration (32nm, temperature=350K)

L2 Cache Technology	RL/WL ($cycles$)	RE (nJ)	WE (nJ)	LP (mW)
SRAM	7.43/5.78	0.161	0.156	295.58
STT-MRAM	9.08/25.58	0.216	0.839	18.39
SOS	9.08/25.58	PCSA=0.208 SPCSA=0.218	0.839	18.39

RL: Read Latency, WL: Write Latency, RE: Read Energy, WE: Write Energy, LP: Leakage Power

Technology Parameters

Tech node	22nm
$pMOS$	$\mu(V_{th})$=460mV, $\sigma(V_{th})$=50mV (10%) $width(=2\times Length)$=44nm, $\sigma(width)$=0.44nm (1%)
$nMOS$	$\mu(V_{th})$=500mV, $\sigma(V_{th})$=50mV (10%) $width(=Length)$=22nm, $\sigma(width)$=0.22nm (1%)
MTJ	*The effects of variation are applied to TMR* MgO Thickness=0.85nm Shape Area(main MTJ)=(π/4)×40×40nm^2 Reference MTJ: Shape Area(MTJ$_{AP}$)=(π/4)×30×30nm^2 Shape Area((MTJ$_P$+MTJ$_{AP}$)$\|$(MTJ$_P$+MTJ$_{AP}$))=(π/4)×40×40nm^2 R.A(Resistance×Area)=5Ω.μm^2 TMR=100%, $\sigma(TMR)$=1% & 10% α(Damping Factor)=0.01 Nominal Voltage=1.0V, SEN Signal Period (T)=1ns

program execution. We model a Chip Multi-Processor (CMP) with four single-threaded x86 cores. Each core consists of private L1 cache, and shared LLC among all the cores. Eleven workloads are executed for 500 million instructions starting at the Region Of Interest (ROI) after warming up the cache for 5 million instructions. The `simsmall` input sets are used for all PARSEC workloads.

1) Energy Usage Comparison: In order to evaluate the energy benefit of SOS, we compare the energy breakdown of SOS with SRAM-based LLC, and LLC with conventional SA. Based on the extracted results from NVSim which are listed in Table I, SOS neutralizes the high energy consumption of

TABLE II
SIMULATION RESULTS FOR IDEAL STATE (MTJ$_{Ref}$=5.7KΩ)

Design	Area (Device Count)			Anti-Parallel (6.4KΩ)			Parallel (3.2KΩ)		
	PMOS Trans.	NMOS Trans.	MTJ	Delay (ps)	Power (μW)	EDP (J*ps)	Delay (ps)	Power (μW)	EDP (J*ps)
PCSA	4	3	2	20.8	0.79	16.43	13.5	0.76	10.24
SPCSA	8	5	2	28.8	3.21	92.45	22.9	3.21	73.51

TABLE III
MONTE CARLO SIMULATION 10,000 RUN RESULTS
(MTJ$_{Ref}$=5.7KΩ, MTJ$_P$=3.2KΩ, AND MTJ$_{AP}$=6.4KΩ FOR TMR=100%)

Design	Variation	BER (%) for TMR=						SBER($X \geq 16$)(%)	
	10% in V_{th}	100%	150%	200%	250%	300%	350%	100%	150%
PCSA	**1%** in TMR	38.29	17.15	5.89	1.65	0.30	0.03	11.96	0.002
SPCSA	**1%** in TMR	34.04	9.41	1.35	0.09	0.01	0.00	4.54	<1E-6
PCSA	**10%** in TMR	38.44	17.18	6.06	1.62	0.34	0.04	12.32	0.002
SPCSA	**10%** in TMR	34.32	10.00	1.44	0.13	0.02	0.00	4.88	<1E-6

SPCSA via low-power PCSA during read operation. The effect of this compensation has been shown in Fig. 6 whereby the dynamic energy of SOS technique and the design that benefit exclusive conventional SA is approximately even across all benchmarks suite.

The high write energy overhead for storing a value into STT-MRAM cell incurs significant energy overhead in both SOS and STT-MRAM based LLC with conventional SA designs while the SRAM-based LLC design benefits from symmetric acceptable energy consumption for both read and write operations. This incident is conspicuous for write-intensive workloads such as **`facesim`**, **`ferret`**, and **`vips`** where the ratio of write accesses to the LLC is significantly more than read accesses. Although SRAM exhibits lower dynamic energy consumption, its high leakage power has exacerbated the overall consumed energy compared to two other designs as shown in Fig. 7. Both SOS and conventional SA designs can conserve 88.38% on average of the total consumed energy.

2) Empirical Fault Model Analysis: Fig. 8 illustrates the comparison of distribution of sensed data between LLC equipped with conventional SA and SOS circuit strategy. We assume that the PV map for each cache bank is similar to the floorplan of STT-MRAM layer, shown in Fig. 2. We apply the PV ratio of each accessed sub-bank during fault analysis for each workload. For example, if a sub-bank experiences a high amount of PV, it is highly likely that the data will be sensed incorrectly. Our experimental results indicate that the PV effect may incur around 27.5% of the sensed data to be read incorrectly from which 21.5% are extremely vulnerable which implies that around one fifth of the overall sensing operations have the potential to contaminate the application's data structure. If this rate of sensed data are not accommodated properly, it may induce application crashes or prolong the program execution. Across all benchmarks suite, the calculated VFDS for some benchmarks is more than others. For example, in **`blackscholes`** and **`canneal`** workloads, the proportion of read operations and dirty victim blocks residing in LLC are more than write operations which results in the increased VFDS. As another example, the **`streamcluster`** workload is a read-intensive application in which more than 85% of

TABLE IV
MONTE CARLO SIMULATION 10,000 RUN RESULTS
(MTJ_{Ref}=4.8KΩ, MTJ_P=3.2KΩ, AND MTJ_{AP}=6.4KΩ FOR TMR=100%)

Design	Variation	BER (%) for TMR=						SBER($X \geq 16$)(%)	
	10% in V_{th}	100%	150%	200%	250%	300%	350%	100%	150%
PCSA	1% in TMR	24.87	9.01	2.71	0.54	0.05	0.00	0.18	<1E-6
SPCSA	1% in TMR	17.68	3.41	0.32	0.02	0.00	0.00	0.003	<1E-6
PCSA	10% in TMR	24.90	9.31	2.69	0.59	0.07	0.00	0.19	<1E-6
SPCSA	10% in TMR	17.78	3.58	0.35	0.02	0.00	0.00	0.003	<1E-6

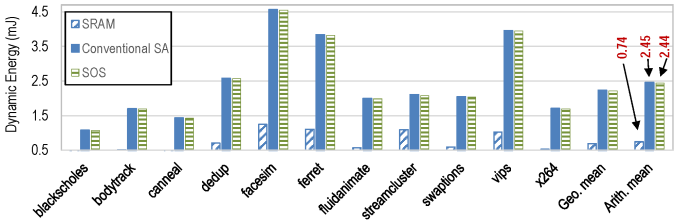

Fig. 6. LLC dynamic energy comparison for SRAM, conventional SA, and SOS.

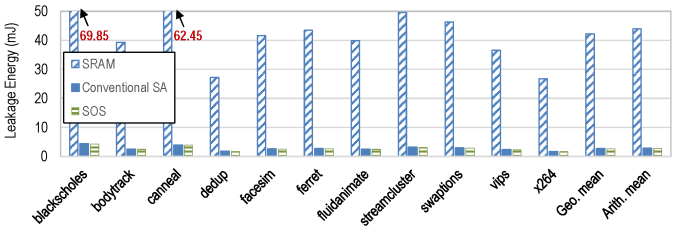

Fig. 7. LLC leakage energy comparison for SRAM, conventional SA, and SOS.

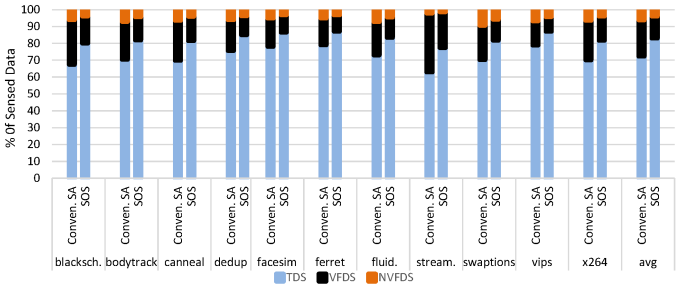

Fig. 8. Distribution of sensed data. SOS is equipped with MTJ_{Ref}=4.8KΩ, TMR=150%, and 10% variation in TMR.

memory operations are read accesses which increase the chance for enduring higher VFDS.

On the other hand, SOS addresses the probability of sensing incorrect data through leveraging PV-resilient SAs array (SPCSA) in the sub-bank architecture whenever the sub-bank's PV ratio is more than a predefined threshold. Namely, the VFDS in the SOS design is reduced by 40% on average compared to LLC with conventional SA, thus improving the mean TDS from 72.5% to 83.2% across all workloads.

V. Conclusion

In conclusion, SOS is a circuit-architecture cross-layer solution which combats the common PV problem in the emerging NVM technologies by engaging PV-resilient SAs array offering acceptable resistive sensing margin. In addition, SOS manages to meet the constrain power budget in IoT devices through low-power SAs in sub-banks that experience lower rates of PV. Furthermore, we classify the output of the sensed data based on its impact on the execution flow of the workload. This classification of experimental outcomes is vital to identify the efficiency of SOS to accommodate critical read operations. Our experimental results indicate that the energy consumption of SOS is as high as LLC with conventional SAs, while SOS reduces the overall VFDS significantly. The confluence of these factors in turn significantly increase the reliability of realistic program execution.

References

[1] M. Imani, Y. Kim, and T. Rosing, "Mpim: Multi-purpose in-memory processing using configurable resistive memory," in *International Symposium on High-Performance Computer Architecture (HPCA)*, 2017.

[2] Z. Sun, X. Bi, and H. Li, "Process variation aware data management for stt-ram cache design," in *ISLPED*. ACM, 2012, pp. 179–184.

[3] E. Eken and et al., "A Novel Self-Reference Technique for STT-RAM Read and Write Reliability Enhancement," *IEEE Transactions on Magnetics*, vol. 50, no. 11, pp. 1–4, 2014.

[4] Y. Zhang and et al., "Adams: asymmetric differential stt-ram cell structure for reliable and high-performance applications," in *ICCAD*, 2013, pp. 9–16.

[5] N. Khoshavi, X. Chen, J. Wang, and R. F. DeMara, "Bit-upset vulnerability factor for edram last level cache immunity analysis," in *2016 17th International Symposium on Quality Electronic Design (ISQED)*. IEEE, 2016, pp. 6–11.

[6] W. Kang and et al., "Separated precharge sensing amplifier for deep submicrometer mtj/cmos hybrid logic circuits," *IEEE Transactions on Magnetics*, vol. 50, no. 6, pp. 1–5, 2014.

[7] W. Zhao and et al., "High speed, high stability and low power sensing amplifier for mtj/cmos hybrid logic circuits," *IEEE Transactions on Magnetics*, vol. 45, no. 10, pp. 3784–3787, 2009.

[8] X. Chen, N. Khoshavi, R. F. DeMara, J. Wang, D. Huang, W. Wen, and Y. Chen, "Energy-aware adaptive restore schemes for mlc stt-ram cache," *IEEE Transactions on Computers*, 2016.

[9] M. Imani, S. Patil, and T. Rosing, "Low power data-aware stt-ram based hybrid cache architecture," in *2016 17th International Symposium on Quality Electronic Design (ISQED)*. IEEE, 2016, pp. 88–94.

[10] N. Khoshavi, X. Chen, J. Wang, and R. F. DeMara, "Read-tuned stt-ram and edram cache hierarchies for throughput and energy enhancement," *arXiv preprint arXiv:1607.08086*, 2016.

[11] P. Friedberg and et al., "Modeling within-die spatial correlation effects for process-design co-optimization." in *ISQED*, 2005, pp. 516–521.

[12] B. Zhao and et al., "Process variation-aware nonuniform cache management in a 3d die-stacked multicore processor," *IEEE Transactions on Computers*, vol. 62, no. 11, pp. 2252–2265, Nov 2013.

[13] S. Borkar, T. Karnik, and V. De, "Design and reliability challenges in nanometer technologies," in *Proceedings of the 41st annual Design Automation Conference*, 2004, pp. 75–75.

[14] S. R. Sarangi and et al., "Varius: A model of process variation and resulting timing errors for microarchitects," *IEEE Transactions on Semiconductor Manufacturing*, vol. 21, no. 1, pp. 3–13, 2008.

[15] X. Liang, R. Canal, G.-Y. Wei, and D. Brooks, "Process variation tolerant 3t1d-based cache architectures," in *Proceedings of the 40th Annual IEEE/ACM International Symposium on Microarchitecture*. IEEE Computer Society, 2007, pp. 15–26.

[16] R. Teodorescu and J. Torrellas, "Variation-aware application scheduling and power management for chip multiprocessors," in *ACM SIGARCH Computer Architecture News*, vol. 36, no. 3, 2008, pp. 363–374.

[17] D. Cheng, H. Hsiung, B. Liu, J. Chen, J. Zeng, R. Govindan, and S. K. Gupta, "A new march test for process-variation induced delay faults in srams," in *2013 22nd Asian Test Symposium*. IEEE, 2013, pp. 115–122.

[18] W. Kang and et al., "A dynamic reference scheme to improve the sensing reliability of magnetic random access memory," in *ICSICT*. IEEE, 2014, pp. 1–3.

[19] A. Rastegari and M. Mobin, "Maintenance decision making, supported by computerized maintenance management system," in *2016 Annual Reliability and Maintainability Symposium (RAMS)*. IEEE, 2016, pp. 1–8.