Soft Error Effect Tolerant Temporal Self-Voting Checkers: Energy vs. Resilience Tradeoffs

Faris S. Alghareb, Mingjie Lin, Ronald F. DeMara
Department of Electrical Eng. and Computer Science, University of Central Florida, Orlando, FL 32816, USA

Abstract

Achieving high reliability against transient faults poses significant challenges due to the trends of technology and voltage scaling. Thus, numerous soft error mitigation techniques have been proposed for masking *Soft Error Rate (SER)* in logic circuits. However, most soft error suppression approaches have significant overheads in terms of area, power consumption, and speed performance degradation. Herein, we propose two circuit-level techniques, namely *Temporal Self-Voting Logic (TSVL)* and *Hybrid Spatial and Temporal Redundancy Double-Error Correction (HSTR-DEC)*, to prevent the effects of soft errors in logic circuits, occurring due to *Single Event Upset (SEU)* or *Single Event Transient (SET)*. TSVL and HSTR-DEC circuits can be utilized to improve the reliability of a logic path with minimal impact on circuit delay while achieving a complete and cost-effective SEU handling as compared to traditional spatial or temporal redundancy approach. The primary contribution of the TSVL approach is that it eliminates error masking from the critical datapath, thus, area and energy overheads are significantly reduced. A transient gate-level fault injection and analysis is used to evaluate the capability of soft errors suppression of the proposed hardening approach. Experimental results indicate that TSVL can cover soft errors, on average, roughly by 99% while realizing an amelioration of 22.02% and 2.15% for area and speed degradation as compared to the previous Self-Voting DMR approach. Meanwhile, HSTR-DEC approach realizes a complete coverage for single and double SEUs while incurring comparable area and delay overheads as compared to the prior hybrid redundancy approach.

Keywords

Fault tolerance, Soft Error Rate (SER), Single Event Transient (SET), Single Event Upset (SEU), reliability.

I. Introduction

Radiation induced-soft errors have become a key issue as they cause malfunctions in CMOS circuits and systems, therefore, the reliability of contemporary processors have negatively impacted even for terrestrial applications. Similarly, operation at higher clock rate has also increased the probability of SETs to be captured by a latch/flip-flop. Additionally, designing systems that are tolerant to soft errors is becoming increasingly significant due to the combined impact of technology scaling and reduction in supply voltage as they reduce the required energy to induce momentary glitches at the susceptible nodes of CMOS circuits [1]. In the literature, several SER suppression schemes have been proposed at multiple levels of design abstraction. They can be categorized into four taxonomies including: device-level, gate-level, circuit/module-level, and system-level. Each level exploits some design property to harden the design against soft error effects. Device-level techniques concentrate on reducing the collected charge at a struck node, whereas gate-level techniques focus on increasing the amount of critical charge, Q_{crit}. The former requires a modification for the existing fabrication process to improve the layout design, i.e., *Silicon-on-Insulator (SOI)*, guard ring (for P-hit mitigation) and guard drain (for N-hit mitigation) [2], and high-density well contacts [3], whereas the latter requires to increase the charge/discharge capacitance by resizing the critical node(s). The functioning of these techniques is based on avoiding the occurrence of transient and upset glitches, *fault avoidance techniques* [4]. However, as moving towards the scaling of the technology process, utilizing more robust fabrication processes adds more complexity and increases the production cost [5]. Furthermore, it is costly and quite difficult to resize each sensitive individual node in designs that consist of over 1 billion transistors, thus some redundancy considerations, at higher level of abstraction are required. At the circuit/module-level, soft error resilience can be obtained by applying three techniques: spatial redundancy approaches such as *Triple Module Redundancy (TMR)*, temporal redundancy approaches such as clock shadow latches, and self-voting redundant system strategies (combining the spatial and temporal redundancy approaches). They are utilized for designing dependable systems so that high reliability and availability are realized while directly countering desirable attributes such as, high speed, low power, and minimal layout area. However, adding extra logic to harden a design against soft error effects increases the number of susceptible nodes, leading towards the degradation of the system's overall performance. Hence, the challenge is not how to realize a high reliability, however, achieving it with minimal area and energy overheads and speed degradation is the aim.

Finally, *Error Correcting Codes (ECC)* and parity that are utilized for memory protection are the predominant schemes at the system-level. However, they require extra bits of information to be stored with the data in order to rollback the error-free data in the event of an upset. Both module- and system-level techniques are considered as *fault correction techniques* [4]. Herein, we have developed two circuit-level logic techniques for soft error mitigation that significantly reduce the rate of SEU due to radiation strike, while incurring lower area and energy overheads.

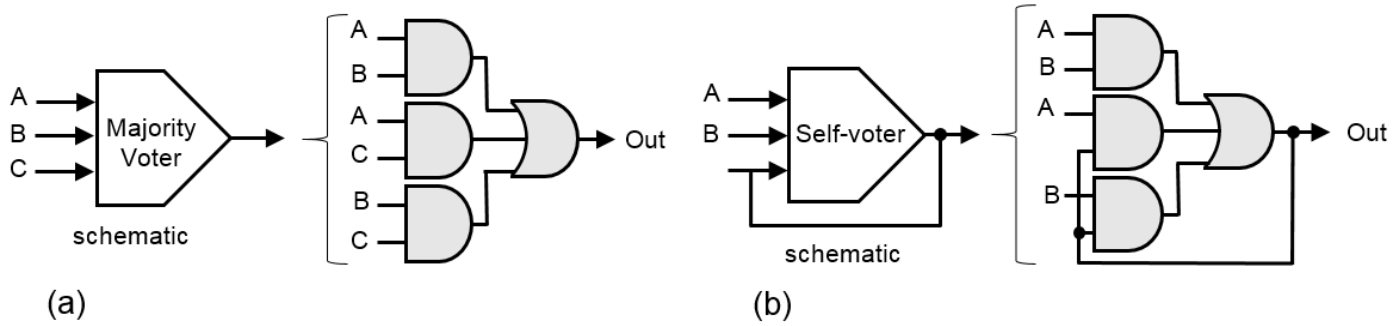

Fig. 1: Voting Circuits: (a) Majority voter (b) Self-voter [10].

Recently, CMOS technologies have been deeply-scaled, thereby a single particle strike that hits a sensitive node can affect more than a single storage element at a given instance of time [6]. This implies that the probability of double or even multiple errors occurring simultaneously has become high. Thus, soft error in flip-flops has become a concern due to the effect of charge sharing between the adjacent nodes [6]. Additionally, circuit-level mitigation techniques introduce reduced benefits under technology scaling. For instance, in [7] it is predicted that, as the spacing between the sensitive nodes is reduced, the vulnerability of hardened flip-flops increases. Therefore, optimized solutions which offer multiple error correction while minimizing performance degradation and energy overhead, imposed by the extra logic for protection, are sought. The prime advantage of our approaches is that they are effective in filtering transient and upset glitches while incurring minimal area, power, and delay penalties as compared to the prior redundancy approaches. We assess the relative performance of the proposed techniques and compare them against temporal, spatial, and self-voting DMR alternatives using 15nm based NanGate open source library. Note that the scope of this work is fault detection and correction, i.e., spatial and temporal redundancy approaches, rather than fault avoidance techniques, i.e., device-level schemes. The remainder of the paper is organized as follows: Section II discusses SER mitigation techniques where continued technology and supply voltage scaling impact terrestrial applications. Section III discusses the proposed approaches, whereas the simulation results are analyzed in Section IV. Section V concludes this work.

II. Redundancy-Based SER Masking Techniques

Soft error handling approaches that use spatial and temporal redundancy typically incur significant overheads in terms of area, power, and delay. In addition, adding extra logic redundancy increases the design area that can be struck by radiation particles, thus increasing the probability of vulnerable nodes [4]; therefore, the challenge is to implement them with minimal penalties. Practically, SET hardening strategies can be categorized into three aspects including: at the point of SET origin (SET generation), along the datapath (SET propagation), and within the latch (SET capturing) [5], [8]. Schemes which tackle soft error at SET's origin concentrate on limiting the collected charge at the sensitive node of the transistor. Limiting the collected charge diminishes SET pulse width and reduces SET voltage amplitude [8]. Meanwhile, device resizing [9] for current drive is an obvious SET mitigation technique. Additionally, one of the most effective techniques for hardening SETs resides inside the latch. It leverages the property that not all SET pulses will arrive at the setup/hold time of a flip-flop, thus transient pulses which do not overlap with the window of vulnerability of a storage element will not cause an upset [8]. Such techniques that are designed based on neglecting the irrelevant SET, i.e., not captured, are profitable concepts and they have been adopted to reduce the overheads of spatial approaches, i.e., TMR.

Most of the redundancy techniques are based on voting mechanisms. Figure 1(a) shows a conventional 3-input majority voter circuit, where the output changes state when two out of three inputs change [10]. A transient pulse on any input will be rejected by the voter as long as the other two inputs are correct. An SET striking inside of the voter can cause a momentary glitch on the output, but it will not cause a permanent SEU. Figure 1(b) shows a circuit implementation of a self-voter which is a 3-input majority voter that is configured to vote on two external inputs and the feedback from the output. The output of a self-voter changes state to 1 logic when both its inputs are high, and becomes 0 logic when both its inputs are low. When the two external inputs mismatch, output remains unchanged and thus prevents an SET from being propagated to the next stage [10]. Thus, self-voter circuit is a state-holding element which behaves as a redundant copy of a latch or a flip-flop. Spatial redundancy is often employed in mission-critical applications to ensure system operation even in unforseen circumstances, such as autonomous vehicles, satellites, and deep space systems [11]–[13]. This is because TMR provides 100% fault masking coverage for faults in single module simultaneously, compared to the simplex arrangement (unprotected design). However, its major drawback is that it significantly incurs roughly 2-fold area and energy overheads [14]. This issue limits the usage of spatial techniques in applications with tight energy budget. Additionally, recent studies have reported that spatial redundancy techniques might increase the susceptibility of SER due to increased area which leads to larger sensitive nodes [3], [4]. On the other hand, in temporal redundancy approach data for the same combinational logic can be sampled at three distinct instances to construct a voting arrangement while using a simplex instance of the datapath [15]. A majority voter is used to determine the final output, so that when a soft error occurs in the combinational logic it will be stored in one of the flip-flops, and it should be rejected by the voter. However, its drawback is that it highly impacts the speed of a design and degrades the system performance. An approach that combines spatial and temporal redundancy for soft errors mitigation is presented in [10]. As can be seen in Figure 2,

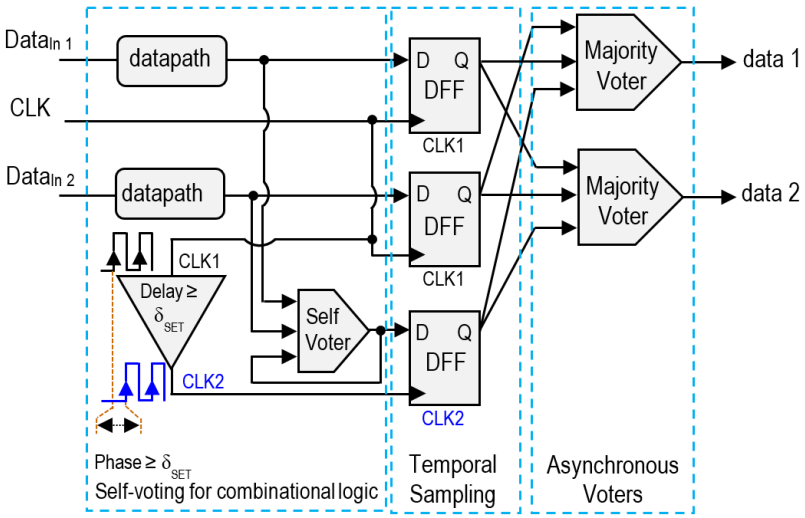

Fig. 2: Self-Voting DMR logic approach [10].

this approach duplicates the combinational logic and votes using self-voter circuit and triplicates the sequential logic part and determines the final output via a majority voter circuit. Similar to a majority voter, an SET striking inside of the self-voter circuit results in a momentary glitch on the voter output, but it will not cause a permanent upset [10]. Thus, Teifel and *et al.* [10] use two self-voter circuits in the output to achieve a complete fault-tolerance coverage. However, its drawback is that it still consumes large amount of area and power, therefore, more efficient schemes that impose less area-energy overhead or tolerate MBUs simultaneously are sought.

III. The Proposed Approaches

Herein, we introduce two novel efficient and cost-effective techniques to harden the critical logic datapaths against soft error effects. The proposed approaches concentrate on protecting the sequential logic elements, i.e., flip-flops or latches, from an upset while achieving significant area and power saving.

A. Temporal Self-Voting Logic (TSVL) Approach

In conventional *Dual Module Redundancy (DMR)* approach, the outputs of two identical modules are compared, and an error is detected where there is a discrepancy between them. Conventional DMR scheme is used to detect when a soft error occurs, without error correction, since voting cannot determine which of the two modules is error-free [16]. However, the proposed scheme, TSVL, can be utilized to detect and correct any upset in a flip-flop while incurring acceptable area, power, and performance penalties. As can be seen in Figure 3, the design is capable to detect and correct any SEU that hits one of the flip-flops or an SET that generates, propagates, and eventually is captured by one of the flip-flops. Herein, there are three possible scenarios in which an upset will occur. The first scenario is when an SET hits the combinational logic preceding the flip-flops and then propagates and arrives at the setup/hold time of the first/original flip-flop, overlapping with window of vulnerability. This will upset the original flip-flop, while the redundant flip-flop is error-free as long as it is triggered by a clock delayed by a phase shift greater than the width of the transient pulse. Thus, the comparator (XOR-gate) will assert the $Error_{SEU}$ signal to indicate the occurrence of an upset, making the self-voter circuit determines the final output.

Hence, the third input of the self-voter is fed from a MUX that receives its first input directly from the datapath and the second input from the feedback of self-voter circuit; an SEU will be masked by the self-voter circuit regardless of whether it occurs in the original or in the redundant flip-flop. This is because the third input of the self-voter determines the output when the external two inputs mismatch. Since the third input of self-voter circuit relies on the output of the first MUX that drives its output based on the delayed clock rate (CLK2), the self-voter's third input will be switched alternately between the direct combinaltionl datapath, with the rising edge, and the feedback of self-voter circuit, with the falling edge. Thus, when an SET hits the combinational logic and is then captured by one of the flip-flops, its duration is significant. If it will have passed by the time that the first input's rising edge arrives to the first MUX, then it will be ignored as long as the delay of CLK2 is larger than the generated SET. Therefore, the correct data will pass as the self-voter's third input with the rising edge. The purpose for using a MUX circuit at the input of self-voter is to update the previous state of the self-voter circuit with the rising edge of the delayed clock (CLK2). Figure 4 depicts the validity of the proposed scheme, as two individual upsets occur in the original and redundant flip-flop, get corrected, and legitimate data is passed to the final output.

As a result, irrespective of whether the upset occurs in the original or redundant flip-flop, the final output is always correct as long as the third input of self-voter circuit alters based on CLK2. The second scenario is when an SET hits inside a flip-flop, an error (SEU) will be observed, and it will be masked in the same way as stated above. The last scenario is when the first

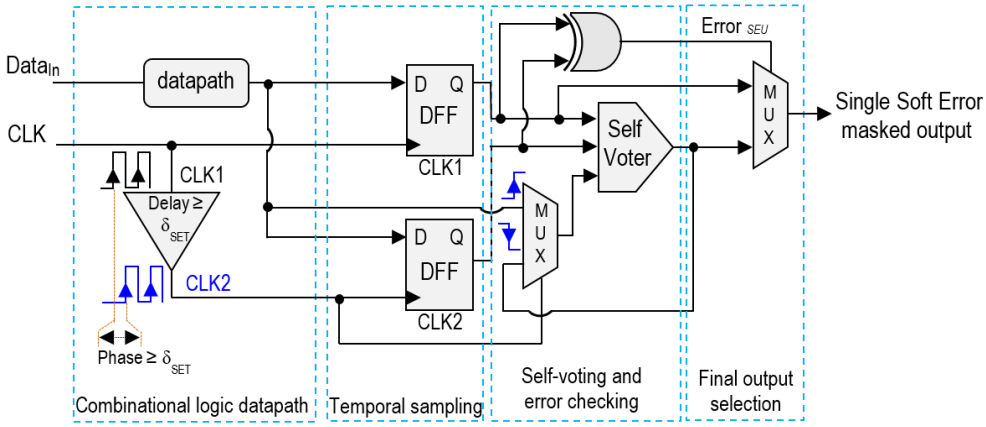

Fig. 3: Temporal Self-Voting Logic (TSVL) approach.

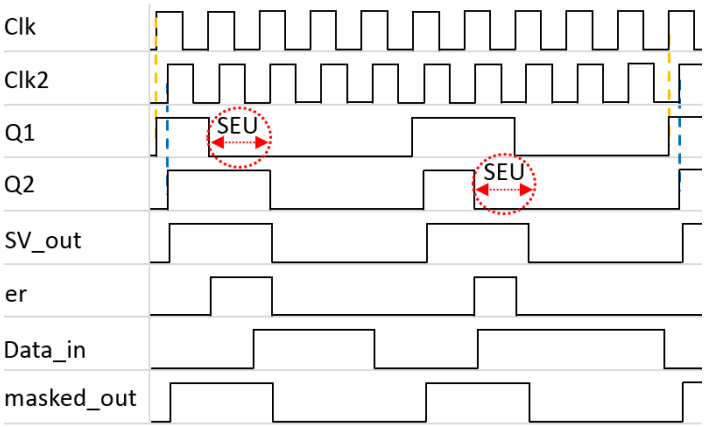

Fig. 4: Timing diagram of TSVL approach with SEU recovery occurred in the original, $Q1$, and redundant, $Q2$, flip-flop consecutively, `masked_out` is an inverse of `data_in`.

MUX or the XOR-gate is hit by a transient pulse, in this case the final output is not effected as long as the output of both flip-flops are correct; therefore, any one of them can be selected as the final output. However, an SET that hits the second MUX circuit, that determines the final output, will cause a momentary glitch in the final output, as in the majority voter of a TMR. Note that signal CLK2 is generated by buffering the main clock to add phase delay greater than the SET pulse width, which is a popular practice in the design of reliable circuits. The main difference between the proposed approach and the Self-Voting DMR approach presented in [10] is that TSVL functions are based on a simplex combinational datapath and double flip-flops, whereas Self-Voting DMR uses DMR for the combinational logic portion and TMR for the sequential logic portion, thus TSVL achieves significant reduction in area and power penalties as compared to the Self-Voting DMR approach; this will be discussed in Section IV.

As compared to spatial and temporal redundancy approach flip-flop based designs, TSVL provides a performance compromise between TMR and temporal redundancy approaches. The proposed scheme (TSVL) consumes less area (by two redundant logic modules) than TMR and provides higher performance in term of speed than temporal redundancy (roughly half the speed degradation of the temporal redundancy scheme). Overall, the delay of TMR, temporal redundancy, Self-Voting DMR, and TSVL approach are given by:

$$\delta_{critical} = \max_{1 \le i \le n} (\delta_i) \tag{1}$$

$$\delta_{TMR} = \delta_{critical} + \delta_{voter} \tag{2}$$

$$\delta_{Temp} = \delta_{datapath} + \delta_{voter} + 2 * \delta_{SET} \tag{3}$$

$$\delta_{SVDMR} = \delta_{critical} + 2 * \delta_{voter} + \delta_{SET} \tag{4}$$

$$\delta_{TSVL} = \delta_{datapath} + \delta_{voter} + 2 * \delta_{Mux} + \delta_{SET} \tag{5}$$

Where $\delta_{critical}$, δ_{voter}, and δ_{SET} represent the critical path delay of the datapath logic, delay of the voting logic, and delay of the transient pulse width, respectively. $2 * \delta_{voter}$ is required in the self-votig DMR approach because the longest circuit path includes one majority voter and one self-voter, whereas $2 * \delta_{SET}$ is required in the temporal redundancy approach to ensure that the legitimate data is captured at the registers. On the other hand, if A_{logic} represents the required logic area of a design and

A_{comb}, A_{seq}, A_{voter}, A_{SVDMR}, and A_{TSVL} represent combinational logic, sequential logic, voter area, Self-Voting DMR area, and TSVL area, respectively, then the area overhead for the redundant designs are given by:

$$A_{logic} = A_{comb} + A_{seq} \tag{6}$$
$$A_{TMR} = 2 * A_{logic} + A_{voter} \tag{7}$$
$$A_{Temp} = 2 * A_{seq} + A_{voter} \tag{8}$$
$$A_{SVDMR} = A_{comb} + 2 * A_{seq} + 2 * A_{voter} \tag{9}$$
$$A_{TSVL} = A_{seq} + A_{voter} + 2 * A_{Mux} \tag{10}$$

Equation 2-5 consider the longest datapath delay. Thus, to meet the timing constraints of a radiation hardening technique, its main clock period must be greater than, or equal to, the longest logic datapath delay.

B. Hybrid Spatial and Temporal Redundancy Double-Error Correction Approach

In this section, we propose a new technique, namely Hybrid Spatial and Temporal Redundancy Double-Error Correction (HSTR-DEC), for soft error mitigation. As illustrated in Figure 5, the proposed approach utilizes DMR circuit for the combinational datapath with TMR for the sequential portion, i.e., flip-flops. The final output is determined by voting based on two masked outputs, nodes N1 and N2, and the masked output from the original and redundant datapaths. The proposed scheme significantly improves the error resilience as compared to previous traditional redundancy approaches due to its ability to tolerate double SEUs simultaneously, i.e., *Multi-bit Upsets (MBUs)* are tolerated. Moreover, HSTR-DEC approach can surpass not only the SEUs, but also can mask SETs that generate through datapath logic and are eventually captured by one of the flip-flops. Our approach has been motivated by the original technique proposed in [10], and the proposed changes have been designed by evaluating the limitations of error resilience, i.e., *Multi-Bit Upsets (MBUs)*, regarding area and delay overheads. Table I shows the possible scenarios of soft error (SEU) that HSTR-DEC approach can tolerate. In case a single SEU occurs, the proposed approach is able to mask an upset regardless in which register the error occurs. On the other hand, in case there are two SETs generated and propagated through the datapath at the same time, they might be captured by R1 and R3 only, whereas R2 will capture the legitimate data since it is triggered by a clock which is delayed by a phase shift greater than the generated transient pulse. There exist three possible scenarios for two SEUs to occur simultaneously. In case I, both register R1 and R2 are upset, therefore, the output of the first self-voter circuit, node N1, is incorrect while node N2 is correct due to the second self-voter votes based on R2, R3, and the redundant direct datapath during the rising edge of the clock. Thus, N2 is error-free as long as both R3 and the redundant datapath are correct. The same scenario, i.e., case III, occurs when both R2 and R3 get upset. In case II, register R1 and R3 get upset, meanwhile nodes N1 and N2 are correct. This is because both self-voter circuits vote based on R2, which is error-free, and the original and redundant datapaths which are also error-free as long as the width of SET is less than 200 psec. However, the proposed scheme is unable to recover when all the flip-flops, i.e., R1, R2, and R3, become upset at the same time. This indicates that the proposed scheme fails to recover only when the energetic particles strike inside the flip-flops and are adequately large to flip the bit state at all registers during the same clock period.

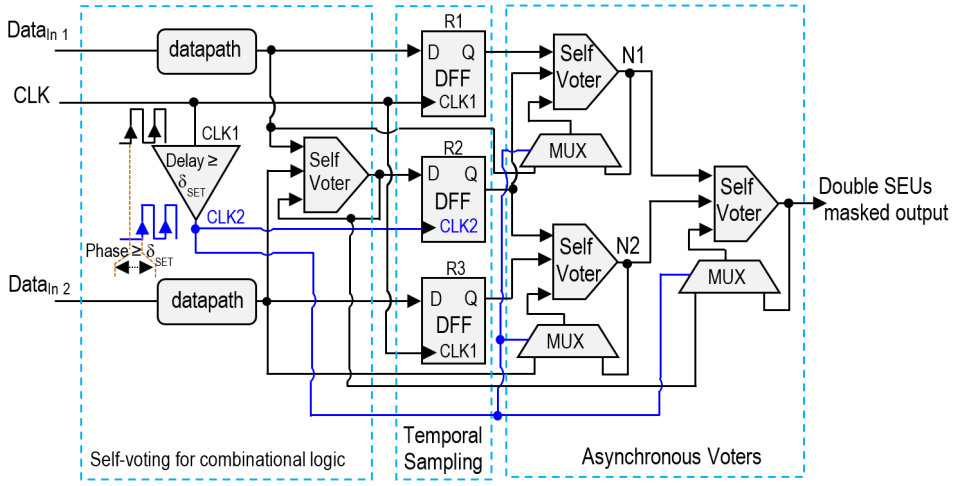

Fig. 5: Hybrid Spatial and Temporal Redundancy Double-Error Correction approach.

TABLE I: Possible error scenarios of HSTR-DEC approach.
(NE = No Error; UE = Upset Error)

♯ of SEUs	Case	R1	R2	R3	N1	N2	Masked Output
Single	I	UE	NE	NE	✓	✓	✓
	II	NE	UE	NE	✓	✓	✓
	III	NE	NE	UE	✓	✓	✓
Double	I	UE	UE	NE	UE	✓	✓
	II	UE	NE	UE	✓	✓	✓
	III	NE	UE	UE	✓	UE	✓

TABLE II: Fault coverage analysis of TSVL approach.

Benckmark Circuit	♯ of Cells	♯ of Injected Faults	♯ of Masked Faults	♯ of Unmasked Faults	Fault Coverage %	SV-DMR [10] FCPR	TSVL FCPR
$S27$	13	500	487	13	97.4	20.40	23.75
$S349$	127	4000	3883	117	97.075	3.51	4.35
$S444$	163	7000	6814	186	97.34	2.13	2.5
$S838$	418	7000	6798	202	97.11	1.73	2.21
$S1423$	683	7000	6779	221	96.84	0.68	0.804
$S9234$	1369	7000	6737	263	96.24	0.365	0.455

IV. Simulation Results and Reliability Analysis

Synopsys Design Compiler was used to synthesize the proposed approach using 15nm technology process. Since TSVL does not require any modifications or adoptions at the device-level, the standard cell libraries were used to implement the circuits. Thus, no complexity or additional fabrication cost will be associated with the proposed scheme under technology generations. Additionally, area and energy costs are minimized in the generation of the delayed clock signal (CLK2) by using buffers that introduce maximum delay with minimum power consumption and area usage. The ability of the proposed hardening approach to suppress soft errors, was tested by randomly injecting transient and upset faults at the gate-level design. As a case study, a set of ISCAS89 benchmark circuits, with a different combinational and sequential logic ratio, have been synthesized using *Synopsys Design Compiler* and validated with fault injection technique, presented in [17], where 7000 faults, both SET and SEU, were injected into the gate-level Verilog code describing the benchmark circuit constructed with the proposed approach. SEUs were injected into the input node of a flip-flop with the rising edge, whereas SETs were injected into a node of a logic gate, and they were injected at arbitrarily chosen locations and times. The fault coverage of the proposed approach is listed in Table II for a set of ISCAS89 benchmark circuits constructed with TSVL using 15nm technology process.

The analysis of simulation results indicates that TSVL is able to recover from soft errors by 100% of SEUs and 97% of SETs, thus, on average, it can roughly suppress 99% of soft errors. In addition, since SER mitigation techniques offer a tradeoff between the error resilience and overheads of protection techniques, we calculate a new metric called *Fault Coverage Power Ratio (FCPR)* by dividing the fault coverage by the power consumption, as the goal is to maximize the fault coverage and minimize the power consumption. Thus, the higher the value of FCPR, the better the design. As can be seen in the last two columns of Table II, TSVL realizes higher FCPR for all the selected benchmark circuits, regardless whether the combinational or the sequential logic ratio is higher. Also, TSVL achieves higher FCPR for the small circuits. Notice that the unmasked faults in the $S1423$ and $S9234$ are large because these benchmark circuits utilize large number of flip-flops, 74 and 228 respectively, thus the probability of an SET hitting the second Mux circuit is increased. Thus, the proposed approach can be advantageous for soft error tolerant designs constrained with a tight energy consumption budget with a minimal impact on the reliability by 1% for the soft error effects. Furthermore, the area overhead for the TSVL is estimated by measuring the implementation area in um^2, and it turned out that the proposed scheme requires 54.53 um^2, whereas 66.5, 64.9, and 43.4 um^2 is needed to configure $S27$ benckmark circuit with TMR, Self-Voting DMR, and temporal redundancy approach, respectively. Figure 6 (a) shows the area overhead for a set of ISCAS89 benchmark circuits with a distinct combinational and sequential logic ratio. It can be seen that the proposed approach imposes an area overhead comparable to the temporal redundancy, while achieving significant reduction as compared to Self-Voting DMR or TMR approach. In addition, Self-Voting DMR approach realizes an area reduction when the sequential logic portion is high, while the proposed approach saves significant area either if the sequential logic portion is high or if the combinational logic portion is high. On average, TSVL approach imposes less area overhead by 22.02% and 36.84% as compared to Self-Voting DMR approach, presented in [10], and TMR, respectively. In terms of power consumption, TSVL realizes a power consumption improvement of 20.1% and 35.55% over the Self-Voting DMR and conventional TMR approach, respectively. Therefore, for applications which seek to protect a design against soft errors with constant energy budget, it is advantageous to utilize TSVL approach as it imposes high level of protection, besides achieving significant reduction in area-energy overhead as compared to other hardening redundancy-based techniques.

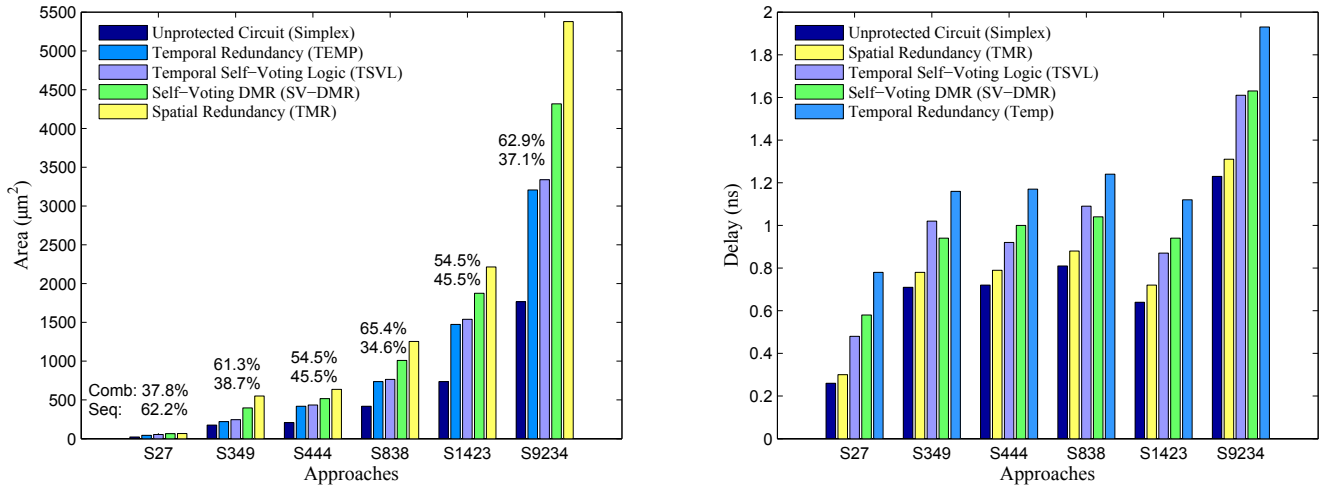

Fig. 6: Evaluation of redundancy-based soft error masking techniques; (a) area overhead , (b) speed performance.

TABLE III: Mean area-power consumption and delay of redundancy-based approaches w.r.t. simplex design.

Design Implementation	**Normalized Area**	**Normalized Power**	**Normalized Delay**
Spatial Redundancy	$3.14x$	$3.11x$	$1.19x$
Temporal Redundancy [15]	$1.88x$	$1.83x$	$1.69x$
Self-Voting DMR [10]	$2.48x$	$2.46x$	$1.4x$
Proposed Approach (TSVL)	$1.96x$	$1.91x$	$1.37x$
Proposed Approach (HSTR-DEC)	$2.6x$	$2.54x$	$1.43x$

In terms of performance, TSVL provides a comparable speed performance to that of Self-Voting DMR approach, shown in Figure 6 (b), as both incur a phase delay within a period that depends on the SET pulse width. Overall, TSVL outperforms Self-Voting DMR by 2.15%. A transient pulse of 200 psec was considered in order to generate CLK2 that triggers the second and third flip-flop of TSVL and Self-Voting DMR approach, respectively. Thus, an SET pulse within a width larger than the considered phase delay might be captured by a flip-flop if it arrives at the setup/hold time thereby causing an upset in that storage element, unless it is masked via the electrical or logical masking mechanism.

Interestingly, HSTR-DEC approach is able to tolerate an SET within a width wider than 200 psec. However, in this case the transient pulse should occur in the original datapath only, $Data_{in1}$, and the redundant datapath should be error-free at the same time, and vice versa. This indicates that HSTR-DEC is able to tolerate a single SET with a width larger than the considered phase delay as long as the other datapath is correct. On the other hand, HSTR-DEC scheme is able to tolerate two simultaneous SETs within a width up to 200 psec. While TMR, temporal redundancy, and self-voting DMR approaches achieve complete fault masking coverage for SEU in single module simultaneously, HSTR-DEC approach realizes complete fault masking coverage for SEU in single or double module concurrently. In addition to its increased level of reliability, the proposed scheme consumes acceptable extra logic for error masking. The evaluation results indicate that HSTR-DRC approach reduces area and power overheads roughly by 18.2% and 16.83%, respectively, and imposes the performance by 20.17% as compared to conventional TMR using 15nm technology. On the other hand, it improves speed performance by 15.38% while incurring 19.23% of area overhead as compared to temporal redundancy approach. Likewise, it achieves comparable overheads in terms of power, area, and delay as compared to previous works of hybrid redundancy approach, presented in [10], as both utilize duplicated datpaths and triplicated flip-flops. However, our approach is able to tolerate double upsets, occurred at the same time, whereas conventional TMR, temporal redundancy, and SV-DMR are unable to detect and correct double upsets simultaneously. Table III lists the area, power consumption, and speed degradation penalties of the redundancy-based soft error mitigation techniques, normalized to the simplex (non-redundant) design. In addition to increased levels of fault coverage, the proposed approaches are considered a compromise solution ranging between the spatial and temporal redundancy approaches, as they realize a high protection against soft error effects, MBUs tolerance for HSTR-DEC, and impose acceptable overheads in terms of area, power, and performance degradation.

V. Conclusion

Technology trends of CMOS devices have improved the capability of contemporary processors. However, it has increased the susceptibility of CMOS circuits to transient faults. Thus, SER masking approaches are sought to increase reliability within speed, area, and energy consumption constraints. In this work, a reliable and cost-effective, area and energy efficient, redundancy-based approaches have been developed to mitigate soft error effects at the circuit/module-level. The proposed soft error-tolerant techniques are able to tolerate both transient and upset faults and provide complete SEUs protection, detection and masking. TSVL was synthesized and simulated using 15nm technology process, and the experimental results indicate that TSVL can reduce SER roughly by 99% if the delay phase shift is designed adequately, while achieving an improvement of 22.02% and 2.15% for area and speed degradation, respectively, as compared to Self-Voting DMR approach. On the other hand, HSTR-DEC approach imposes comparable speed performance and area overheads as compared to SV-DMR hybrid redundancy approach, in addition to its ability to tolerate double SEUs simultaneously.

References

[1] P. Reviriego, C. J. Bleakley, and J. A. Maestro, "Structural DMR: A technique for implementation of soft-error-tolerant FIR filters," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 58, no. 8, pp. 512–516, Aug. 2011.

[2] J. Chen, S. Chen, Y. He, J. Qin, B. Liang, B. Liu, and P. Huang, "Novel layout technique for single-event transient mitigation using dummy transistor," *Device and Materials Reliability, IEEE Transactions on*, vol. 13, no. 1, pp. 177–184, March 2013.

[3] O. Amusan, A. Steinberg, A. Witulski, B. Bhuva, J. Black, M. Baze, and L. Massengill, "Single event upsets in a 130 nm hardened latch design due to charge sharing," in *Reliability physics symposium, 2007. proceedings. 45th annual. ieee international*, April 2007, pp. 306–311.

[4] Y. Lin, M. Zwolinski, and B. Halak, "A low-cost, radiation-hardened method for pipeline protection in microprocessors," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[5] D. Tang, C. He, Y. Li, H. Zang, C. Xiong, and J. Zhang, "Soft error reliability in advanced CMOS technologies-trends and challenges," *Science China Technological Sciences*, vol. 57, no. 9, pp. 1846–1857, Sep. 2014.

[6] N. Eftaxiopoulos, N. Axelos, and K. Pekmestzi, "DONUT: A double node upset tolerant latch," in *VLSI (ISVLSI), 2015 IEEE Computer Society Annual Symposium on*, July 2015, pp. 509–514.

[7] N. Mahatme, B. Bhuva, N. Gaspard, T. Assis, Y. Xu, P. Marcoux, M. Vilchis, B. Narasimham, A. Shih, S.-J. Wen, R. Wong, N. Tam, M. Shroff, S. Koyoma, and A. Oates, "Terrestrial SER characterization for nanoscale technologies: A comparative study," in *Reliability Physics Symposium (IRPS), 2015 IEEE International*, April 2015, pp. 4B.4.1–4B.4.7.

[8] V. Ferlet-Cavrois, L. Massengill, and P. Gouker, "Single event transients in digital CMOS–A review," *Nuclear Science, IEEE Transactions on*, vol. 60, no. 3, pp. 1767–1790, June 2013.

[9] R. Rao, D. Blaauw, and D. Sylvester, "Soft error reduction in combinational logic using gate resizing and flipflop selection," in *Computer-Aided Design, 2006. ICCAD '06. IEEE/ACM International Conference on*, Nov 2006, pp. 502–509.

[10] J. Teifel, "Self-voting Dual-Modular-Redundancy circuits for single-event-transient mitigation," *Nuclear Science, IEEE Transactions on*, vol. 55, no. 6, pp. 3435–3439, Dec. 2008.

[11] J. Celis, S. De La Rosa Nieves, C. Fuentes, S. Gutierrez, and A. Saenz-Otero, "Methodology for designing highly reliable fault tolerance space systems based on COTS devices," in *Proceedings of the IEEE International Systems Conference (SysCon)*, 2013, pp. 591–594.

[12] M. Pignol, "How to cope with SEU/SET at system level?" in *Proceedings of the 11th IEEE International On-Line Testing Symposium (IOLTS)*, Jul 2005, pp. 315–318.

[13] R. Al-Haddad, R. Oreifej, R. Ashraf, and R. F. DeMara, "Sustainable modular adaptive redundancy technique emphasizing partial reconfiguration for reduced power consumption," *International Journal of Reconfigurable Computing*, vol. 2011, no. 430808, 2011.

[14] M. Nicolaidis, "Design for soft error mitigation," *Device and Materials Reliability, IEEE Transactions on*, vol. 5, no. 3, pp. 405–418, Sept 2005.

[15] D. Mavis and P. Eaton, "Soft error rate mitigation techniques for modern microcircuits," in *Reliability Physics Symposium Proceedings, 2002. 40th Annual*, 2002, pp. 216–225.

[16] P. Reviriego, O. Ruano, M. Flanagan, S. Pontarelli, and J. Maestro, "An efficient technique to protect serial shift registers against soft errors," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 60, no. 8, pp. 512–516, Aug. 2013.

[17] M. Shokrolah-Shirazi and S. Miremadi, "FPGA-based fault injection into synthesizable verilog HDL models," in *Secure System Integration and Reliability Improvement, 2008. SSIRI '08. Second International Conference on*, July 2008, pp. 143–149.