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Adaptive Mitigation of Radiation-Induced Errors and TDDB in Reconfigurable Logic Fabrics

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Motivations and Goals

- FPGAs are susceptible to radiation-induced soft faults such as Single Event Upsets (SEUs).
  - ✓ *TMR and Scrubbing techniques in literature can address adequately*
- Hard-faults need new handling techniques to sustain long mission lifetimes
  - ✓ *Significant aging effects at sub 45nm technology nodes*

Sponsors: ***NASA*: FPGA platform and Genetic Algorithm research**
***DARPA*: OC approach and SOAR Longevity Platform**

OC Approach: addresses system controllability with increasing complexity

System Property	Composed of large collection of autonomous systems	Autonomous system owned sensor and actuators	Communication networks among autonomous systems
Self-x Characteristics	•Self-organization •Self-configuration •Self-optimization	•Self-healing •Self-protection •Self-explaining	•Context-awareness •Self-synchronization

Contributions

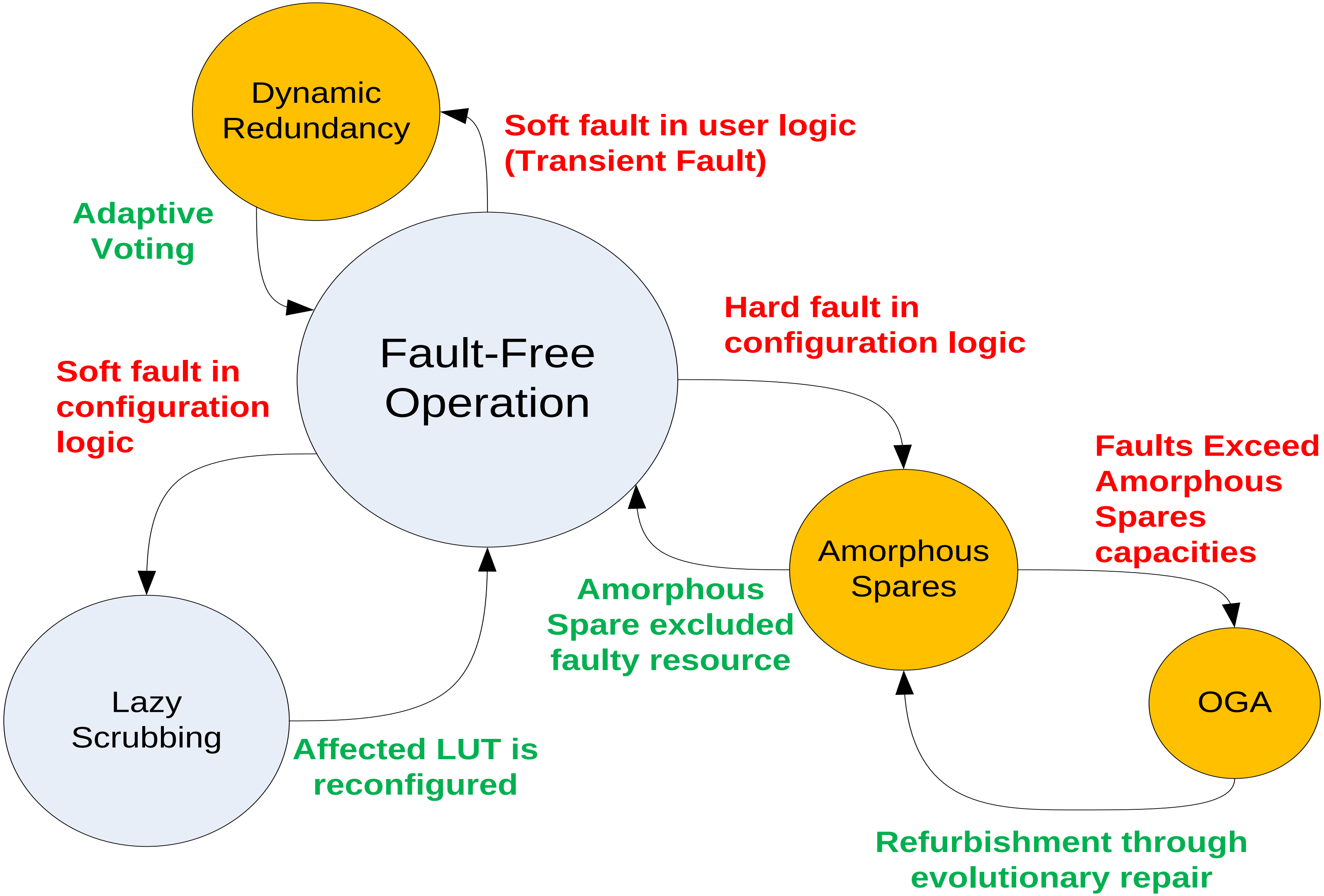
C-1) Sustainable Modular Adaptive Redundancy Technique, (SMART) supporting:

- **a) Adaptive Modular Redundancy (AMR), in contrast to the fixed one in Duplex and TMR, by exploiting the reconfigurability of FPGAs:** ***Adaptive Behavior***
- **b) Organic autonomous soft and hard fault-tolerance technique** ***Increased Availability***
- **c) Runtime self-regulation of availability, area, and energy based on mission status and requirements:** ***Lower Overhead***

C-2) Continuous Markov Time Chains (CMTC) modeling approach with standard evaluation metrics for availability, power, and area.

C-3) Novel Organic Genetic Algorithm (OGA) targeting self-repair and refurbishment of SRAM-based FPGA devices.

SMART's Operational Phases



Dynamic Redundancy

Soft fault in user logic (Transient Fault)

Adaptive Voting

Fault-Free Operation

Hard fault in configuration logic

Soft fault in configuration logic

Faults Exceed Amorphous Spares capacities

Amorphous Spares

Amorphous Spare excluded faulty resource

OGA

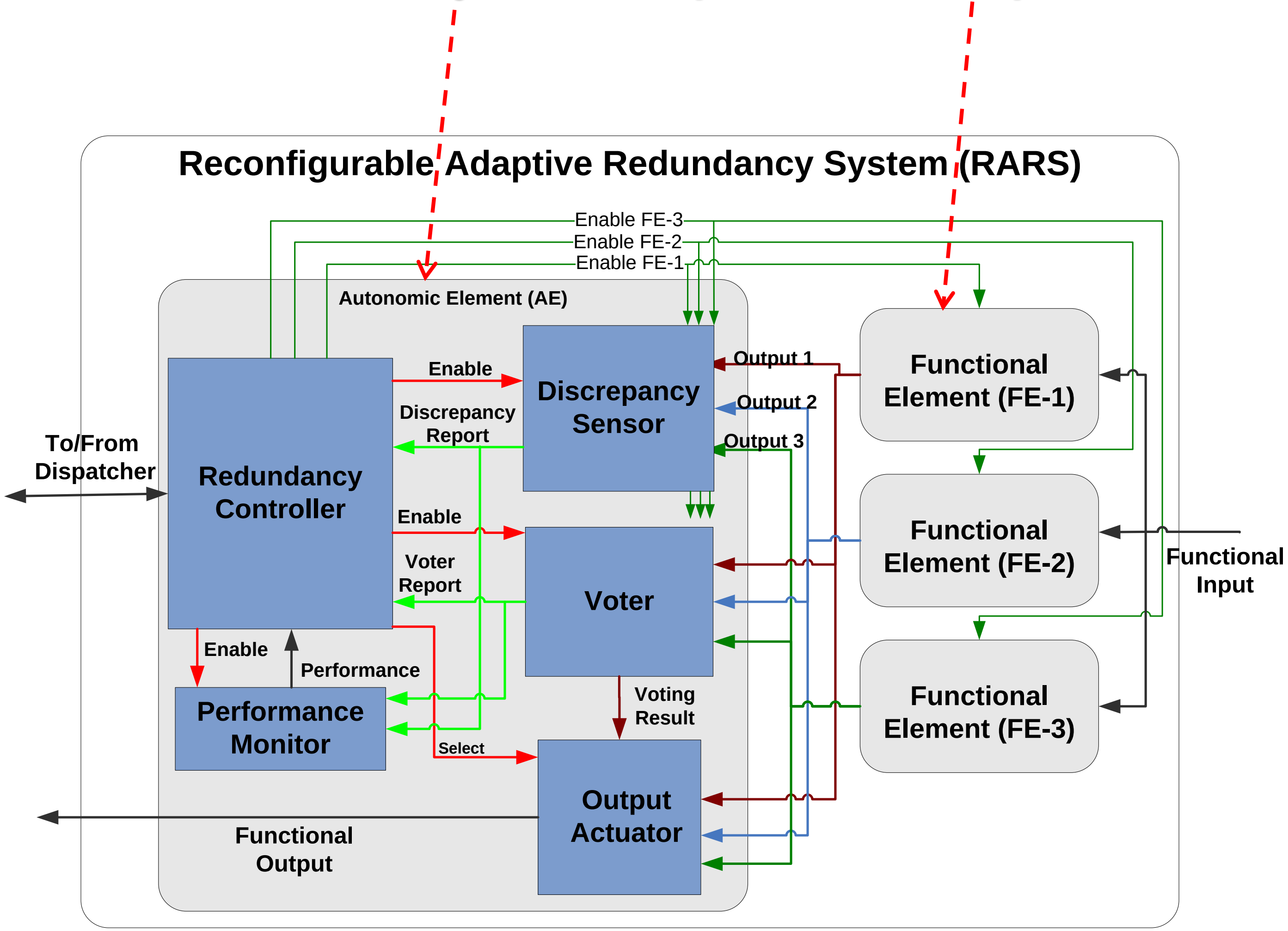
Lazy Scrubbing

Affected LUT is reconfigured

Refurbishment through evolutionary repair

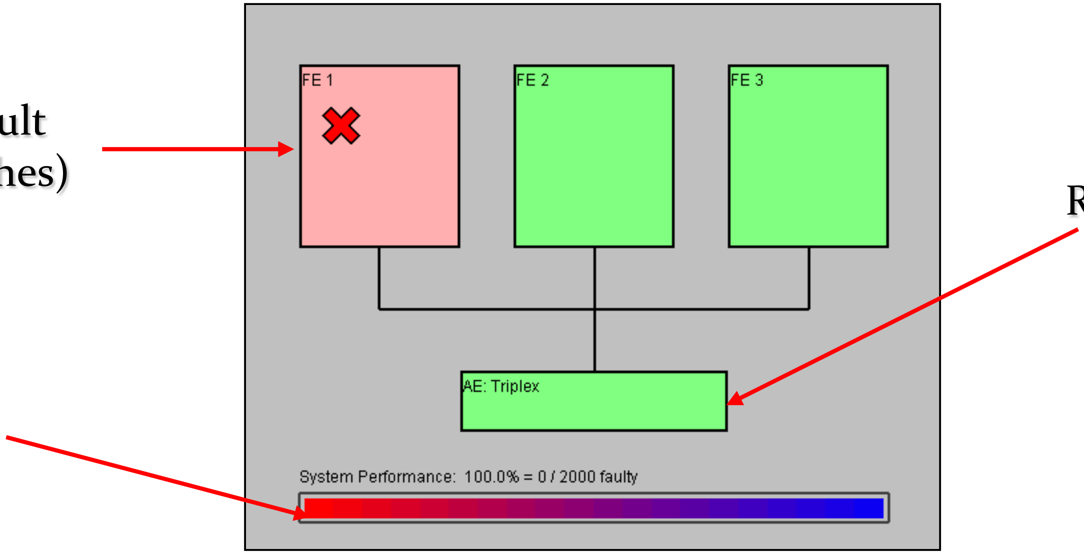
Hardware Layer (RARS)

- Reconfiguration enables *dynamic adaptation* of *data path* during the mission



Software Layer

- Monitors the higher level behavior of the system such as the status of each FE, configuration of AE and the overall performance level.
- Enable higher-level recovery techniques:
    1. Lazy Scrubbing: SEUs in configuration logic
    2. Amorphous Spares: Hard Faults when spare resources are available
    3. Organic GA (OGA): More persistent hard faults.
- Validated using a novel Human Interface Module (HIM) with graphical user interface (Java applet) to depict mission status and control it



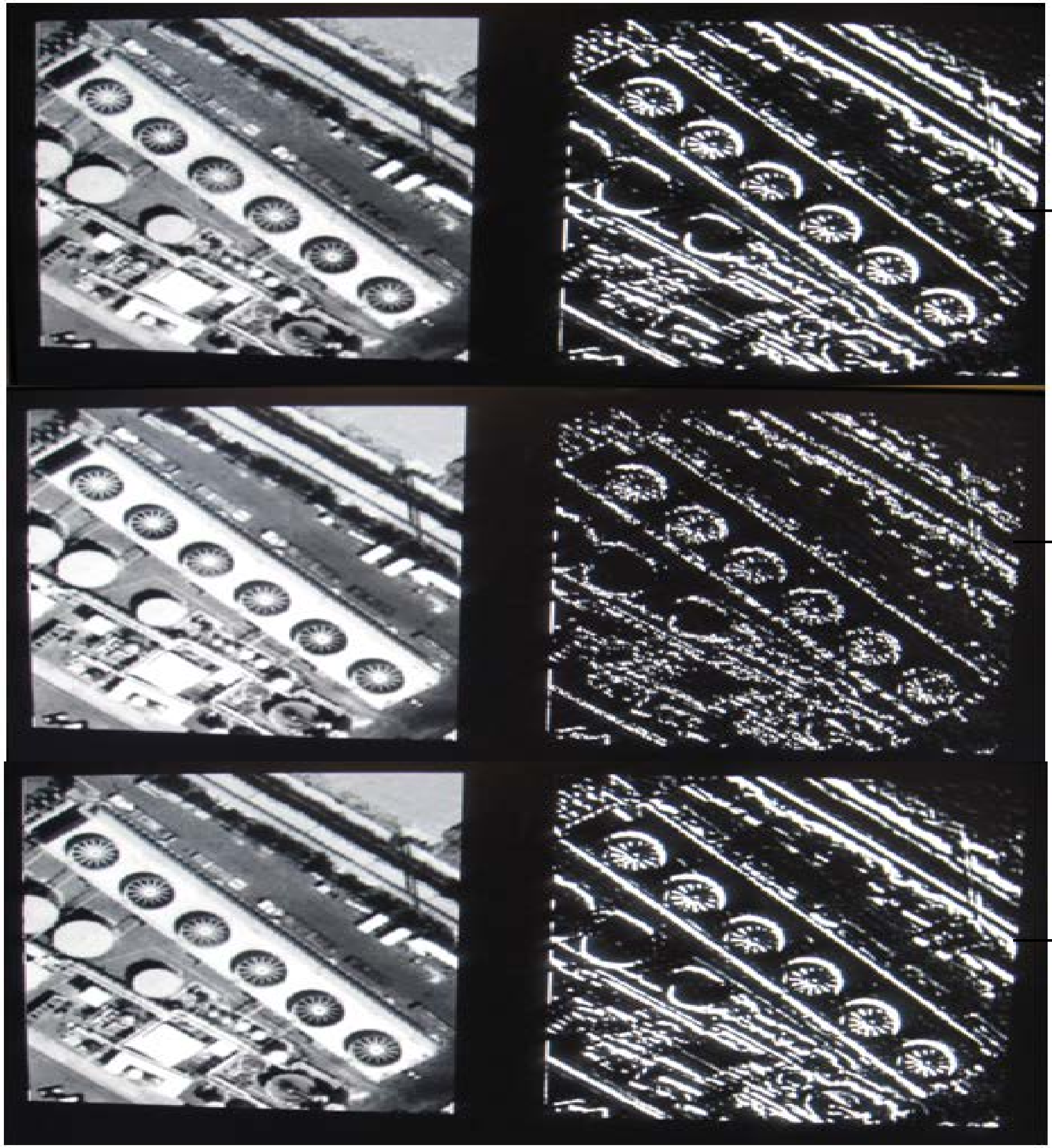
System Performance: 100.0% = 0 / 2000 faulty

Injected fault (DIP switches)

RARS status

Performance bar

Experimental Results (RARS)



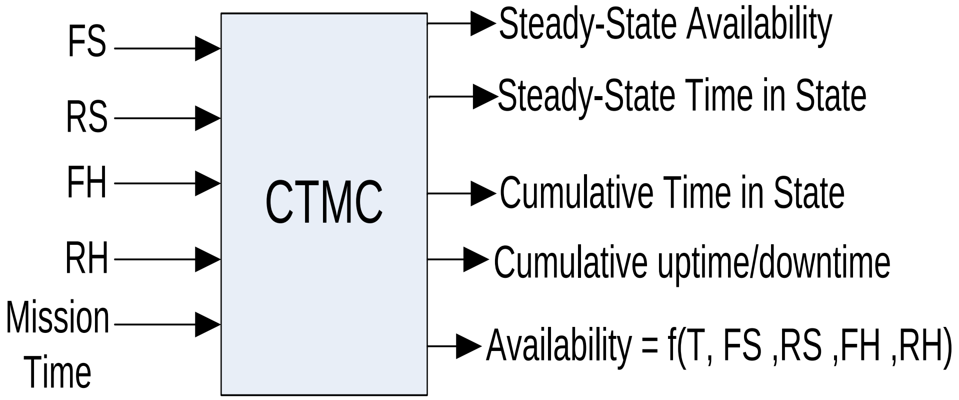
Normal fault-free output

Degraded output

Refurbished 100% performance output

Continuous Time Markov Chain of 9 Realistic Use Cases

UC #	Description
1	**Demanding** conditions Rapid repair period
2	**Moderate** conditions Rapid repair period
3	**Favorable** Conditions Rapid repair period
4	**Demanding** conditions Lengthy repair period
5	**Moderate** conditions Lengthy repair period
6	**Favorable** Conditions Lengthy repair period
7	**Demanding** conditions Intermediate Repair period
8	**Moderate** conditions Intermediate Repair period
9	**Favorable** Conditions Intermediate Repair period



FS

RS

FH

RH

Mission Time

CTMC

Steady-State Availability

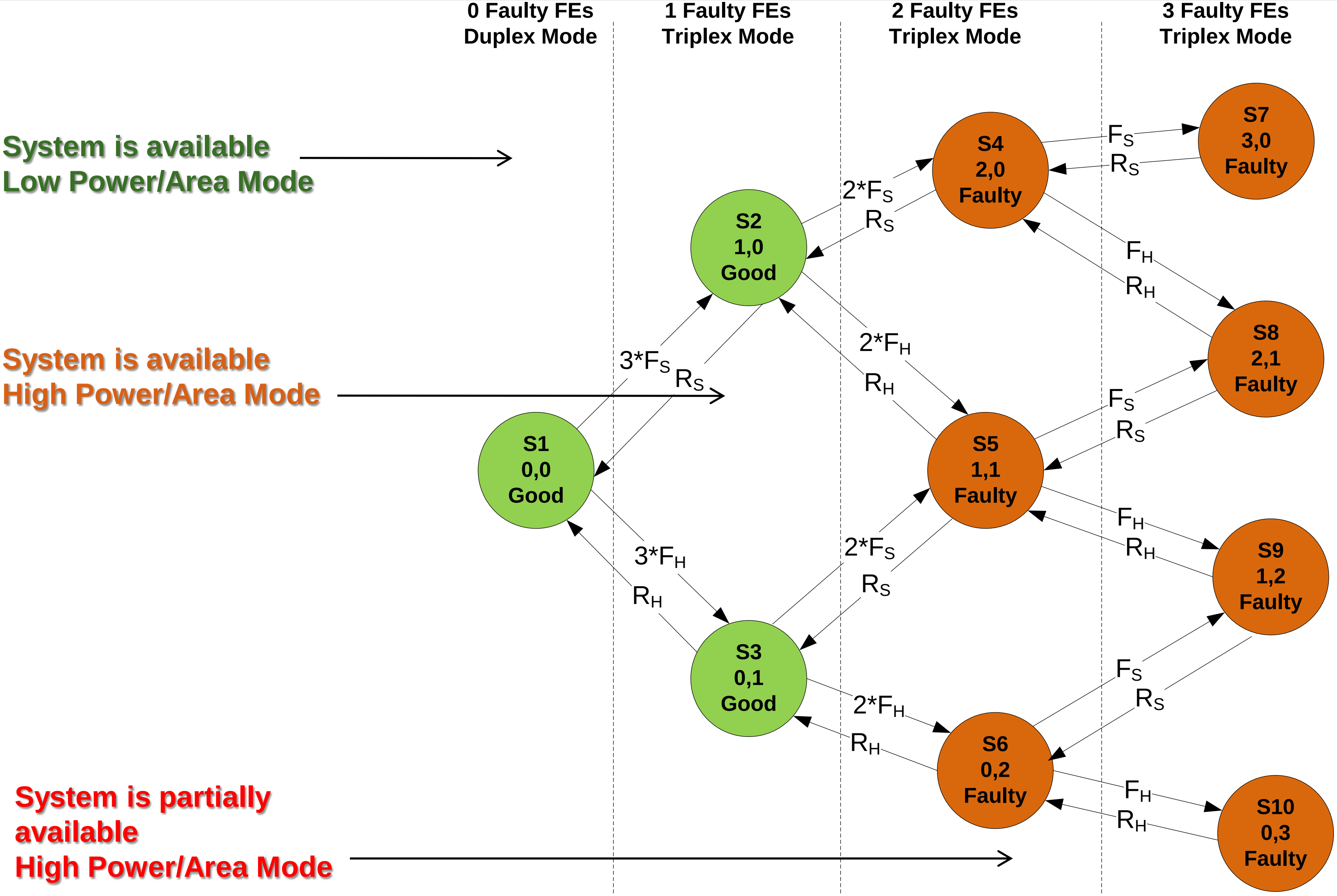
Steady-State Time in State

Cumulative Time in State

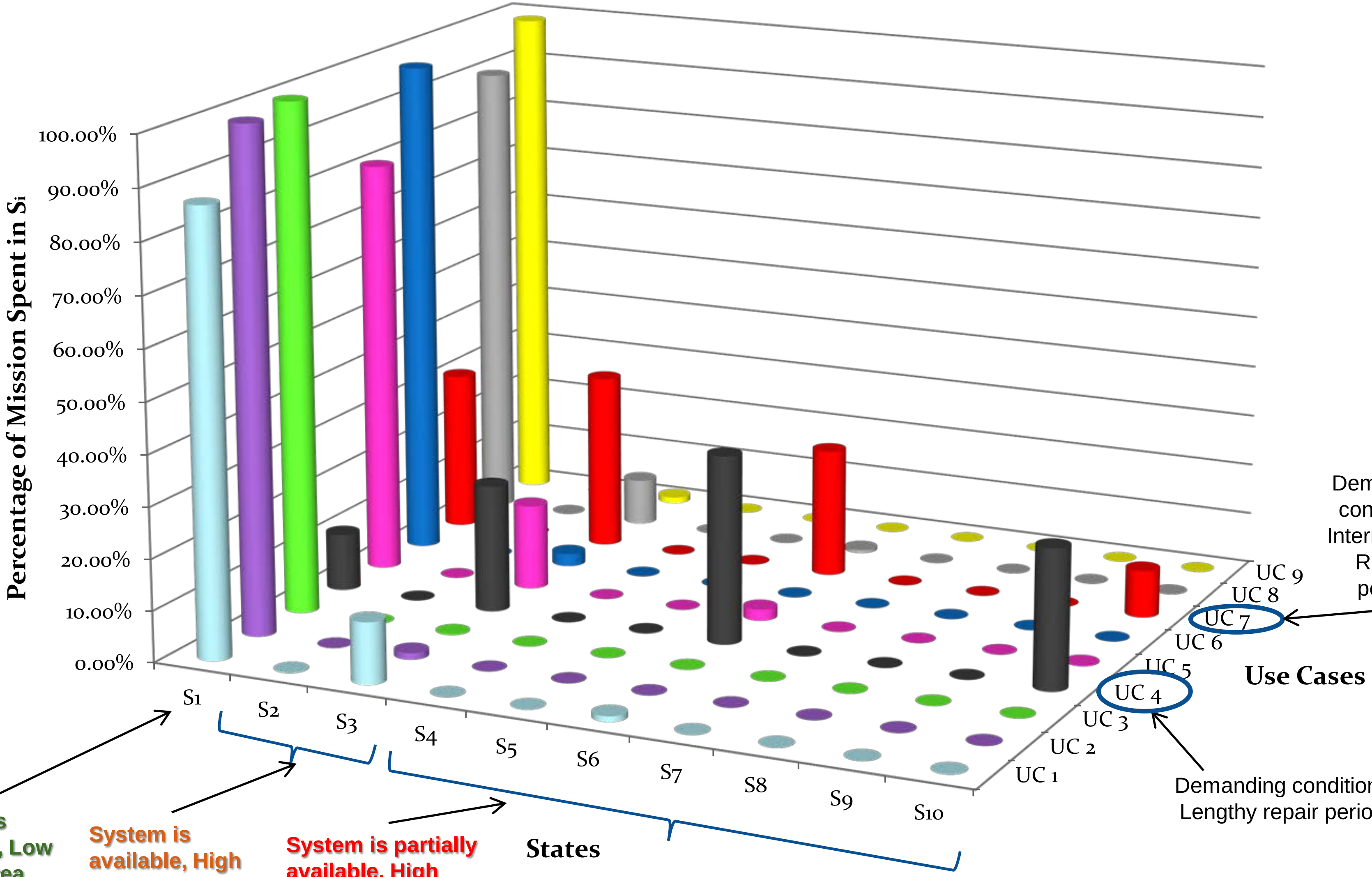
Cumulative uptime/downtime

Availability = f(T, FS ,RS ,FH ,RH)

CTMC Availability Analysis



Percentage of Mission Time in S_i



Demanding conditions Intermediate Repair period

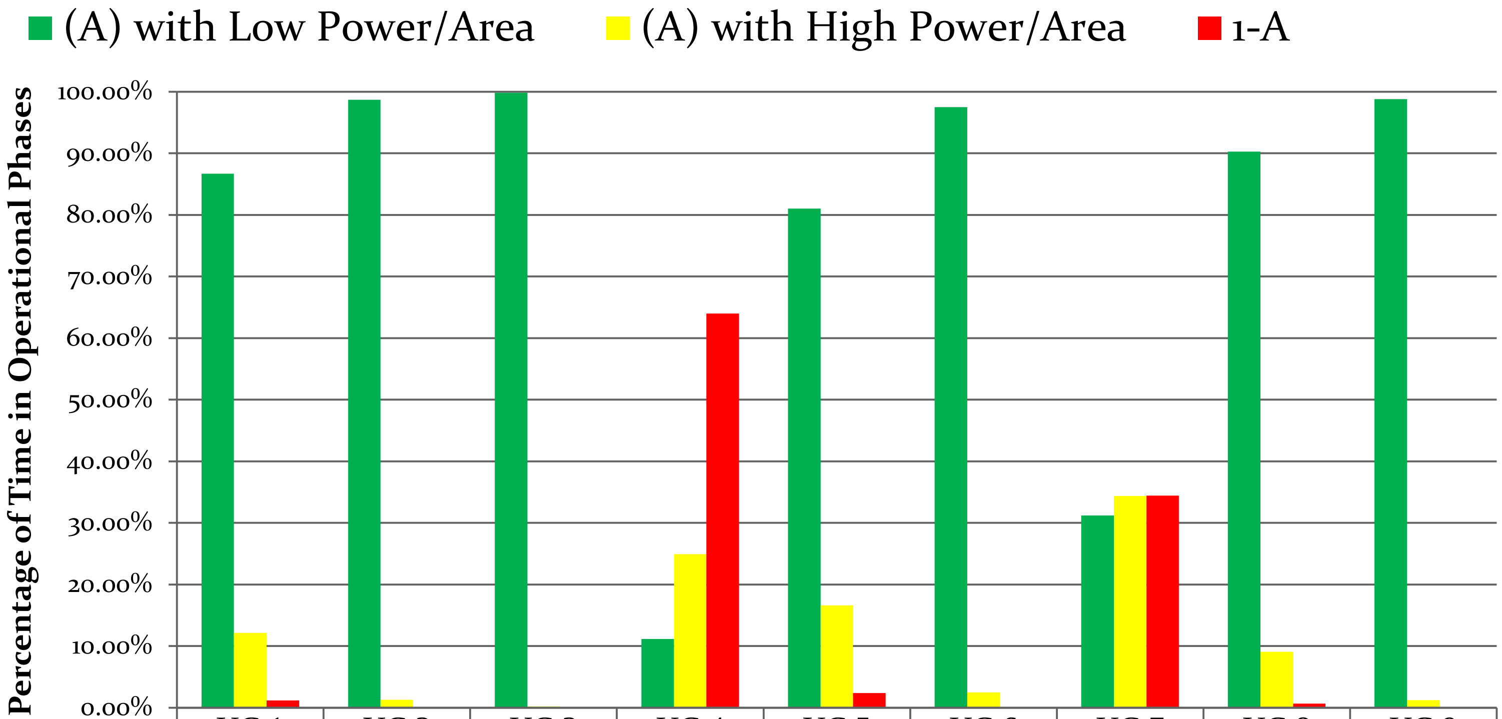
Demanding conditions Lengthy repair period

System is available, Low Power/Area Mode

System is available, High Power/Area Mode

System is partially available, High Power/Area Mode

Operational Phases of SMART



	UC 1	UC 2	UC 3	UC 4	UC 5	UC 6	UC 7	UC 8	UC 9
(A) with Low Power/Area	86.70%	98.71%	99.83203%	11.13%	81.02%	97.50%	31.19%	90.28%	98.79%
(A) with High Power/Area	12.14%	1.28%	0.16782%	24.89%	16.62%	2.46%	34.38%	9.07%	1.20%
1-A	1.16%	0.01%	0.00015%	63.98%	2.36%	0.04%	34.43%	0.65%	0.01%

% Availability	98.8417	99.9899	99.9999	36.0179	97.6778	99.9526	65.5709	99.3451	99.9925

Standardized TMR Benchmarks

- Each of the **4x7=28** designs are compared to RARS in term of area and power

Voter Selection

1. Triplicate logic only (TL)
2. Triplicate login and input ports (TLI)
3. Triplicate logic and output ports only (TLO)
4. Triplicate logic, input, and output ports (TLIO)

Voter Insertion Algorithm

1. Voters before Every Flip-Flop Algorithm
2. Voters after Every Flip-Flop Algorithm
3. Basic Strongly Connected Components (SCC) Decomposition Algorithm
4. Highest Fanout SCC Decomposition Algorithm
5. Highest Flip-Flop Fanout SCC Decomposition Algorithm
6. Highest Flip-Flop Fanin Input
7. Highest Flip-Flop Fanin Output

Overhead Savings Model

- TMR always consumes 3 times the resources overhead only to mask faults in finite portions of the mission
- RARS enables redundant parts when they are required

Overhead of RARS:

$$O_{RARS} = T_{S1} \times O_{DX} + (1 - T_{S1}) \times O_{TX}$$

Duplex Mode Overhead:

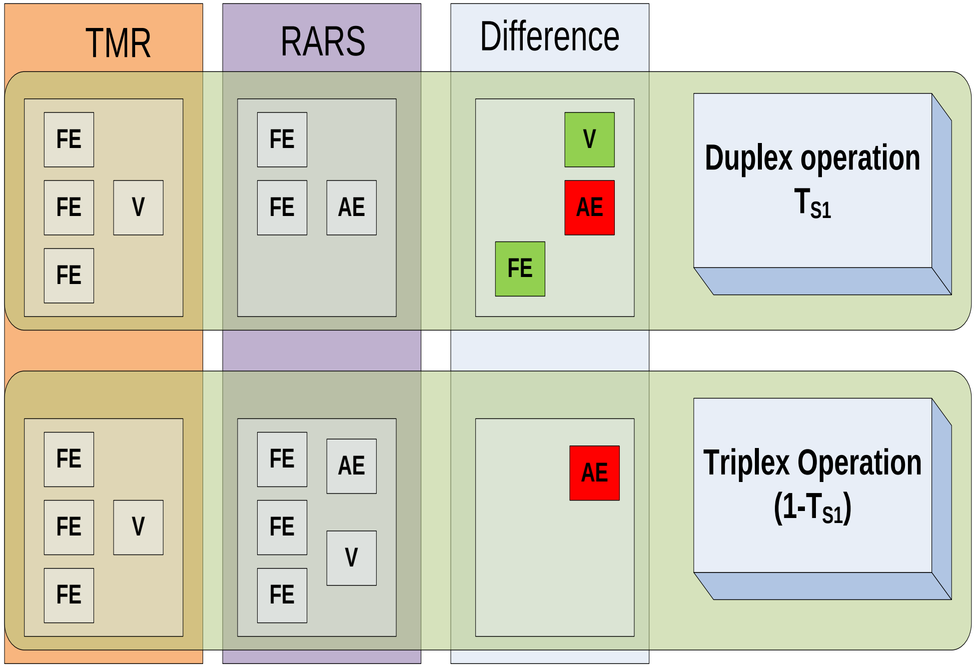
$$O_{DX} = 2 \times O_{FE} + O_{AE}$$

Triplex Mode Overhead:

$$O_{TX} = 3 \times O_{FE} + O_{AE} + O_{V}$$

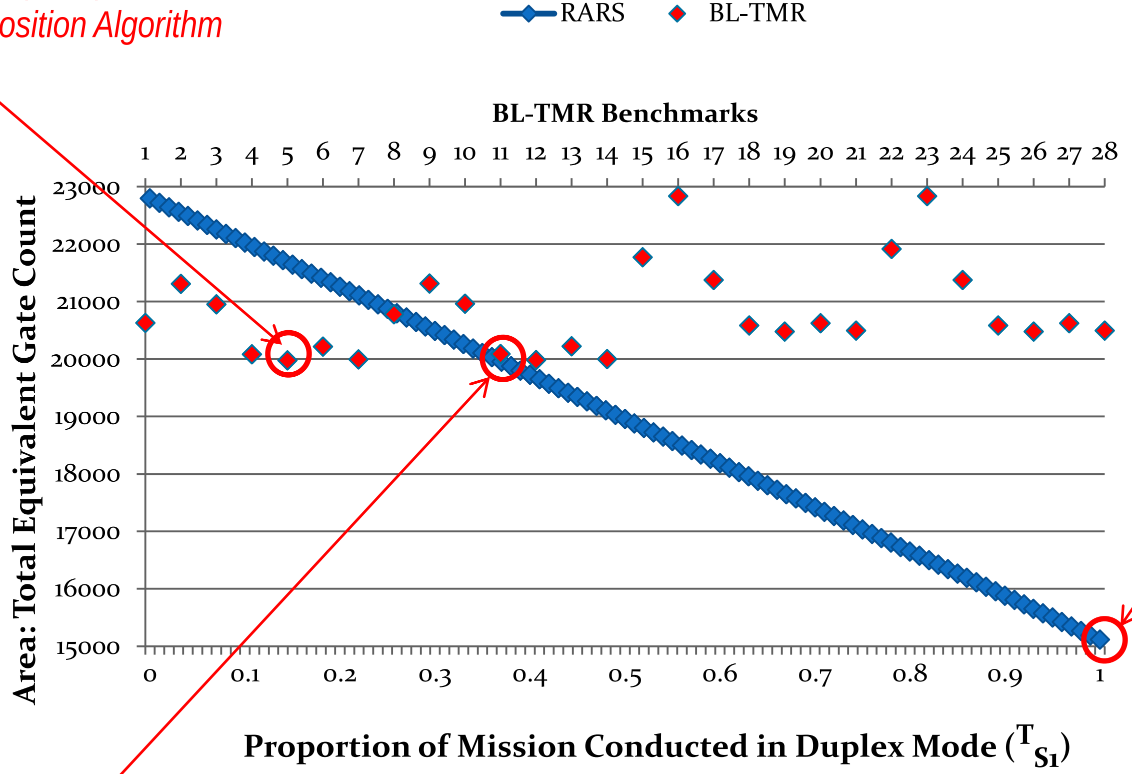
Overhead savings of RARS compared to TMR:

$$O_S = \frac{O_{TMR} - O_{RARS}}{O_{TMR}}$$



TMR Vs RARS Areas

Winner Design (Area):
TL + Highest Flip-Flop Fanout
SCC Decomposition Algorithm



TS1 = 100%
Area Savings: 24.33%
Power Savings: 29.52%

T_{S1} > 37%:
RARS starts to require
less area than TMR

Comparison to Winner TMR Benchmarks

UC	S1 (A, Low Power, low Area)	S2, S3 (A, High Power, High Area)	S4-S10 1-A, High Power, High Area)	A (%)	RARS Avg Power	RARS Avg Area	Power Savings over Design 22	Area Savings over Design 5	Recom-mended method
1	86.704%	12.1379%	1.15828%	98.8417	125.3	15319.13	24.66%	19.22%	SMART
2	98.707%	1.28331%	0.01014%	99.9899	118	14284.5	29.05%	23.83%	SMART
3	99.833%	0.16663%	0.00012%	99.9999	117.3	14187.37	29.46%	24.27%	SMART
4	11.130%	24.8876%	63.9821%	36.0179	171.2	21833.57	-2.94%	-9.83%	TMR
5	81.162%	16.5161%	2.32216%	97.6778	128.7	15796.86	22.64%	17.09%	SMART
6	97.522%	2.43057%	0.04736%	99.9526	118.7	14386.6	28.62%	23.38%	SMART
7	31.189%	34.3823%	34.4291%	65.5709	159	20104.55	4.38%	-2.12%	TMR
8	90.189%	9.15584%	0.65490%	99.3451	123.2	15018.69	25.94%	20.56%	SMART
9	98.798%	1.19488%	0.00749%	99.9925	118	14276.64	29.08%	23.87%	SMART

1. SMART is recommended in 7 out of 9 use cases
2. TMR savings are nominal: *AE Overhead*
3. SMART savings are significant: *FE Overhead*

Conclusion

- Adaptive Modular Redundancy (AMR) is shown to sustain stressful sequences of injected soft and hard faults while maintaining minimal required resources ➔Substantiating C-1.a
- Hard faults tolerance significantly impacts system availability, increasing it from 35% in UC4 to 98% in UC1 ➔ Substantiating C-1.b
- Dynamic PR reduces FE configuration time by 98.2% compared to full CBS, and allows the system to remain online while under repair ➔ Substantiating C-1.b
- RARS Exploits the reconfigurability of FPGAs to provide 15%-30% power and area savings over standard TMR techniques ➔Substantiating C-1.c
- Development of new evaluation metrics based on Monte Carlos simulation of CTMC and innovative triplication tools, helping in predicting and controlling mission-critical systems. ➔ Substantiating C-2
- Novel organically-amenable Genetic Algorithm (OGA) targeting hard-fault repair in FPGAs is shown capable of repairing injected hard faults in average of 149 generations ➔ Substantiating C-3