# Applicability of Power-Gating Strategies for Aging Mitigation of CMOS Logic Paths

**Navid Khoshavi, Rizwan A. Ashraf, and Ronald F. DeMara**
Department of Engineering and Computer Science
University of Central Florida
Orlando, FL, USA 32816-2362
e-mail: demara@mail.ucf.edu

***Abstract*—Aggressive CMOS technology scaling trends exacerbate the aging-related degradation of propagation delay and energy efficiency in nanoscale designs. Recently, Power-gating has been utilized as an effective low-power design technique which has also been shown to alleviate some aging impacts. However, the use of MOSFETs to realize power-gated designs will also encounter aging-induced degradations in the sleep transistors themselves which necessitates the exploration of design strategies to utilize power-gating effectively to mitigate aging. In particular, Bias Temperature Instability (BTI) which occurs during activation of power-gated voltage islands is investigated with respect to the placement of the sleep transistor in the header or footer as well as the impact of ungated input transitions on interfacial trapping. Results indicate the effectiveness of power-gating on NBTI/PBTI phenomena and propose a preferred sleep transistor configuration for maximizing higher recovery.**

***Keywords—aging; power-gating; voltage islands; sleep trasnsistor; MOSFET threshold-voltage shift; Bias Temperature Instability (BTI); NBTI; PBTI; low power design.***

## I. INTRODUCTION AND PREVIOUS WORK

As technology scales, *Bias Temperature Instability (BTI)* has become a significant reliability concern for circuit designers. The combined impact of increasing oxide field strength and the use of oxynitrides have exacerbated this aging effect [1]. The former has become prominent to enhance transistor performance without scaling gate oxide thickness while the latter has been used to prevent Boron penetration and reduce gate leakage [2]. For instance, *Negative BTI (NBTI)* manifests itself as an increase in the transistor threshold voltage whenever a PMOS transistor is negatively biased, causing logic gates to switch at slow rates, and thus the critical paths may become unable to meet timing constraints. In order to alleviate the impact of NBTI-induced degradation, several studies have proposed techniques at various design abstraction levels, from the circuit level [1]-[4] up through the architecture level [5]–[11] to deal with these degradations. At the architecture level, techniques have been proposed to bias input vectors to mitigate aging [5], perform aging-aware scheduling [8], apply voltage scaling [11], implement power-gating [6] and utilize a combination of power-gating and operation at a greater-than-nominal supply voltage [12] to mitigate the effects of aging.

Power-gating reduces the duration of circuit operation and hence power consumption as well as temperature, both of which can decrease BTI effects. Furthermore, the stress interval of MOS transistors is reduced because a power-gated MOS transistor enters a recovery condition due to clearing of interfacial traps. In [12], two alternating phases are utilized. In the first phase, the circuit operates at a greater-than-nominal supply voltage which completes tasks more quickly to generate idle-time slack. Next, sleep-mode is activated in the second phase which deactivates the circuit. These circadian rhythms were shown to reduce delay degradation by about 1.3-fold to 1.8-fold. Alternately, design-time mitigation approaches have been provided. For example, the authors of [13] propose use of accurate aging models for NBTI at microarchitecture-level which are derived and validated with transistor-level models. A survey of power-gating techniques to mitigate BTI effect is presented in [14].

In order to utilize power-gating techniques, a transistor inserted into the header and/or footer called a *Sleep Transistor (ST)* is inserted to realize a pull-up and/or pull-down supply network to provide a virtual $V_{DD}$ or $V_{SS}$. The ST reduces the leakage current that flows in the supply-ground path when the circuit is in its stand-by mode which is known as sleep mode. However, the ST suffers continuous BTI stress during active mode and can age significantly. The aging impact will aggravate the performance degradation of the logic circuit in a power-gating structure [6]. NMOS devices exhibit a smaller threshold voltage shift than PMOS devices under the effect of NBTI [18]. Conversely, PBTI on NMOS can be the dominant degradation mechanism. Accordingly, the power-gating model used in order to mitigate a BTI effect is important.

In order to alleviate aging of ST, several works have been presented previously. The authors of [15] proposed to realize NBTI-aware power-gating through *(i)* sleep transistor over-sizing, *(ii)* forward body-biasing, and *(iii)* stress time reduction. However, the aging of logic networks has not been considered in that work. In [16], authors showed the interdependence between the degradation or logic networks and the ST. In their work, redundant STs are introduced for mitigating the aging of a single ST. This is shown to extend the lifetime of power-gated circuits. With the existence of ST redundancy, the recovery mechanism is explored by recovering redundant STs in a round-robin sequence. Consequently, a sufficient recovery interval is provided to STs for reversing NBTI. Hence, a decrease in the virtual $V_{DD}$ due to ST aging is postponed, which mitigates the long-term performance degradation and extends the circuit lifetime. The authors of [17] evaluated the reliability and power consumption benefits of power-gated circuits in 22nm technology under the effects of NBTI/PBTI. They found that power-gating can improve the reliability and provide significant power savings as long as sufficient time for the circuit is provided in sleep mode. For example, [14] reports that to reduce the delay degradation by 5% over an operational period of 10 years, the circuit must remain power-gated for over 60% of the device lifetime which may represent an unacceptable reduction in operational capacity. Thus, alternative approaches have constituted an active area of research [20].

In this work, we evaluate the effectiveness of power-gating on PBTI/NBTI phenomenon and propose a preferred ST configuration for achieving improved recovery. In addition, different input frequency signals with the same duty cycle are considered as a case study to obtain more complete results which include the effect of input transitions on the recovery of MOSFET transistors while in sleep mode.

## II. POWER-GATING SCENARIOS

There are several possible power-gating scenarios based on the location of the ST in the header or footer. To evaluate these, a case study is considered using 50 CMOS inverters which are connected in series, as shown in Fig. 1(a). For the baseline circuit, supply voltage and ground are directly connected without any ST. We implement three different power-gating scenarios in order to investigate the impact of BTI on each of them. In the *Header-based ST (HST)*, we insert a PMOS ST to create virtual $V_{DD}$ as illustrated in Fig. 1(b). Since the PMOS ST in power-gated circuit suffers from NBTI in active mode and ages quickly, it degrades the performance of logic elements due to supply voltage changes. One advantage of an HST arrangement is that PMOS transistor exhibits less leakage current than NMOS transistor of equivalent size. The NBTI effect elevates $V_{th}$ over time and makes PMOS transistor even less leaky. The disadvantage of an HST arrangement is that PMOS has lower drive current than NMOS of a same size. As a result, a HST implementation usually consumes more area than a *Footer-based ST (FST)* implementation.

In FST, we insert a NMOS ST between $V_{SS}$ and actual ground, shown in Fig. 1(c). The advantage of FST is its high drive current and hence smaller area for equivalent performance. However, NMOS is leakier than PMOS and application designs become more sensitive to ground noise on the virtual ground coupled through the FST. The NMOS ST also suffers from PBTI in active mode which imposes additive performance loss. However, the performance loss of HST and FST circuits is not equal since PMOS ST experiences more dramatic aging effects when it is used in an HST structure in compare to NMOS ST in a FST design. Consequently, HST and FST designs both impact the logic network performance in a different way which are elucidated in this paper.

Regarding this observation, we also implement a hybrid power-gating scenario referred to as *Header and Footer ST (HFST)*. HFST corresponds to simultaneous use of PMOS and NMOS STs which help to isolate the transistor gate terminals from electric field stress due to application of inputs during sleep mode. Fig. 1(d) shows HFST design which combines the HST and FST characteristics in this manner.

A taxonomy of these three alternatives is depicted in Fig. 2. It shows the various ST implementation features in comparison for each technique. For instance, HST and FST are influenced more by an NBTI effect or PBTI effect, respectively. Since HFST utilizes both NMOS and PMOS STs in the power-gating implementation, it suffers from both NBTI and PBTI. Furthermore, the PMOS ST channel width in HST approach should be wider to compensate for reduced carrier mobility in comparison to NMOS ST. Consequently, HST approach imposes approximately two times larger overhead to the ST. Hence, HFST approach endures 1X+2X=3X increase in overhead due to use of both PMOS and NMOS ST in its structure. PMOS ST has a reduced amount of leakage current in comparison to NMOS ST. Thus, HST design exhibits a lower leakage current than FST design. As a result, HFST takes advantage of both HST and FST in its implementation and bears a smaller amount of leakage current.

## III. EXPERIMENTAL RESULTS

To evaluate the above scenarios, the three ST arrangements are subjected to an input squarewave with a 50% duty cycle having a frequency of 1KHz or 100KHz. Each circuit is evaluated under conditions whereby it is in sleep-mode for 70% its lifetime. Consequently, the sleep transistor interrupts the path between the $V_{DD}$ and ground based on ST arrangement. Our circuit-level modeling is performed via Synopsys HSPICE reliability analysis to simulate BTI effect for the *45nm Nangate open cell library*. In order to apply aging on the inverter chain circuit, we used MOSRA model [19]. The MOSRA model is constructed with physics-based formulations and augmented with coefficient parameters, to improve the model accuracy and parameter extraction flexibility as identified in the equations below.

### A. $V_{th}$ Shift

NBTI/PBTI effects have two phases of operation depending on the bias condition of a PMOS/NMOS transistor: these are a *stress phase* and a *recovery phase*. In the stress phase, the threshold voltage ($V_{th}$) of PMOS/NMOS increases. During the recovery phase, $V_{th}$ degradation is partially recovered due to clearing of interfacial traps.

In order to calculate $V_{th}$ shift, we used the built-in model provided by MOSRA [19]. The MOSRA threshold voltage degradation model provides results which are accurate in numerous aging studies. Two principal physical mechanisms are considered in MOSRA: one is related to the contribution of the interface traps (Equation 1) and the other related to the traps inside the dielectric layer (Equation 2) which are provided here in abbreviated form. In the equations, $E(V_{GS}, V_{DS})$ denotes the strength of the electric field of the dielectrics. Regarding to the significant dependence of NBTI and PBTI on the channel length, flexible channel width- and length-dependence equations are included in the BTI model of

$$\Delta v_{TH,IT} \approx \exp\left(-\frac{E_a}{K.T}\right).\left[\frac{\varepsilon}{t_{0x}}\left(V_{gs}-V_{TH}\right)\right]^{TITCE}.\exp\left[TITFD.E\left(V_{gs},V_{da}\right)\right]t^{NIT} \quad (1)$$

$$\Delta v_{TH,OT} \approx \exp\left[-\frac{TOTFD+\frac{TOTTD}{T}}{E\left(V_{gs},V_{ds}\right)}\right]t^{NOT} \quad (2)$$


Fig 1. (a) The original circuit

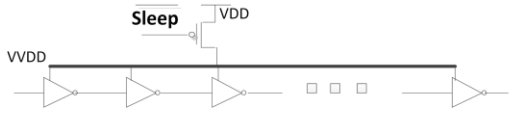


Fig 1. (b) The Header-based ST circuit

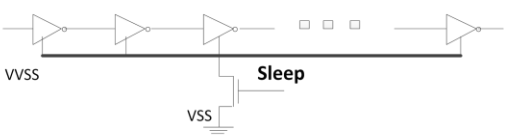


Fig 1. (c) The Footer-based ST circuit

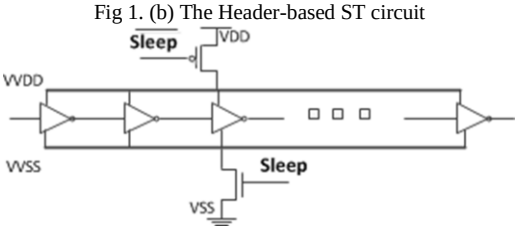


Fig 1. (d) The Header and Footer based ST circuit

MOSRA. The partial-recovery effect is modeled by taking into account the stress stimulus duty cycle. When the partial-recovery effect is considered, the total degradation becomes smaller:

$$\Delta v_{TH,AC} = TTD0.\Delta v_{TH}.\exp(-TDCD.g) \quad (3)$$

where the g quantity models the effect of duty cycle. As shown in Fig 3(a),(b) $V_{th}$ shift in the power-gated circuits is less than the baseline circuit. Moreover, $V_{th}$ shift in the baseline circuit rises rapidly over time while power-gated circuits have a rather smooth $V_{th}$ shift. The reason is that the power-gated circuits are in sleep mode 70% of the time which results in much less stress than the baseline circuit. So, during sleep mode, only the recovery phase impacts aging and decreases the aging-induced threshold voltage shift.

### *B. Delay Penalty*

Typically, sleep transistors are sized such that a tradeoff among voltage drop, leakage savings, and area overhead is obtained [6]. At the beginning of the device lifetime, addition of a ST will increase the delay. However, the delay penalty decrease as the size of the ST is increased. In this research, the ST has been chosen in a way that the increased delay of the power-gated circuits is less than 3% as compared to the delay of the baseline circuit and the leakage current is optimum. When we compare the delay of the three circuits, we find that the power-gated circuits have higher delay within 2 years as compared to the baseline, as shown in Fig. 4(a), (b). However, the power-gated circuits suffer less from aging after 2 years due to the reduced $V_{th}$ shift.

### *C. Input Vector Impact on BTI Recovery*

It has been assumed that the circuits operate all the time yet practically, not every application requires the underlying hardware to operate at highest performance level all the time. There are periods during which the circuit is not in use, but still affected by the stress induced by the electric field from the application of inputs over a path to ground. This results in the PMOS/NMOS transistors being either under stress or recovery conditions. Although power-gating of portions of the circuit which are not in use may decrease $V_{th}$ shift, although doing so does not completely recover PMOS/NMOS transistors since they are still under input stress. Fig. 5 demonstrates the comparison of $V_{th}$ shift for the first three PMOS and NMOS transistors of the Circuit Under Test (CUT) within the inverter chain. The CUT is evaluated in the HST design for 100KHz input signal. The $V_{th}$ shift for PMOS transistors is around three times greater than $V_{th}$ shift for NMOS transistors due to further impact of NBTI on PMOS transistors rather than PBTI on NMOS transistors. Moreover, as illustrated in Fig. 5, initial transistors in the CUT experience increased aging compared to subsequent

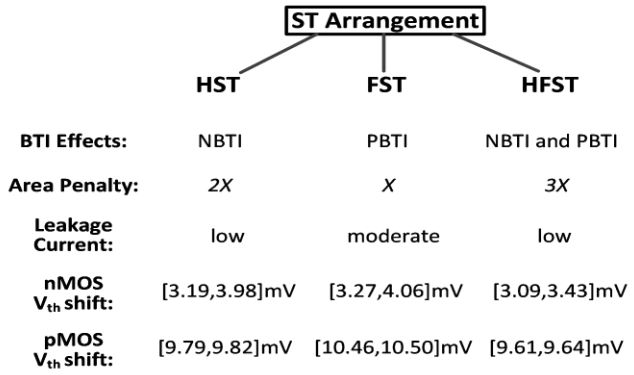


Fig 2. Taxonomy of ST Arrangements and their characteristics

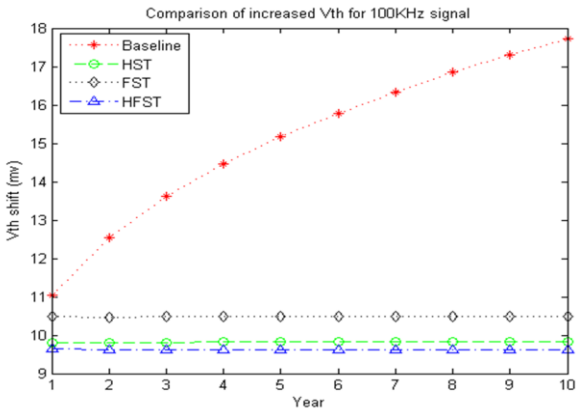


Fig 3. (a) Comparison of increased $V_{th}$ for 100KHz signal

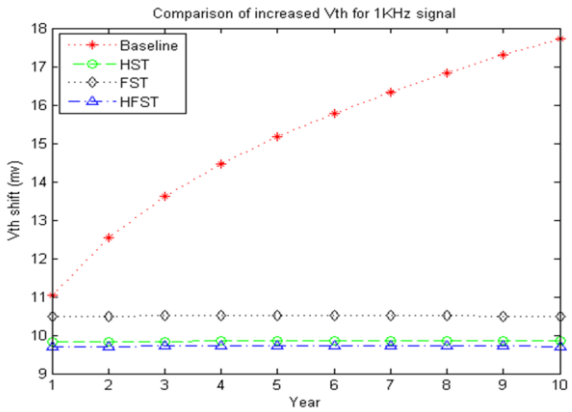


Fig 3. (b) Comparison of increased $V_{th}$ for 1KHz signal

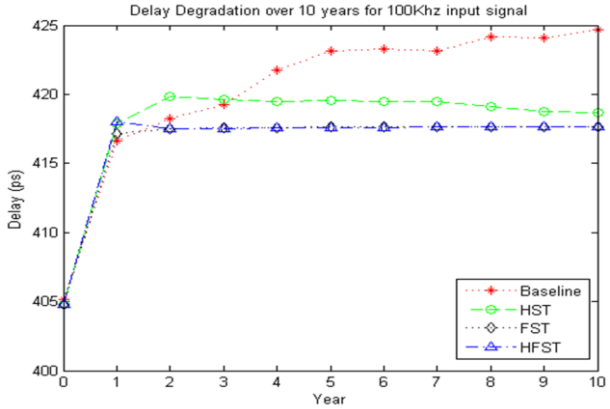


Fig 4. (a) Comparison of increased *delay* for 100KHz signal

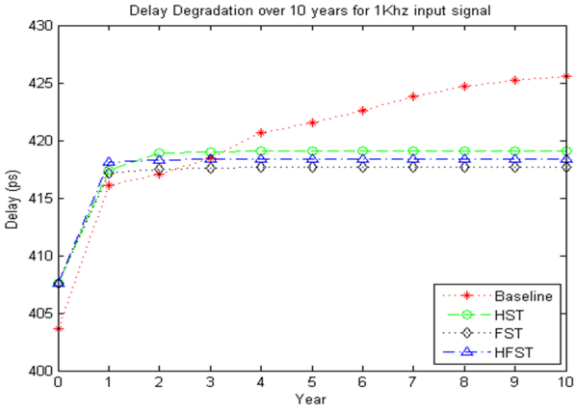


Fig. 4. (b) Comparison of increased *delay* for 1KHz signal

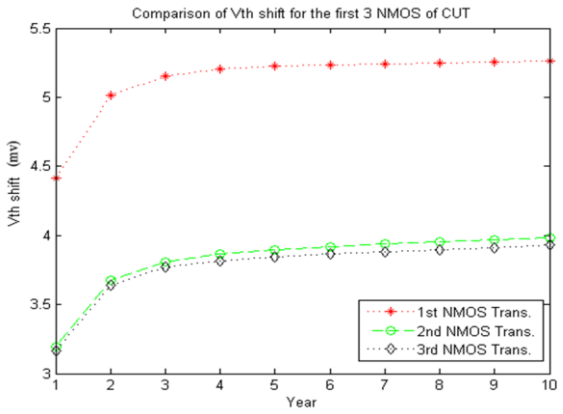


Fig 5. (a) Comparison of $V_{th}$ *shift* for the first 3 NMOS of CUT

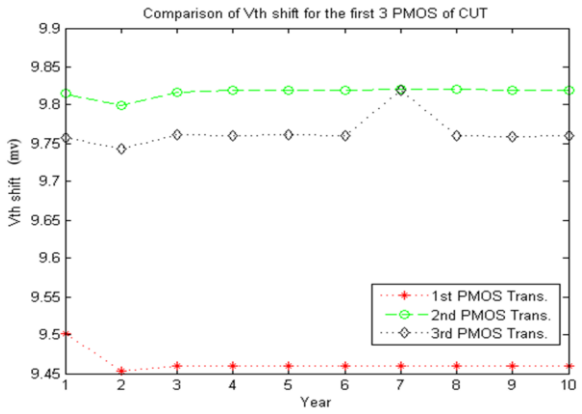


Fig 5. (b) Comparison of $V_{th}$ *shift* for the first 3 PMOS of CUT

transistors, depending on if the circuit is in the sleep mode.

## IV. Analysis and Conclusions

Table I shows the comparison of the delay degradation for the circuit which is equipped with different ST arrangements. The delay degradation is between 3.14% and 3.72% for all circuits within the first 2 years of their lifetime which indicates that all arrangements are seen to degrade at similar rates. However, the power-gated circuits suffer less from the aging effect since they benefit from the less $V_{th}$ shift after two years. As a result, the delay penalty of the power-gated circuits reduce over time.

Table II demonstrates power consumption comparison with 100KHz input vector. The baseline circuit is influenced further by the aging effect over time which results in higher $V_{th}$ shift which reduces the leakage current. Consequently, the trends of power consumption for the baseline circuit shift more than other methods which have relatively constant power consumption. In conclusion, it is observed that:

- FST arrangements can be preferred to minimize degradation of delay based on Figure 4(a),(b),
- HFST arrangements are seen to incur increased power consumption according to Table II and more area penalty according to Figure 2, yet Figure 3 and Figure 4 shows HFST performs comparably to FST in terms of both $V_{th}$ shift and delay degradation according to Table I,
- The impact of the electric field between inputs and ground is not a significant influence on aging degradation between Figure 5(a),(b),
- HFST arrangements are seen to only slightly reduce ST $V_{th}$ shift compared to HST in Figure 3(a)(b),
- Based on Figure 2, since HST has less leakage then the benefit of HFST may not be justified, and
- Area penalty of FST may provide a practical advantage for manufacturing layout while having less aging due to decreased impact of PBTI compared to NBTI.

TABLE I. DELAY DEGRADATION COMPARISON (% BASELINE)

| Time / Method | 2 years (%) | 4 years (%) | 6 years (%) | 8 years (%) | 10 years (%) |
|---|---|---|---|---|---|
| **Baseline** | 3.22 | 4.10 | 4.48 | 4.69 | 4.81 |
| **HST** | 3.72 | 3.62 | 3.64 | 3.54 | 3.44 |
| **FST** | 3.14 | 3.17 | 3.18 | 3.18 | 3.18 |
| **HFST** | 3.14 | 3.16 | 3.16 | 3.17 | 3.18 |

TABLE II. POWER CONSUMPTION COMPARISON (IN WATTS)

| Time / Method | 2 years | 4 years | 6 years | 8 years | 10 years |
|---|---|---|---|---|---|
| **Baseline** | 6.64E-07 | 6.54E-07 | 6.47E-07 | 6.43E-07 | 6.41E-07 |
| **HST** | 6.81E-07 | 6.79E-07 | 6.79E-07 | 6.79E-07 | 6.78E-07 |
| **FST** | 6.73E-07 | 6.72E-07 | 6.72E-07 | 6.72E-07 | 6.71E-07 |
| **HFST** | 6.82E-07 | 6.82E-07 | 6.82E-07 | 6.82E-07 | 6.81E-07 |

## References


[1] X. Chen, et. al., "Variation-aware Supply Voltage Assignment for Minimizing Circuit Degradation and Leakage," *ISLPED*, 2009.

[2] K. Kang, et. al, "Estimation of Statistical Variation in Temporal NBTI Degradation and its Impact on Lifetime Circuit Performance," *ICCAD*, 2007.

[3] S. Kumar, C. Kim, and S. Sapatnekar, "Impact of NBTI on SRAM Read Stability and Design for Reliability," *ISQED*, pp. 210–218, 2006.

[4] S. Kumar, et. al. "Adaptive Techniques for Overcoming Performance Degradation due to Aging in Digital Circuits," *ASPDAC*, 2009.

[5] J. Abella, X. Vera and A. Gonzalez, "Penelope: The NBTI-aware Processor," *MICRO 40*, pp. 85–96, 2007.

[6] A Calimera, et. al. "NBTI-aware Power-gating for Concurrent Leakage and Aging Optimization," *ISLPED*, pp. 127–132, 2009.

[7] U. Karpuzcu, et. al., "The Bubble Wrap Many-core: Popping Cores for Sequential Acceleration," *MICRO 42*, pp. 447–458, 2009.

[8] T. Siddiqua, S. Gurumurthi, "A Multi-level Approach to Reduce the Impact of NBTI on Processor Functional Units," *GLSVLSI*, 2010.

[9] J. Srinivasan, S. Adve, P. Bose, and J. Rivers, "The Case for Lifetime Reliability-aware Microprocessors" *ISCA*, pp. *276*, 2004.

[10] J. Srinivasan, S. Adve, P. Bose, and J. Rivers, "Lifetime Reliability: Toward an Architectural Solution," *IEEE MICRO*, Vol. 25, No. 3, 2005.

[11] A. Tiwari and J. Torrellas, "Facelift: Hiding and Slowing Down Aging in Multicores," *MICRO 41*, pp. 129–140, 2008.

[12] S. Gupta and S. Sapatnekar, "Employing Circadian Rhythms to Enhance Power and Reliability," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 18, No. 3, pp. 1-23, 2013.

[13] F. Oboril and M. B. Tahoori, "ExtraTime: Modeling and analysis of wearout due to transistor aging at microarchitecture-level," *DSN*, 2012.

[14] T. B. Chan, J. Sartori, P. Gupta and R. Kumar,"On the efficacy of NBTI mitigation techniques," in *Proceedings of Design, Automation Test in Europe Conference Exhibition (DATE)*, pp. 1-6, 2011.

[15] A Calimera, E. Macii and M. Poncino, "NBTI-aware Sleep Transistor Design for Reliable Power-gating," *GLSVLSI*, pp. 333-338, 2009.

[16] K. Wu, et. al., "Analysis and Mitigation of NBTI-Induced Performance Degradaiton for Power-Gated Circuits" *ISLPED*, pp. 139-144, 2011.

[17] L. Luchuan and H. Mahmoodi "Evaluation of Power-gating under transistor aging effect issues in 22nm CMOS technology," *MIXDES*, pp. 477-481, 2010.

[18] M. Denais, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, N. Revil and A. Bravaix, "Interface trap generation and hole trapping under NBTI and PBTI in advanced CMOS technology with a 2-nm gate oxide," *TDMR* , vol. 4, no. 4, pp.715-722, 2004.

[19] B. Tudor, W. Joddy, L. Weidong and H. Elhak "MOS Device Aging Analysis with HSPICE and CustomSim" Synopsys, Tech. Rep., 2011.