HIGH THROUGHPUT POWER-AWARE FIR FILTER DESIGN BASED ON FINE-GRAIN PIPELINING MULTIPLIERS AND ADDERS

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ABSTRACT

In regular FIR structure, by pipelining the multipliers one can improve the throughput. But as the growth of operand word length, the delay in addition process becomes another important constraint. In this paper, a novel fine-grain pipelining scheme for high throughput FIR is proposed. By pipelining multipliers and adders, very high throughput can be achieved. 2-Dimensional pipeline gating technique is used to make the designed FIR power aware to the precision of the operands. The average power dissipation and latency are both significantly reduced with changing of input precisions.

1. INTRODUCTION

With the growing demand on battery-powered mobile computing and communication devices, how to achieve lower power dissipation in order to extend battery life becomes a major concern of IC designers. Digital signal processing (DSP) systems are widely used in computing and communication area. Finite impulse response (FIR) filter is one of the basic elements in DSP applications. Design low power, high throughput FIR is a hot topic in DSP research area. In recent years varies techniques for high throughput, low power FIR design have been proposed [1-2]. Bhardwaj et al., [3] introduced a new measurement, power-awareness, to indicate the ability of the system energy to scale with changing conditions and quality requirements. Scalability is an important figure-of-merit since it allows the end user to implement operational policy.

In this paper, a novel method to design high throughput power-aware FIR filter is proposed. Based on pipelining multipliers and adders, very high throughput can be achieved. To lower power dissipation and reduce latency, 2-Dimensional pipeline gating technique is applied to improve the power-awareness of the designed FIR filter.

2. HIGH THROUGHPUT FIR FILTER DESIGN BY PIPELINING MULTIPLIERS AND ADDERS

To shorten the critical path in order to achieve high throughput, Data-Broadcast structure is used in this paper [4]. To improve the throughput of the FIR filter, one commonly used method is to pipeline the multipliers. Since the multiplication time T_M is usually much larger than the addition time T_A, much shorter critical path length can be achieved by carefully balancing the pipeline stages. Figure 1 shows a pipelining scheme for FIR filter.

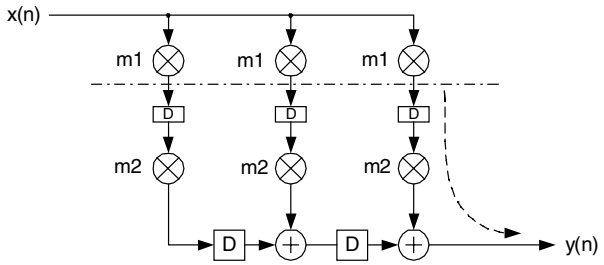

Fig. 1. Improve throughput by pipelining multipliers

By pipelining multipliers can only achieve limited throughput improvement because the shortest critical path length can be achieved is T_A. In recent years, the word length of FIR filter has been growing up to 64-bit. Under long word length condition, addition also takes significant time. To further improve throughput of FIR filters, the critical path in addition process needs to be shortened also. So adders, as well as multipliers, need to be pipelined. Unlike pipelining multipliers, which doesn't change the relative timing sequence between adder inputs, pipelining adders just likes adding delay elements to the paths between adders. This will change the timing difference of the two inputs of the next adder from one clock cycle to more than one clock cycle, thus causes the incorrect output results.

To solve this problem, additional delay elements are added between next adder and its corresponding multiplier. The goal is to maintain the timing difference between the two inputs of the adder as one clock cycle. The revised FIR filter structure is shown in Figure 2.

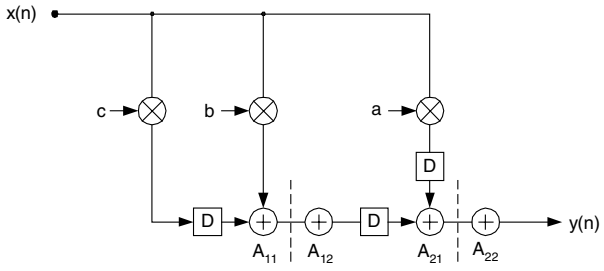

Fig. 2. Revised adder pipelining scheme

Along with the achieved high throughput, pipelining both multipliers and adders also causes two problems. Firstly the power dissipation will become larger because some registers are added between the pipeline stages; secondly the total latency from the input to output also becomes larger because

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the pipelined addition paths are longer. To reduce power dissipation and pipeline latency in the FIR filter structure shown in Figure 2, since in most cases, the precisions of input data and coefficients are shorter than the designed calculation length, the average power dissipation can be saved by improving power awareness. As shown later in this section, the technique used to improve power awareness of the FIR filter also reduces pipeline latency.

Boolean designs have natural power awareness to the changing of input precision. But in fine-grain pipelined designs, the number of registers is much larger than that of other elements. The switching power caused by clock in registers is the major part of power dissipation. So the power dissipation in fine-grain pipelined circuit is nearly stable under different input precisions. Suhwan et al., [5] introduced a clock gating method to design reconfigurable multiplier. This technique can be described as 1-D pipeline gating because it only considers gating clocks to unnecessary stages along the data flow direction. Di et al., [6] proposed a 2-D pipeline gating technique to improve the power awareness in pipelined signed multipliers. The basic idea of this technique is to selectively gate the clocks to the registers in both vertical direction (the data flow direction, as in 1-D gating technique) and horizontal direction (within each pipeline stage). This 2-D technique is able to greatly enhance the power awareness in pipelined circuits and reduce pipeline latency. Moreover, Di et al., [6] also proposed a method avoid the sign extension problem to design run-time reconfigurable signed multiplier. This selective method and the 2-D gating technique together are used in this paper to improve the power awareness and reduce latency of the FIR filter.

3. RESULTS AND ANALYSIS

Based on the structure in Figure 2, three implementations of 4-tap 16-bit FIR, including the original pipelined filter, the filter applying 1-D technique, and the filter applying 2-D technique, are designed and tested. These designs are synthesized by Synopsys Design Compiler and then simulated in Powermill.

The throughput of the pipeline is determined by the slowest stage. Since both multipliers and adders are fine-grain pipelined, the delay in each pipeline stage is very small. The technology used in synthesis process is 0.24μm static CMOS logic. Simulation results show that the designed FIR filter is able to work under 1.25GHz clock rate.

Figure 3 shows the average power dissipation of the designed FIR filters. From Figure 3 several conclusions can be made:

First, 2-D gating technique has great advantage over 1-D technique in terms of power saving. There are two reasons: one is that 2-D technique not only gates the redundant pipeline stages like 1-D technique does, but also disables the unused registers within the useful pipeline stages. So the total number of switching is further reduced. The other reason is the use of sign extension brings more switching to 1-D multipliers and adders. But the run-time reconfigurable multipliers and adders using 2-D gating do not have this problem. These two reasons combine together to make the 1-D curve look like convex functions while the 2-D curve looks like concave functions.

Second, the power overheads of the filter using 2-D technique is very small, less than 2% compared to the original design.

Last, the average power saving of the filter using 1-D technique is 22.7% compared to the original design under equal input precision probabilities. But the filter using 2-D technique has a power saving of 62.5% over original design and 51.4% over the design using 1-D technique.

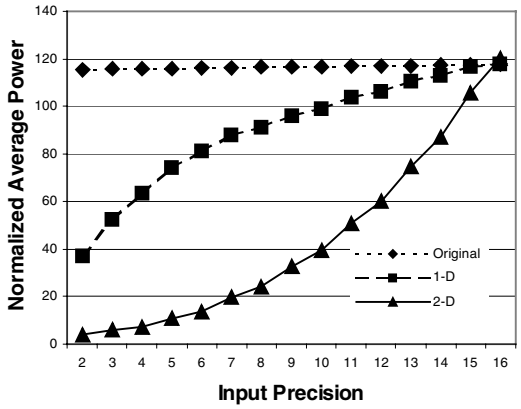

Fig. 3 Average power dissipation of the designed FIR filters

4. CONCLUSION

A novel design technique to overcome the throughput limit in FIR filters is proposed. This technique fine-grain pipelines both multipliers and adders in FIR structure to achieve very high throughput. Two-dimensional pipeline gating technique is applied to improve the power awareness of the designed FIR filter and reduce the overall latency.

5. REFERENCES

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