Ronald F. DeMara

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I. Technical Interests

Emerging Device Computer Architectures; Reconfigurable Logic Devices; Resilient and Energy-aware Logic Design; Evolvable and Intelligent Hardware; Digitization and Personalization of STEM Learning

II. Education

- Doctor of Philosophy – Computer Engineering
  University of Southern California – December, 1992
  Dissertation: *Parallelism, Design, and Performance of a Marker-Propagation Reasoning Architecture*
- Master of Science – Electrical Engineering
  University of Maryland, College Park – May, 1989
  Emphasis: Digital Computer Systems
- Bachelor of Science – Electrical Engineering with High Honors
  Lehigh University – May, 1987
  Minor: Science, Technology, and Society

III. Professional Experience

1993 – present: University of Central Florida – Orlando, Florida

Department of Electrical Engineering and Computer Science

– *Professor*: 2006 – present
– *Program Coordinator*, Computer Engineering Program: 1994 – 1995, 2011 – 2015
– *Graduate Coordinator:* December 2009 – August 2012
– *Associate Professor*: 1999 – 2005
– *Assistant Professor*: 1993 – 1998

Taught 14 courses, developed 10 new courses, and served as Program Coordinator. Principal Investigator (PI) or co-PI of research totaling $7.2M of which roughly two-thirds was federally-sponsored including the *National Science Foundation*, *NASA*, *U.S. Army / Navy / Air Force*, *Defense Modeling and Simulation Office*, *DARPA*, and *National Security Agency*. Completed 17 Doctoral graduates and 26 Masters graduates with thesis as Advisor. Eight of these graduates went on to full-

time faculty positions in academic programs at the university level, of which one is ECE Department Chair, and another is Dean of a College of Science, Engineering, and Mathematics.

Performed program administration in Computer Engineering at the undergraduate and graduate levels, laboratory enhancement within the department and the college, and academic committee service at the department-level through the university-level. Conducted accreditation activities and strategic planning for the Computer Engineering program. Active in junior faculty mentoring and program development including chairing faculty recruiting committees resulting in the hiring of tenure-track faculty, lecturers, and staff. Service in professional societies through peer review of many technical journal and conference venues, member rank elevation committees, and as a faculty advisor to student groups.

Served as member of the University Graduate Council and the Faculty Senate. Served on Editorial Boards of four journals. Held officer positions in Southeast Section of American Society for Engineering Education. Hold a joint appointment in the Computer Science program for coursework and doctoral advising.

Received the *Outstanding Engineering Educator Award (IEEE Southeastern US Region level and Florida Council level), Research Initiation Award (University-level), Distinguished Research Lecturer Award (College of Engineering), Advisor of the Year Award (College of Engineering), Excellence in Graduate Teaching Award (ECE Department),* twice received the *Researcher of the Year Award (ECE Department),* and received the *State of Florida University System's Teaching Initiative Award (State-level/University-level)* three times.

2002: NASA Ames Research Laboratory – Mountain View, CA (UCF Sabbatical Period)

Visiting Research Scientist, Evolvable Hardware Program

Conducted research in Autonomous FPGA Repair techniques. Developed evolutionary computation approaches using Genetic Algorithms to regain lost functionality due to stuck-at-faults and other permanent failures in Xilinx SRAM FPGA platforms. Contributed to three conference papers on the topic, including technical approach, experimental system, and research results.

1989 – 1992: University of Southern California – Los Angeles, California

Research Assistant III, Department of Electrical Engineering-Systems

Conducted research in High Performance Computer Architectures for Knowledge Processing applications. Developed the SNAP-1 Multiprocessor, a 144-CPU DSP system for real-time speaker-independent continuous speech processing, including processor configuration, interconnection network, and performance monitoring strategy. Research in performance modeling and assessment of hybrid SIMD/MIMD architectures.

1986 – 1989: IBM Corporation – Manassas, Virginia

Associate Engineer, Federal and Complex Systems Division

Specification, design, and capacity analysis of telecommunication systems. Responsibilities included performance modeling using SIMSCRIPT/NETWORK-II.5, processor selection, connection topology, redundancy/availability analysis, and technical proposal development. Lead systems architect for fly-by-wire Automated Inventory Management system. Site representative to IBM division-level steering committee on systems engineering workstation environments.

IV. Teaching Activities

A. Teaching Summary

Taught 14 courses, including development of 10 new courses added to the catalog, and served as Computer Engineering degree Program Coordinator. Active in developing STEM curricula with educational contributions and publications regarding:

- **s**ustainable curriculum renewal in STEM,
- flipped classroom pedagogies and tools,
- integration of STEM research and teaching,
- digitization of STEM assessments,
- remediation with Socratic video blog**s.**
- innovations in remediation and tutoring, and
- individualized, adaptive, and personalized learning pedagogies.

B. Courses Taught

Taught courses in lecture, recitation, and seminar-style formats at Undergraduate (EEL3xxx/4xxx) and Graduate (EEL5xxx/6xxx) levels with [class size] as listed:

1. EEL3801: *Computer Organization* [70]
   – ALU, control path, memory design, instruction set architectures, assembly lang.
2. EEL4767: *Computer System Design I with Laboratory* [40]
   – Computer Organization, Microprocessor Systems
3. EEL4768: *Computer System Design II with Laboratory* [30]
   – Computer Architecture, Data Path Design
4. EEL4851: *Engineering Data Structures with Laboratory* [50]
   – Data Structures and Algorithms in C++ and now Java
5. EEL4882: *Engineering Systems Software* [30]
   – Operating Systems Concepts, Process Scheduling, Resource Management
   – offered in live-only and live-with-web-based formats
6. EEL4817: *Machine Learning I* [15]
   – Decision Trees, Evolvable Hardware, Neural Networks
   – Team taught with 3 faculty: taught module on Evolvable Hardware
7. EEL4818: *Machine Learning II* [10]
   – Honors course for undergraduates developing Machine Learning projects
   – Team taught with 3 faculty: supervised autonomous FPGA projects
8. EEL5708: *High Performance Computer Architecture* [40]
   – Pipelining/Branch Prediction, Superscalar Architecture, Cache Design
   – offered in live-only and live-with-remote-video plus web-based formats
9. EEL5706: *Resilient Computer Systems Design* [15]
   – Fault Classification, Redundancy, Failure Rate Analysis, Checkpointing
   – added to graduate course catalog
10. EEL6361: *Emerging Device Computing Architectures* [15]
    – Logic-In-Memory and non-Boolean computing approaches. System design
    – added to graduate course catalog
11. EEL6707: *Parallel Processing* [20]
    – Distributed/Shared Memory, Interconnection Networks, Data Transformations
    – offered in live-only and live-with-remote-video plus web-based formats

12. EEL6763a: *Current Topics - Scalable Shared-Memory Architectures* [20]
    – Data Consistency, Cache Coherence, Profiling and Metrics
    – offered in live-with-remote-video format
13. EEL6763b: *Current Topics - Clockless Processor Design* [20]
    – Asynchronous ALU Design, Fine-grained and Coarse-grained Dataflow
14. EEL6763c: *Current Topics - Autonomously Reconfigurable and Evolvable Hardware* [20]
    \ECM6308 – FPGA-based Intrinsic/Extrinsic Evolution, Autonomous Regeneration
    – offered in live-with-remote-video plus web-based format
15. EEL6721: *Evovable Hardware* [15]
    – Evolvable digital and analog computing hardware, autonomous architectures,
    – added to graduate course catalog

16. EEL6769: *Parallel Knowledge Processing* [15]
    – Marker-propagation Architectures, Classifier Systems, Genetic Algorithms
    – added to graduate course catalog

Revised material, supervised, and/or substitute-taught three additional courses:

17. EEL3342: *Digital Logic Design with Laboratory* [60]
    – Boolean Logic, Combinational and Sequential Circuits
18. EEL4781: *Computer Networks* [30]
    – Protocols, Routing Algorithms, OSI Model, Flow Control
19. EEL5762: *Computer Systems Performance Analysis* [20]
    – Stochastic Modeling, Discrete Event Simul., Appl. to Networks/ Multiprocessors

C. Curriculum Enhancement

- University Course Catalog additions:
  - EEL4882: Systems Software
  - EEL5708: High Performance Computer Architecture
  - EEL5762: Computer System Performance Analysis
  - EEL5706: Resilient Computer System Design
  - EEL6707: Parallel Processing
  - EEL6763/ECM6308: Current Topics in Parallel Processing
  - EEE 6721: Evolvable Hardware
  - EEL6361: Emerging Device Computing Architectures
  - EEL6769: Parallel Knowledge Processing
  - and also assisted in the development of EEL4817 and EEL4818 (Machine Learning I and II)
- Curriculum development to support Bachelors degree program in Information Technology and degree program tracks in Computer Engineering
- Evaluation and Proficiency Center (EPC)
  - Founding Director at department scale and expanded college scale
  - Obtained $275,000 in Technology Fee Grant as PI. Resources include testing center facilities, laptops, tablets, and vlogging stations for tutoring
  - Administer $300,000 IT Performance Fund allocation for College of Engineering and Computer Science Expansion

- Directed ten faculty, five Ph.D. students, and the manager staff spanning both pedagogical research and delivery aspects for STEM innovation of ten undergraduate courses.

- Digitizing and Remediating STEM Assessments
  - Created and offered 6-week Faculty Development Workshop to 10 Engineering faculty to digitize their assessments
- Laboratory Development:
  - Obtained $520,150 in laboratory infrastructure grants as PI or Co-PI. Resources include network servers, workstations, 8-way shared-memory multiprocessor, scopes, and analyzers
  - Founder and Director: Computer Architecture Lab
  - Co-developed or renovated: Microprocessor Lab, Open Computing Lab, Intelligent Systems Lab, and VLSI Lab
  - Directed integration of National Instrument's Labview PC-based virtual instrumentation breadboard environment into 2 undergraduate laboratories: EEL3342 and EEL4767
  - Mentoring of student assistants for laboratory manual revision and web-based hosting
- Assessment and Accreditation:
  - Accreditation Coordinator for Accreditation Board for Engineering and Technology (ABET) for Computer Engineering program: 2008
  - Initiated the Southern Association of Colleges and Schools (SACS) Outcomes Assessment methods in UCF Computer Engineering program and maintained Evaluation Matrices
  - ABET lab coordinator and course custodian on multiple occasions
- Co-PI of NSF Combined Research Curriculum Development (CRCD) grant:

  Title: *Machine Learning Advances for Engineering Education*
  Amount: $416,851 plus $165,077 additional university match for a total of $581,928
  Duration: June 2002 – August 2007
  - Co-developed Machine Learning modules that have been taught them to 243 students in 8 undergraduate classes.
  - Modules motivate students to take senior-level course sequence entitled *Machine Learning I* and *II* that have been taught to 34 students.
  - Project has produced approximately 20 undergraduate research projects, three Masters with thesis, 1 Ph.D., 14 conference papers (8 technically-oriented venues and 6 educationally-oriented venues), and 3 journal papers.

D. Ph.D. Students Completed

Completed 17 Ph.D. students as Dissertation Chair or Co-Chair:

1. Yu Bai, *Stochastic-Based Computing with Emerging Spin-Based Device Technologies*, Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2016. (Dissertation Co-chair)

   – Dr. Bai became a faculty member at California State University at Fullerton.

2. Ahmad Al-Zahrani, *Fast Online Diagnosis and Recovery of Reconfigurable Logic Fabrics using Design Disjunction*, Doctor of Philosophy, Computer Engineering, University of Central Florida, December, 2015. (Dissertation Chair)

– Dr. Al-Zahrani became a faculty member at Umm Al Qura University.

3. Rizwan A. Ashraf, *Adaptive Architectural Strategies for Resilient Energy-Aware Computing*, Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2015. (Dissertation Chair)

   – Dr. Ashraf joined Oak Ridge National Laboratory.

4. Naveed Imran, *Autonomous Recovery Of Reconfigurable Logic Devices Using Priority Escalation Of Slack*, Doctor of Philosophy, Electrical Engineering, University of Central Florida, December, 2013. (Dissertation Chair)

   – Dr. Imran became a Technical Staff member at AMD, Inc.

5. Rashad Oreifej, *A Sustainable Autonomic Architecture for Organically Reconfigurable Computing Systems*, Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2011. (Dissertation Chair)

   – Dr. Oreifej is a Senior Technical Staff at Qualcomm, Inc.

6. Rawad Al-Haddad, *An Adaptive Modular Redundancy Technique To Self-Regulate Availability, Area, And Energy Consumption In Mission-Critical Applications*, Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2011. (Dissertation Chair)

   – Dr. Al-Haddad is a Senior Hardware Engineer at Apple, Inc.

7. Juan Carlos Leon-Barth, *Phoneme-Based Video Indexing Using Phonetic Disparity Search*, Doctor of Philosophy, Computer Engineering, University of Central Florida, December, 2010. (Dissertation Chair)

   – Dr. Leon-Barth became a Research Scientist at L3 Communications.

8. Kening Zhang, *A Competitive Reconfiguration Approach to Autonomous Fault Handling Using Genetic Algorithms,* Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2008. (Dissertation Chair)

   – Dr. Zhang became a research scientist at Baidu.

9. Carthik A. Sharma, *Sustainable Fault-Handling of Reconfigurable Logic using Throughput-Driven Assessment*, Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2008. (Dissertation Chair)

   – Dr. Sharma is an Instructor at Puppet Labs in Portland, OR.

10. Heng Tan, *A Multi-layer Field Programmable Gate Array Framework Supporting Autonomous Partial Runtime Reconfiguration*, Doctor of Philosophy, Computer Engineering, University of Central Florida, December, 2007. (Dissertation Chair)

    – Dr. Tan became Senior Digital Hardware Engineer/Project Group Leader at xG Technology, Inc. in Fort Lauderdale, FL.

11. Hubert A. Bahr II, *Bandwidth Reduction Techniques for Embedded Simulation Using Concurrent Behavior Models*, Doctor of Philosophy, Computer Engineering, University of Central Florida, December, 2004. (Dissertation Chair)

    – Dr. Bahr became an Assistant Professor at TAMU Central Texas, and is now retired.

12. Juan J. Vargas, *Data Transmission Scheduling for Distributed Simulation Using Packet Alloying*, Doctor of Philosophy, Computer Engineering, University of Central Florida, December, 2004. (Dissertation Chair)
    – Dr. Vargas is a tenured faculty member at the University of Costa Rica.

13. Adam J. Rocke, *Mitigation of Network Tampering Through Dynamic Dispatch of Mobile Agents*, Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2004. (Dissertation Chair)
    – Dr. Rocke is faculty member at Seminole State College.

14. Scott C. Smith, *Gate and Throughput Optimization of NULL Convention Digital Circuits*, Doctor of Philosophy, Computer Engineering, University of Central Florida, May, 2001. (Dissertation Chair)
    – Dr. Smith is Professor and ECE Department Chair at the North Dakota State University.

15. Yili Tseng, *High Performance Termination Detection Techniques Supporting Multithreaded Execution*, Doctor of Philosophy, Computer Engineering, University of Central Florida, December, 2000. (Dissertation Chair)
    – Dr. Tseng is Associate Professor at Rivier College.

16. Yousef Ma, *Localized Adaptive Networks for Hybrid Symbolic and Subsymbolic Processing*, Doctor of Philosophy, Computer Engineering, University of Central Florida, August, 2000. (Dissertation Chair)
    – Dr. Ma formed and operated his own computing consulting company.

17. Bahman S. Motlagh, *A Concurrent-Read Exclusive-Write Architecture for Scalable Shared-Memory Multiprocessing*, Doctor of Philosophy, Computer Engineering, University of Central Florida, May, 1997. (Dissertation Chair)
    – Dr. Motlagh is Associate Professor at Daytona State College.

E. M.S. Thesis Students Completed

Completed 26 M.S. students as Thesis Chair and Advisor:

1. Soheil Salehi, *Towards Energy-Efficient And Reliable Computing: From Highly Scaled CMOS Devices To Resistive Memories*, Master of Science, Computer Engineering, University of Central Florida, December, 2016.
   – Graduate pursued doctoral studies.

2. Navid Khoshavi, *Reactive Rejuvenation of CMOS Logic Paths Using Self-Activating Voltage Domains*, Master of Science, Computer Engineering, University of Central Florida, August, 2016.
   – Graduate pursued doctoral studies.

3. Mohan Krishna Gopi Krishna, *Energy-Aware Reconfigurable Logic Devices Using Spin-Based Storage and Carbon Nanotube Switching*, Master of Science, Computer Engineering, University of Central Florida, May, 2016.
   – Graduate accepted full-time industrial employment.

4. Steven D. Pyle, *Self-Scaling Evolution of Analog Computation Circuits with Digital Accuracy Refinement*, Master of Science, Electrical Engineering, University of Central Florida, August, 2015.
   – Graduate pursued doctoral study at UCF.

5. Adnan Aquib Naseer, *Assessing Approximate Arithmetic Designs In The Presence Of Process Variations and Voltage Scaling*, Master of Science, Computer Engineering, University of Central Florida, May, 2015.
   – Graduate hired by Deloitte.

6. Vignesh Thangavel, *Cascaded Digital Refinement for Intrinsic Evolvable Hardware*, Master of Science, Electrical Engineering, University of Central Florida, May, 2015.

7. Matthew Parris, *Optimizing Dynamic Logic Realizations For Partial Reconfiguration Of Field Programmable Gate Arrays*, Master of Science, Computer Engineering, University of Central Florida, May, 2009.
   – Graduate is Avionics Design Lead at NASA Kennedy Space Center.

8. Raul Dookhoo, *Automated Construction and Testing of Dialog Scripts*, Master of Science, Computer Science, University of Central Florida, December, 2008.
   – Graduate joined industry at a software consulting company.

9. Guantong Wang, *Mobile Agent File Integrity Analyzer*, Master of Science, Computer Engineering, University of Central Florida, May, 2001.
   – Graduate started and operates his own company.

10. Dong Lin, *Identification of Similar, Conflicting, and Redundant Entries in Distributed Databases*, Master of Science, Computer Engineering, University of Central Florida, May, 2001.
    – Graduate hired by technology start-up company in San Jose, California.

11. Lu Wang, *Automated Generation of XML Schemas using a Transportation Interchange Language*, Master of Science, Computer Engineering, University of Central Florida, May, 2001.
    – Graduate hired by Oracle Corporation in Orlando, Florida.

12. Bharat Kapoor, *Remote Misuse Detection Using Mobile Agents and Relational Database Query Techniques*, Master of Science, Computer Engineering, University of Central Florida, May, 2000.
    – Graduate hired by Motorola Corporation in Minneapolis, Minnesota.

13. Yong Zhu, *Decentralized Control Schemes for Coordinating Distributed Processing Activities of Mobile Software Agents*, Master of Science, Computer Engineering, University of Central Florida, May, 2000.
    – Graduate hired by AT&T in Santa Clara, California.

14. Jie Lu, *Time-Type Mobile Agent Protocols for Distributed Detection of Network Intrusions*, Master of Science, Computer Engineering, University of Central Florida, May, 2000.
    – Graduate hired by Ingenix, Inc in Hartford, Connecticut.

15. Juan Carlos Leon-Barth, *Forced-Miss Data Referencing Methods for Benchmarking Multiprocessor Memory Hierarchies*, Master of Science, Computer Engineering, University of Central Florida, August, 1998.
    – Graduate hired by IBM Corporation.

16. David Hammer, *High Performance Multiprocessing with Read-time Resolution Data Coherent Strategies*, Master of Science, Computer Engineering, University of Central Florida, August, 1996.
    – Graduate hired by General Dynamics in Buffalo, New York.

17. Paul J. Wilder, *N-ary Cube Interconnection using Multiport Memories*, Master of Science, Computer Engineering, University of Central Florida, May, 1996.
    – Graduate is the Dean of the College of Science, Engineering, and Mathematics, Vincennes University, Vincennes, IN.

18. Benito Rosada, *Concurrent Read Replicated Multiprocessor Systems*, Master of Science, Computer Engineering, University of Central Florida, December, 1995.
    – Graduate hired as lecturer in Dominican Academy in Brookyln, New York.

19. He Zhu, *Rate-Adaptive Source Quench Schemes in Congestion Avoidance Techniques – Performance Bound and Simulation Evaluation*, Master of Science, Computer Engineering, University of Central Florida, December, 1995.
    – Graduate hired by technology start-up company in San Jose, California.

20. Shrikanth Sripathi, *High Performance Classifier Systems on SIMD Architectures*, Master of Science, Computer Engineering, University of Central Florida, December, 1995.
    – Graduate hired by Siemens Corporation in St. Paul, Minnesota.

21. Kenneth A. Drake, *Time and Space Efficient Multiprocessor Synchronization and Quiescence Detection*, Master of Science, Computer Engineering, University of Central Florida, May, 1995.
    – Graduate employed at Lockheed Martin Information Systems in Orlando, Florida.

22. Scott E. Crawford, *Cache Coherence Strategies for Multiported Shared-Memory Architectures*, Master of Science, Computer Engineering, University of Central Florida, December, 1994.
    – Graduate hired by General Motors in Detroit, Michigan.

23. Hubert A. Bahr II, *Distribution-Adaptive Priority Queue Scheduling Algorithms for Discrete Event Simulation*, Master of Science, Computer Engineering, University of Central Florida, December, 1994.
    – Graduate was employed at STRICOM in Orlando, Florida.

24. Robert A. Cagle, *Content Addressable Memory with Built-in Marker-Passing Functions*, Master of Science, Computer Engineering, University of Central Florida, May, 1994.
    – Graduate hired by Honeywell in Clearwater, Florida.

25. Richard N. Mercer, *Incremental Boolean Logic Techniques for Nanometer-Scale Computing Devices*, Master of Science, Computer Engineering, University of Central Florida, May, 1994.
    – Graduate hired by Oracle Corporation in Orlando, Florida.

26. Niraj Shah, *Rate-Adaptive Source Quench Congestion Avoidance Technique for TCP and UDP Protocols*, Master of Science, Computer Engineering, University of Central Florida, May, 1994.
    – Graduate hired by AT&T in Boston, Massachusetts.

F. Honors Thesis Students Completed

Completed two undergraduate Honors Thesis students who have pursued graduate degrees:

1. Corey K. Milliord, *Voting Schemes to Enhance the Performance of Evolutionary Repair in Reconfigurable Logic Devices*, Honors Thesis, Bachelor of Science, Computer Engineering, University of Central Florida, May, 2005.
   – Student entered graduate program at Columbia University.
2. Kirk Carter, *An AI Performance Benchmark for the n-Cube-*2, Honors Thesis, Bachelor of Science, Computer Engineering, University of Central Florida, Fall, 1993.
   – Student entered graduate program at Georgia Institute of Technology.

G. Undergraduate Research Students Completed

1. Stephen Williams, *Evolution of Analog Circuits for Low-Energy Computation*, Young Entrepreneur and Scholar (YES) and RAMP advisee, Fall 2014 – Spring 2016.
2. Nour Oreifej, *FPGA Fault Recovery Simulation Environment*, Undergraduate Exchange Research Project, Training completed September, 2005.
   – Graduate employed by Oracle Corporation.

H. Additional Funded Graduate Project Supervision

1. George R. Harris, M.S. Thesis student, Topic: *Self-timed Architecture for Masked Successive Approximation Analog-to-Digital Conversion*. Graduated May, 2006. Funded 20 hours per week Research Assistantship.
2. Michael Haendel, M.S. Thesis student, Topic: *Dynamic Reconfiguration of Field Programmable Gate Arrays under JTAG Control*. Graduated in December, 2005. Funded 10 hours per week Research Assistantship.
3. Anuja Thakkar, Graduate Research Project: *Dynamic Partial Reconfiguration of FPGAs using JTAG APIs*. Graduated in September, 2005. Funded 10 hours per week Research Assistantship.

I. Students Under Advisement

Currently advising 8 students as Dissertation Chair, 1 as Dissertation Co-Chair, and 1 as Masters Thesis Chair:

1. Navid Khoshavi, CpE Ph.D. student, Topic: *Technology and Energy-Aware Memory Hierarchies*, passed Ph.D. Qualifying Review in Spring, 2015. Graduation anticipated in Fall, 2017.
2. Arman Roohi, CpE Ph.D. student, Topic: *Domain Wall-based True Random Number Generator Leveraging Stochastic Switching Behavior*, passed Ph.D. Qualifying Review in Spring, 2015. Graduation anticipated in Fall, 2018.

3. Ramtin Zand, CpE Ph.D. student, Topic: *Reconfigurable Spintronic Fabric for Minimal Energy Field Programmable Devices*, Graduation anticipated in Fall, 2018.
4. Steven D. Pyle, CpE Ph.D. student, *Self-Complementing Domain Wall Latch for Wide Sensing Margin Non-Volatile Memory*, graduation anticipated, Fall, 2018.
5. Faris Alghareb, CpE Ph.D. student, Topic: *Scalability of Temporal Modular Redundancy for Near-Threshold Computing*, passed Ph.D. Qualifying Review in Spring, 2015. Graduation anticipated in Fall, 2018.
6. Soheil Salehi Mobarakeh, CpE Ph.D. student, Topic: *U-shaped Magnetic Tunnel Junction (U-MTJ) Memory Cell*, Graduation anticipated in Fall, 2019.
7. Co-advisor for Prof. Deliang Fan of Sehar Butt, CpE Ph.D. student, Topic: *Voltage-Controlled Spintronic Computation*, Graduation anticipated in Fall, 2019.
8. Co-advisor for Prof. Mingjie Lin of Y. Bai, CpE Ph.D. student, Topic: O*ptimally Fortifying Logic Reliability through Criticality Ranking*, Graduation anticipated in May, 2017.

V. Research Activities

A. Funded Projects

Funding, match, and cost share as PI or co-PI: $7,205,565.

– Federally-Sponsored Projects: $4,902,363 (68%)

– R. F. DeMara's credit share: $4,087,590

1. B. Chen, R, Hartshorne, R. F. DeMara, *Incorporating Career-Readiness Learning in Foundational STEM Curricula via Integrative Assessments*, UCF Quality Enhancement Plan (QEP) Fund, July 2017 – June 2019: $10,000. DeMara share: $3,333.
2. R. F. DeMara, *Evaluation and Proficiency Center*, UCF Technology Fund, January 2017 – January 2018, $275,000. College match $32,840. Project Total: $307,840.
3. R. F. DeMara, Y. Jin, M. Lin, J. Wang, and J. S. Yuan, *Ubiquitous Computing Showcase*, Florida SUS ITPF, July 2014 – June 2015, $300,000. DeMara share: $60,000.
4. R. F. DeMara, *College of Engineering and Computer Science Expansion of the Evaluation and Proficiency Center*, Florida SUS ITPF, July 2016 – June 2017, $300,000. Directed ten faculty, five Ph.D. students, and the manager staff spanning both pedagogical research and delivery aspects for STEM innovation of ten undergraduate courses.
5. R. F. DeMara, *Initiatives in STEM Fellow (iSTEM Fellow)*, NSF Grant for iSTEM Initiatives, August 2016 – June 2016, $20,000.
6. R. F. DeMara, *Trusted IoT using Cross-layer Leveraging of Reconfigurable Device Signatures*, Florida Cybersecurity Center, May 2016 – April 2017, $25,000.
7. J. S. Yuan, H. Cho, R. Abdolvand, G. Atia, R. F. DeMara, and X. Gong, *NSF I/UCRC Center for Multi-functional Integrated System Technology (MIST)*, National Science Foundation (NSF), September 2014 – August 2015, $255,000 including match. DeMara share: $5,200.
8. R. F. DeMara, *Aging-Aware Hardware-Trojan Detection at Runtime*, Florida Cybersecurity Center, May 2015 – August 2016, $25,000.
9. R. F. DeMara, *Electronic Evaluation and Proficiency Enhancement in ECE Gateway Courses*, Florida SUS ITPF funding administered, May 2014 – April 2016, $228,385.

10. R. F. DeMara, Y. Jin, M. Lin, J. Wang, and J. S. Yuan, *Trusted and Bio-inspired Computing Laboratory and Testbed*, Florida SUS ITPF, July 2014 – June 2015, $100,000. DeMara share: $20,000.
11. M. Lin, K. O. Stanley, L. Wei, R. F. DeMara, M. Georgiopoulos, P. F. Wahid, *Hardware-Assisted Large-Scale Neuroevolution for Multiagent Learning*, U.S. Army Research Office (ARO) Defense University Research Instrumentation Program (DURIP), June 2012 – May 2013, $201,500. DeMara share: $14,105.
12. A. J. Gonzalez and R. F. DeMara, *CRPA: Communicating Avatars: Artificial Intelligence + Computer Graphics = Innovative Science*, National Science Foundation (NSF), Oct 2011 – September 2014, $150,000. DeMara share: $75,000.
13. A. J. Gonzalez and R. F. DeMara, *IRES: U.S.-France Research and Education on Contextual Reasoning and its Application to Conversational Agents*, National Science Foundation (NSF), April 2010 – March 2014, $141,129. DeMara share: $70,565.
14. A. J. Gonzalez and R. F. DeMara, *Collaborative Research: Towards Lifelike Computer Interfaces that Learn*, National Science Foundation (NSF), February 2007 – January 2014, $682,843 (includes an NSF Supplement of $44,500 and REU supplements totaling $63,600) plus $43,208 university match for a total of $735,651. DeMara share: $367,825.
15. R. F. DeMara, *Soar-Longevity: A Sustainable Autonomic Architecture for Organically Reconfigurable Computing Systems,* Defense Advanced Research Projects Agency (DARPA) SBIR Phase I subcontract, January 2008 – August 2008, $32,851. DeMara share: $32,851.
16. R. F. DeMara, *FPGA Dynamic Reconfiguration Resource Management,* U. S. Air Force SBIR Phase II subcontract, August 2006 – July 2008, $198,903 awarded but retained.
17. R. F. DeMara, *Adaptive Device Fault Occlusion through Competitive Runtime Reconfiguration*, National Aeronautics and Space Administration (NASA), October 2004 – September 2007, $356,000 awarded (modified to $300,000) plus $84,337 university match and $58,532 cost share for a total of $525,538 (modified to $469,538). DeMara share: $469,538.
18. M. Georgiopoulos, R. F. DeMara, A. J. Gonzalez, M. Kysilka, M. Mollaghasemi, E. Gelenbe, and A. Wu, *Machine Learning Advances for Engineering Education***,** National Science Foundation (NSF), June 2002 – August 2007, $428,851 plus $165,077 university match for a total of $593,928. DeMara share: $83,149.
19. R. F. DeMara, *Distributed Simulation Fidelity Optimization in the Presence of Communication Latency,* U.S. Army Research, Development, and Engineering Command (RDECOM), January 2005 – February 2006, $100,000 plus $5,000 university match and $3,600 cost share for a total of $108,600. DeMara share: $108,600.
20. R. F. DeMara, *Multi-layer Runtime Reconfiguration Architecture supporting FPGA Defragmentation,* U. S. Air Force SBIR Phase I subcontract, September 2005 – December 2005, $16,178. DeMara share: $16,178.
21. R. F. DeMara, A. J. Gonzalez, and M. Georgiopoulos, *Bandwidth and Latency Implications of Integrated Training and Tactical Communication Networks*, U.S. Army Research, Development, and Engineering Command (RDECOM), May 2002 – September 2004, $268,491 plus $28,700 university match and $21,600 cost share for a total of $318,591. DeMara share: $254,873.

22. A. J. Gonzalez, M. Georgiopoulos, and R. F. DeMara, *Learning Robotic Behaviors from Observation of Human Performance*, U.S. Army Simulation Training and Instrumentation Command (STRICOM), May 2002 – April 2003, $110,000. DeMara share: $27,500.
23. J. S. Yuan and R. F. DeMara, *Application-Specific IC Design Using Asynchronous Methodologies*, Theseus Logic, Inc., September 1999 – December 2002, $270,000 plus $240,000 state match and $72,000 cost share for a total of $582,000. DeMara share: $291,000.
24. R. F. DeMara, *Active Computer Defense using Autonomous Agents*, National Security Agency (NSA) subcontract, August 1999 – December 2002, $147,382 plus $6,500 department match for a total of $153,882. DeMara share: $153,882.
25. A. J. Gonzalez, R. F. DeMara, and M. Georgiopoulos, *Automated Model Development Techniques for Human Behavior Models*, Defense Modeling and Simulation Office (DMSO), May 2001 – August 2002, $98,510 plus $9,834 university match for a total of $108,344. DeMara share: $27,086.
26. A. J. Gonzalez, M. Georgiopoulos, and R. F. DeMara, *An Advanced Representational Paradigm for Human Behavior Modeling in Computer Generated Forces*, U.S. Army STRICOM and Defense Modeling and Simulation Office (DMSO), March 2001 – August 2002, $198,889 plus $15,323 university match for a total of $214,212. DeMara share: $53,553.
27. K. Reynolds, M. Georgiopoulos, R. F. DeMara, R. Eaglin, A. J. Gonzalez, and C. Watkins, *Florida Department of Law Enforcement Drug Enforcement Distributed Database System*, State of Florida, April 2000 – April 2001, $250,000 plus $55,400 university cost share for a total of $305,400. DeMara share: $62,500.
28. A. J. Gonzalez, M. Georgiopoulos, and R. F. DeMara, *Context-Based Representation of Intelligent Behavior in Degraded Systems Simulation*, Naval Air Warfare Center Training Systems Division (NAWCTSD), March 2000 – September 2000, $49,960. DeMara share: $7,494.
29. A. J. Gonzalez, R. F. DeMara, and M. Georgiopoulos, *Research Collaboration on Human Behavioral Modeling Techniques for Computer Generated Simulation Entities*, Mitsubishi Research Institute, August 1999 – August 2000, $29,269. DeMara share: $7,317.
30. R. F. DeMara, M. Georgiopoulos, and A. J. Gonzalez, *Intelligent Data-Mining of Advanced Training Management and Support Systems*, Lockheed Martin Information Systems, August 1999 – May 2000, $38,000 in cost share. DeMara share: $34,200.
31. J. S. Yuan, R. F. DeMara, and Z. Qu, *Interdisciplinary Research in Computer Architecture, ASIC, and Microelectronics Testing and Characterization*, Theseus Logic and UCF Presidential Research Infrastructure Initiative, January, 2000, $116,000. DeMara share: $38,667.
32. R. F. DeMara and P. McCauley-Bell, *Tethered Agent System for Distributed Intrusion Detection*, Lockheed Martin Information Systems, January 1999 – December 1999, $35,000 plus $35,000 state match for a total of $70,000. DeMara share: $70,000.
33. R. F. DeMara, *Software Mechanism for Efficient Barrier Synchronization*, UCF Office of Research, July 1998 – June 1999, $7,485. DeMara share: $7,485.
34. R. F. DeMara, R. Eaglin, and M. Y. Wu, *Media Hawk Processor System*, New Equipment Grant, Concurrent Computer Corporation, Inc., August, 1998, $110,000. DeMara share: $110,000.

35. A. J. Gonzalez, R. F. DeMara, and M. Georgiopoulos, *Vehicle Model Generation and Optimization for Embedded Simulation*, Naval Air Warfare Center Training Systems Division (NAWCTSD), January 1998 – December 2001, $402,496. DeMara share: $132,823.
36. R. F. DeMara and B. Petrasko, *Concurrency Strategies for High-Level Simulation Architecture*, Lockheed Martin Information Systems, January 1996 – April 1996, $10,000. DeMara share: $5,000.
37. R. F. DeMara, *Nighthawk Multiprocessor System*, New Equipment Grant, Harris Computer Systems / Concurrent Computer Systems Corporation, Inc., January, 1996, $275,000. DeMara share: $275,000.
38. R. F. DeMara, *Interprocessor Bandwidth Capacities of Hierarchical Multiprocessor Memory Systems*, Harris Computer Systems / Concurrent Computer Systems Corporation, Inc., June 1995 – December 1996, $46,473. DeMara share: $46,473.
39. R. F. DeMara and B. Petrasko, *X-terminal Workstations*, New Equipment Grant, NCR Corporation, September, 1994, $6,000. DeMara share: $3,000.
40. R. F. DeMara, *Distributed Interactive Simulation of Computer Generated Forces*, Institute for Simulation and Training, May 1993 – December 1993, $18,700. DeMara share: $18,700.
41. R. F. DeMara, *Engineering Infrastructure-Engineering Station Development*, State of Florida, September, 1994, January, 1993, $13,150 including $5,000 department match. DeMara share: $13,150.

B. Edited Proceedings

1. T. Plaks (Ed.), and R. DeMara, M. Gokhale, S. Guccione, C. Patterson, M. Platzner, G. Smit, and M. Wirthlin, (Assoc. Eds.), *Proceedings of the Seventh International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, Nevada, U.S.A., June 25 – 28, 2007, CSREA Press, 321 pages, ISBN 1–60132–026–4, 2007.
2. T. Plaks (Ed.), and R. DeMara, M. Gokhale, S. Guccione, C. Patterson, M. Platzner, G. Smit, and M. Wirthlin, (Assoc. Eds.), *Proceedings of the Sixth International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, Nevada, U.S.A., June 26 – 29, 2006, CSREA Press, 272 pages, ISBN 1–60132–011–6, 2006.
3. T. Plaks (Ed.), and R. DeMara, M. Gokhale, S. Guccione, M. Platzner, G. Smit, and M. Wirthlin, (Assoc. Eds.), *Proceedings of the Fifth International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, Nevada, U.S.A., June 27 – 30, 2005, CSREA Press, 264 pages, ISBN 1–932415–74–2, 2005.

C. Book Chapters

1. A. Vega, P. Bose, and A. Buyuktosunoglu, and R. F. DeMara, "Reliable and power-aware architectures: Fundamentals and modeling," in Rugged Embedded Systems: Computing in Harsh Environments, Elsevier Publishing (Chapter 2), 2017, A. Vega, P. Bose, and A. Buyuktosunoglu, Eds., ISBN-10: 0-128-02459-3, ISBN-13: 978-0-12-802459-1.
2. R. F. DeMara, N. Imran, and R. A. Ashraf, "Emerging Resilience Techniques for Embedded Devices," in Rugged Embedded Systems: Computing in Harsh Environments, Elsevier Publishing, (Chapter 4), 2017, A. Vega, P. Bose, and A. Buyuktosunoglu, Eds., ISBN-10: 0-128-02459-3, ISBN-13: 978-0-12-802459-1.

3. J. Castro, J. Secretan, M. Georgiopoulos, R. F. DeMara, G. Anagnostopoulos, and A. Gonzalez, "Pipelining Fuzzy ARTMAP without Match-Tracking," in *Intelligent Engineering Systems through Artificial Neural Networks*, Vol. 14, ASME Press, 2004, ISBN: 0–791–80228–0, pp. 100 – 106.
4. R. F. DeMara, Contributor, *Comprehensive Dictionary of Electrical Engineering*, P. A. Laplante, Editor-in-chief, IEEE Press, 1999, ISBN: 0–8493–3128–5.
5. S. H. Chung, D. I. Moldovan, and R. F. DeMara, "Massively Parallel Speech Understanding," in *Massively Parallel Artificial Intelligence*, MIT Press, 1993, J. A. Hendler and H. Kitano, Ed., ISBN: 0–262–61102–3, pp. 138 – 170.

D. Journal Articles

1. R. Zand, A. Roohi, and R. F. DeMara, "Energy-Efficient and Process Variation-Resilient Write Circuit Schemes for Spin Hall Effect MRAM," accepted to *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. PP, No. PP, in-press, accepted 24 April 2017.
2. N. Khoshavi, R. A. Ashraf, R. F. DeMara, S. Kiamehr, F. Oboril, and M. B. Tahoori, "Contemporary CMOS Aging Mitigation Techniques: Survey, Taxonomy, and Methods," accepted to *Integration, the VLSI Journal*, Vol. PP, No. PP, in-press, accepted 24 March 2017.
3. R. Zand, A. Roohi, D. Fan and R. F. DeMara, "Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. PP, No. PP, in-press, accepted 22 January 2017.
4. M. Krishna, R. Zand, A. Roohi, and R. F. DeMara, "Heterogeneous Energy-Sparing Reconfigurable Logic: Spin-based Storage and CNFET-based Multiplexing," *IET Circuits, Devices, and Systems, (IEEE-indexed)*, Vol. PP, No. PP, pp. 1-8, Accepted 11 January 2017.
5. R. Oreifej, R. Al-Haddad, R. A. Ashraf, R. Zand, and R. F. DeMara, "Survivability Modeling and Resource Planning for Self-Repairing Reconfigurable Device Fabrics," accepted to *IEEE Transactions on Cybernetics*, in-press, accepted 23 August 2016.
6. M. Alawad, Y. Bai, M. Lin, and R. F. DeMara, "Robust Large-Scale Convolution through Stochastic-Based Processing without Multipliers," accepted to *IEEE Transactions on Emerging Topics in Computing*, in-press, accepted 12 August 2016.
   Selected to *IEEE Transactions* Special Issue on Approximate and Stochastic Computing Circuits, Systems and Algorithms.
7. A. Roohi, R. Zand, S. Angizi, and R. F. DeMara, "A Parity-Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency," accepted to *IEEE Transactions on Emerging Topics in Computing*, in-press, accepted 18 July 2016.
   Selected to *IEEE Transactions* Special Issue on Defect and Fault Tolerance in VLSI and Nanotechnology Systems.
8. F. Alghareb, R. A. Ashraf, A. Al-Zahrani, and R. F. DeMara, "Energy and Delay Tradeoffs of Soft Error Masking for 16nm FinFET Logic Paths: Survey and Impact of Process Variation in Near Threshold Region," accepted to *IEEE Transactions on Circuits and Systems II*, in-press, accepted 16 April, 2016.
   IEEE ISCAS Program Committee Selection as an *IEEE Transactions on Circuits and Systems* highlighted article of 2017.

9. R. F. DeMara, M. Platzner, and M. Ottavi, "Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures," *IEEE Transactions on Computers*, Vol. 66, No. 6, pp. in-press, June 2017.

10. X. Chen, N. Khoshavi, R. F. DeMara, J. Wang, D. Huang, W. Wen, and Y. Chen, "Energy-Aware Adaptive Restore Schemes for MLC STT-RAM Cache," *IEEE Transactions on Computers*, Vol. 66, No. 5, pp. 786 – 798, May 2017, doi:10.1109/TC.2016.2625245

    Paper of the Month, including free download with hosted companion video featured on *IEEE Transactions* webpage.

11. R. F. DeMara, M. Platzner, and M. Ottavi, "Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures," *IEEE Transactions on Emerging Topics in Computing*, Vol. 4, No. 3, pp. in-press, April - June 2017.

12. S. Salehi, D. Fan, and R. F. DeMara, "Survey of STT-MRAM Cell Design Strategies: Taxonomy and Sense Amplifier Tradeoffs for Resiliency," *ACM Journal on Emerging Technologies in Computing (JETC)*, Vol. 33, No. 3, pp. 1 – 16, April 2017. DOI: https://doi.org/10.1145/2997650

13. S. Angizi, A. Roohi, S. Sheikhfaal, and R. F. DeMara, "Towards Ultra-efficient QCA Reversible Circuits," *Microprocessors and Microsystems*, Volume 49, March 2017, Pages 127–138, ISSN 0141-9331, http://dx.doi.org/10.1016/j.micpro.2016.09.015.

14. A. J. Gonzalez, J. R. Hollister, R. F. DeMara, J. Leigh, B. Lanman, S. Y. Lee, S. Parker, C. Walls, J. Parker, J. Wong, C. Barham, B. Wilder, "AI in Informal Science Education: Bringing Turing Back to Life to Perform the Turing Test," *International Journal of Artificial Intelligence in Education*, Vol. 27, No. 3, pp. 353 – 384, March 2017. doi:10.1007/s40593-017-0144-1

15. R. Zand, A. Roohi, D. Fan and R. F. DeMara, "Energy-Efficient Nonvolatile Reconfigurable Logic using Spin Hall Effect-based Lookup Tables," *IEEE Transactions on Nanotechnology*, Vol. 16, No. 1, pp. 32 - 43, January 2017. https://doi.org/10.1109/TNANO.2016.2625749

16. A. Al-Zahrani and R. F. DeMara, "Fast Online Diagnosis and Recovery of Reconfigurable Logic Fabrics using Design Disjunction," *IEEE Transactions on Computers*, Vol. 65, No. 10, pp. 3055-3069, October 2016. DOI 10.1109/TC.2015.2513762

17. A. Roohi, R. Zand, and R. F. DeMara, "A Tunable Majority Gate based Full Adder using Current-Induced Domain Wall Nanomagnets," *IEEE Transactions on Magnetics*, Vol. 52, No. 8, pp. 1 – 7, August 2016. DOI: 10.1109/TMAG.2016.2540600

18. R. Zand, A. Roohi, S. Salehi, and R. F. DeMara, "Scalable Adaptive Spintronic Reconfigurable Logic using Area-Matched MTJ Design," *IEEE Transactions on Circuits and Systems II*, Vol. 63, No. 7, pp. 678-682, July 2016. doi: 10.1109/TCSII.2016.2532099

19. S. D. Pyle, H. Li, and R. F. DeMara, "Compact Low-Power Instant Store and Restore D Flip-Flop using a Self-Complementing Spintronic Device," *IET Electronics Letters (IEEE indexed)*, Vol. 52, No. 14, pp. 1238 – 1240, June 2016. DOI: 10.1049/el.2015.4114.

    Featured Paper of the Issue, including author interview of topic area and field outlook.

20. H. Shabani, A. Roohi, A. Reza, M. Reshadi, N. Bagherzadeh, and R. F. DeMara, "Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks," *IEEE Transaction on Computers*, Vol. 65, No. 6, June 2016, pp. 1789 – 1801. DOI: 10.1109/TC.2015.2458866.

    Paper of the Month, including free download with hosted companion video featured on *IEEE Transactions* webpage.

21. V. Thangavel, Z. Song, and R. F. DeMara, "Intrinsic Evolution of Truncated Puiseux Series on a Mixed-Signal Field Programmable SoC," *IEEE Access*, Vol. 4, pp. 2863 – 2872, April 2016. DOI 10.1109/ACCESS.2016.2537983.

22. A. Roohi, H. Thapliyal, and R. F. DeMara, "Wire Crossing Constrained QCA Circuit Design using Bilayer Logic Decomposition," *IET Electronics Letters (IEEE indexed)*, vol. 51, no. 21, October 2015, pp. 1677 – 1679. DOI: 10.1049/el.2015.2622, Print ISSN 0013-5194, Online ISSN 1350-911X.

23. M. Lin, S. Chen, R. F. DeMara, and J. Wawrzynek, "ASTRO: Synthesizing Application-Specific Reconfigurable Hardware Traces to Exploit Memory-Level Parallelism," *Microprocessors and Microsystems*, vol. 39, no. 7, October 2015, pp. 553 – 564.

24. A. Roohi, R. F. DeMara, and N. Khoshavi, "Design and Evaluation of an Ultra-Area-Efficient Fault-Tolerant QCA Full Adder," *Microelectronics Journal*, vol. 46, no. 6, June 2015, pp. 531 – 542.

25. M. Alawad, R. F. DeMara, and M. Lin, "Stochastically Estimating Modular Criticality in Large-Scale Logic Circuits Using Sparsity Regularization and Compressive Sensing," *Journal of Low Power Electronics and Applications*, vol. 5, no. 1, March 2015, pp. 3 – 37.

26. Y. Bai, M. Alawad, R. F. DeMara, and M. Lin, "Optimally Fortifying Logic Reliability through Criticality Ranking," *Electronics*, vol. 4, no. 1, February 2015, pp. 150 – 172.

27. N. Imran, R. A. Ashraf, and R. F. DeMara, "Power and Quality-Aware Image Processing Soft-Resilience using Online Multi-Objective GAs," *International Journal of Computational Vision and Robotics*, Vol. 5, No. 1, January 2015, pp. 72 – 98. DOI: 10.1504/IJCVR.2015.067154

28. N. Imran, R. A. Ashraf, J. Lee, and R. F. DeMara, "Activity-based Resource Allocation for Motion Estimation Engines," *Journal of Circuits, Systems, and Computers*, Vol. 24, No. 1, January 2015, pp. 1 – 32. DOI: 10.1142/S0218126615500048

29. N. Imran and R. F. DeMara, "Distance-Ranked Fault Identification of Reconfigurable Hardware Bitstreams via Functional Input," *International Journal of Reconfigurable Computing*, vol. 2014, pp. 1 – 21, March 2014. DOI: 10.1155/2014/279673

30. R. A. Ashraf and R. F. DeMara, "Scalable FPGA Refurbishment using Netlist-driven Evolutionary Algorithms," *IEEE Transactions on Computers*, vol. 62, no. 8, pp. 1526 – 1541, August 2013. DOI:10.1109/TC.2013.58

    Selected to *IEEE Transactions* Special Section on Adaptive Hardware and Systems.

31. N. Imran, R. F. DeMara, J. Lee, and J. Huang, "Self-Adapting Resource Escalation for Resilient Signal Processing Architectures," *Journal of Signal Processing Systems*, Volume 77, Issue 3, pp. 257 – 280, July 2013. DOI: 10.1007/s11265-013-0811-x

32. N. Imran, J. Lee, and R. F. DeMara, "Fault Demotion Using Reconfigurable Slack (FaDReS)," *IEEE Transactions on VLSI* Systems, vol. 21, no. 7, pp. 1364–1368, July 2013. DOI: 10.1109/TVLSI.2012.2206836
33. A. J. Gonzalez, R. F. DeMara, V. C. Hung, J. C. Leon-Barth, M. Elvir, J. Hollister, S. Kobosko, J. Leigh, A. Johnson, S. Jones, G. Carlson, S. Lee, L. Renambot, and M. Brown, "Passing an Enhanced Turing Test – Interacting with Lifelike Computer Representations of Specific Individuals," *Journal of Intelligent Systems*, Volume 22, Issue 4, Pages 365–415, ISSN (Online) 2191-026X, ISSN (Print) 0334-1860, DOI: 10.1515/jisys-2013-0016, May 2013.
34. N. Imran, J. Lee, Y. Kim, M. Lin, and R. F. DeMara, "Fault-Mitigation by Adaptive Dynamic Reconfiguration for Survivable Signal-Processing Architectures," *International Journal of Control and Automation (IJCA),* Volume 6, Number 2, Pages 111 – 120, April 2013.
35. C. A. Sharma, A. Sarvi, A. Al-Zahrani, and R. F. DeMara, "Self-Healing Reconfigurable Logic using Autonomous Group Testing," *Microprocessors and Microsystems*, Volume 37, Issue 2, March 2013, pp. 174 – 184. DOI: 10.1016/j.micpro.2012.09.009
36. N. Imran, J. Lee, Y. Kim, M. Lin, and R. F. DeMara, "Amorphous Slack Methodology for Autonomous Fault-Handling in Reconfigurable Devices," *International Journal of Multimedia and Ubiquitous Engineering*, Vol. 7, Issue 4, October, 2012, pp. 29 – 44.
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38. R. Al-Haddad, R. Oreifej, R. A. Ashraf, and R. F. DeMara, "Sustainable Modular Adaptive Redundancy Technique Emphasizing Partial Reconfiguration for Reduced Power Consumption," *International Journal of Reconfigurable Computing*, Article ID 430808, June, 2011, pp 1 – 25, 2011. doi:10.1155/2011/430808.
39. M. G. Parris, C. A. Sharma, and R. F. DeMara, "Progress in Autonomous Fault Recovery of Field Programmable Gate Arrays," *ACM Computing Surveys*, Vol. 43, Issue 4, December 2011, pp 1 – 21.
40. R. F. DeMara, K. Zhang, and C. A. Sharma "Autonomic Fault-Handling and Refurbishment Using Throughput-Driven Assessment," *Applied Soft Computing*, Volume 11, Issue 2, March 2011, pp. 1588 – 1599.
41. W. Kuang, P. Zhao, J. S. Yuan, R. F. DeMara, "Design of Asynchronous Circuits for High Soft Error Tolerance in Deep Submicron CMOS Circuits," *IEEE Transactions on VLSI Systems*, Vol. 18, No. 10, March, 2010, pp. 410 – 422.
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45. H. Tan and R. F. DeMara, "A Multi-layer FPGA Framework Supporting Autonomous Partial Runtime Reconfiguration," *IEEE Transactions on VLSI Systems*, Vol. 16, No. 5, May, 2008, pp. 504 – 516.
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56. H. Fernlund, A. J. Gonzalez, R. F. DeMara, and M. Georgiopoulos, "Learning Tactical Human Behavior through Observation of a Human Actor," *IEEE Transactions on Systems, Man and Cybernetics: Part B - Cybernetics*, Vol. 36, No. 1, February, 2006, pp. 128 – 140.
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E. Conference Proceedings and Presentations

1. R. A. Ashraf, R. Gioiosa, G. Kestor, R. F. DeMara, "Exploring the Effect of Compiler Optimizations on the Reliability of HPC Applications," in *Proceedings of 22nd IEEE Workshop on Dependable Parallel, Distributed and Network-Centric Systems (IEEE DPDNS 2017)*, Orlando, FL, USA, June 2, 2017.
2. F. Alghareb, R. A. Ashraf, A. Al-Zahrani, and R. F. DeMara, "Energy and Delay Tradeoffs of Soft Error Masking for 16nm FinFET Logic Paths: Survey and Impact of Process Variation in Near Threshold Region," *IEEE International Symposium on Circuits & Systems (ISCAS-2017)*, lecture presentation, Baltimore, MD, USA, May 28 – 31, 2017.

   Program Committee Selection as an *IEEE Transactions on Circuits and Systems* highlighted article of 2017 for Lecture Presentation at ISCAS.
3. S. Salehi and R. F. DeMara, "Process Variation Immune and Energy Aware Sense Amplifiers for Resistive Non-Volatile Memories," In *Proceedings of IEEE International Symposium on Circuits & Systems (ISCAS-2017)*, Baltimore, MD, USA, May 28 – 31, 2017
4. Y. Bai, S. Hu, R. F. DeMara, and M. Lin, "A Spin-Orbit Torque based Cellular Neural Network (CNN) Architecture," in *Proceedings of 27th IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI-2017)*, Banff, Alberta, Canada, May 10 – 12, 2017.
5. R. F. DeMara, "Heterogeneous Technology Configurable Fabrics: Leveraging Reconfiguration as a Pathway Towards Emerging Devices," *in Proceedings of IEEE Reconfigurable Architectures Workshop (RAW-2017)*, Orlando, FL, USA, May 29, 2017.

   Keynote Speech of the conference; IEEE-indexed.
6. R. F. DeMara, R. Hartshorne, B. Chen, R. Zand, "Digitizing and Remediating Engineering Assessments: An Immersive and Transportable Faculty Development Workshop," in *Proceedings of American Association for Engineering Education National Conference (ASEE-17)*, Columbus, OH, USA, June 25 – 28, 2017.

7. R. F. DeMara, S. Salehi, R. Hartshorne, B. Chen, "GLASS: Group Learning At Significant Scale via WiFi-Enabled Learner Design Teams in an ECE Flipped Classroom," in *Proceedings of American Association for Engineering Education National Conference (ASEE-17)*, Columbus, OH, USA, June 25 – 28, 2017.
8. N. Khoshavi, S. Salehi, and R. F. DeMara, "Variation-Immune Resistive Non-Volatile Memory using Self-Organized Sub-Bank Circuit Designs," in *Proceedings of 18th International Symposium on Quality Electronic Design (ISQED-2017)*, Santa Clara, CA, USA, March 13 – 15, 2017.

   Conference Best Paper Candidate / A Best Paper of Track.
9. S. Angizi, Z. He, R. F. DeMara, D. Fan, "Composite Spintronic Accuracy-Configurable Adder for Low Power Digital Signal Processing," in *Proceedings of 18th International Symposium on Quality Electronic Design (ISQED-2017)*, Santa Clara, CA, USA, March 13 – 15, 2017.
10. R. Hartshorne, R. F. DeMara, and B. Chen, "Strategies and Lessons Learned from a Faculty Development Pilot Program for Computerizing Assessments in Engineering Curricula," abstract and presentation at *27th Annual Conference of the Society for Information Technology and Teacher Education (SITE-2017)*, Austin, TX, USA, March 5 – 9, 2017.
11. S. Kose, L. Fei, R. F. DeMara, "On-Chip Sensor Circle Distribution Technique for Real-Time Hardware Trojan Detection," poster-only presentation at *Government Microcircuit Applications & Critical Technology Conference* (GOMACTech-2016), Reno, NV, USA, March 20 – 23, 2017.
12. R. Gioiosa, R. A. Ashraf, G. Kestor, R. F. DeMara, C.-Y. Cher, and P. Bose, "Modeling Fault Propagation in HPC Applications," *Workshop on Modeling & Simulation of Systems and Applications (ModSim-2016)* (presentation with abstract), Seattle, WA, USA, August 10 – 12, 2016.
13. R. F. DeMara and M. Lin, "Heterogeneous Technology Fabric," *2016 Command, Control, Communications, Computers, Intelligence (C4I) and Cyber Conference* (poster presentation only), Utica, NY, U.S.A., June 14 – 16, 2016.
14. F. Alghareb, M. Lin, and R. F. DeMara, "Soft Error Effect Tolerant Temporal Self-Voting Logic with Low Area and Energy Overheads," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2016)*, Pittsburgh, Pennsylvania, U.S.A., July 11-13, 2016.
15. R. F. DeMara, N. Khoshavi, S. Pyle, J. Edison, R. Hartshorne, B. Chen, M. Georgiopoulos, "Redesigning Computer Engineering Gateway Courses using a novel Remediation Hierarchy," in *Proceedings of American Association for Engineering Education National Conference (ASEE-16)*, New Orleans, LA, USA, June 26 – 29, 2016.
16. X. Chen, N. Khoshavi, J. Zhou, D. Huang, R. F. DeMara, J. Wang, W. Wen, and Y. Chen, "AOS: Adaptive Overwrite Scheme for Reduced-Latency Energy-Efficient MLC STT-RAM Cache," in *Proceedings of 53rd Design Automation Conference (DAC-2016)*, Austin, TX, USA, June 5 – 9, 2016.
17. R. A. Ashraf, N. Khoshavi, A. Alzahrani, R. F. DeMara, S. Kiamehr and M. B. Tahoori, "Area-Energy Tradeoffs of Logic Wear-Leveling for BTI-induced Aging," in *Proceedings of ACM Computing Frontiers*, May 16 – 18, 2016, Como, Italy. Acceptance rate 27%.
18. R. Hartshorne, B. Chen, J. Edison, and R. F. DeMara, "Flipping the Computer Engineering Gateway Courses: A Discussion of the Processes and Results", in *Proceedings of 27th Annual*

Conference of the Society for Information Technology and Teacher Education (SITE-2016), March 21 – 25, 2016, Savannah, Georgia, USA.

19. X. Chen, N. Khoshavi, R. F. DeMara, J. Wang, W. Wen, and Y. Chen, "A Selective Overwrite Scheme to Mitigate Write Disturbance for Energy Efficient MLC STT-RAM," *2016 Non-Volatile Memories Workshop (NVMW-2016)*, March 6 – 8, 2016. Presentation only; no proceedings.
20. N. Khoshavi, X. Chen, J. Wang, and R. F. DeMara, "Bit-Upset Vulnerability Factor for eDRAM," in *Proceedings of 17th International Symposium on Quality Electronic Design (ISQED 2016)*, Santa Clara, CA, USA, March 15 – 16, 2016. Acceptance rate 36.3%.
21. C. Labrado, H. Thapliyal, and R. F. DeMara, "Design of Testable Adder Circuits for Spintronics Based Nanomagnetic Computing," in *Proceedings of International Symposium on Nanoelectronic and Information Systems* (*INIS-2015)*, pp. 117 – 111, Indore, India, December 21 – 23, 2015.
22. R. F. DeMara, S. Salehi, N. Khoshavi, R. Hartshorne, and B. Chen, "Strengthening STEM Laboratory Assessment Using Student-Narrative Portfolios Interwoven with Online Evaluation," in *Proceedings of American Association for Engineering Education Southeastern Conference (ASEE-SE-16)*, pp. 1 – 15, Tuscaloosa, AL, USA, March 13 – 15, 2016.
23. R. F. DeMara, S. Salehi, and S. Muttineni, "Exam Preparation through Directed Video Blogging using Electronically-Mediated Realtime Classroom Interaction," in *Proceedings of American Association for Engineering Education Southeastern Conference (ASEE-SE-16)*, pp. 1 – 11, Tuscaloosa, AL, USA, March 13 – 15, 2016.

    Selected for a multimedia synopsis in the Teaching Online Pedagogical Repository titled "Using Learner Created Videos for Student Engagement in a Flipped Classroom."
24. R. F. DeMara and C. A. Sharma, and R. A. Ashraf, "Secure Reconfigurable Logic Fabrics through Online Resource Sensing and Competition," *Florida Cybersecurity Symposium*, (presentation with abstract), Tampa, FL, USA, October 13 – 14, 2015.
25. A. M. Chabi, A. Roohi, H. Khademolhosseini, S. Angizi, R. F. DeMara, and K. Navi, "Cost-Efficient QCA Reversible Combinational Circuits Based on a New Reversible Gate," in *IEEE Proceedings of International Symposium on Computer Architecture and Digital Systems (CADS-2015)*, pp. 1 – 6,Tehran, Iran, October 7 – 8, 2015.
26. R. A. Ashraf, R. Gioiosa, G. Kester, C. Cher, P. Bose, and R. F. DeMara, "Understanding the Propagation of Transient Errors in HPC Applications," in *Proceedings of The International Conference for High Performance Computing, Networking, Storage and Analysis (Super Computing-2015)*, Article 72, 12 pages, Austin, TX, USA, November 15 – 20, 2015. Conference acceptance rate 22%; Track acceptance rate 14.4%.
27. A. Al-Zahrani and R. F. DeMara, "Hypergraph-Cover Diversity for Maximally-Resilient Reconfigurable Systems," in *Proceedings of 12th IEEE International Conference on Embedded Software and Systems (ICESS-2015)*, pp. 1086 – 1092, New York, NY, USA, August 24 – 26, 2015. Acceptance rate 20.5%.
28. A. Al-Zahrani and R. F. DeMara, "Process Variation Immunity of Alternative 16nm HK/MG-based FPGA Logic Blocks," in *Proceedings of IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS-2015)*, pp. 1 – 4, Fort Collins, CO, USA, August 2 – 5, 2015.

29. S. D. Pyle, V. Thangavel, S. M. Williams, and R. F. DeMara, "Self-Scaling Evolution of Analog Computation Circuits with Digital Accuracy Refinement," in *IEEE Proceedings of NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2015)*, pp. 1 – 8, Montreal, QC, Canada, June 15 – 18, 2015.

    Best Paper Award of Conference – Citation: *"Best Design Paper."*

30. A. Roohi, R. F. DeMara, and N. Khoshavi, "Dual Computational Layer Based Logic Design for QCA Circuits" in *Proceedings of ACM/EDAC/IEEE* 51st *Design Automation Conference (DAC-2015) Work-In-Progress session (poster presentation only),* San Francisco, CA, USA, June 3 – 6, 2015.

31. R. A. Ashraf, A. Al-Zahrani, N. Khoshavi, R. Zand, S. Salehi, A. Roohi, M. Lin, R. F. DeMara, "Reactive Rejuvenation of CMOS Logic Paths using Self-Activating Voltage Domains," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS),* , pp. 2944 – 2947, Lisbon, Portugal, May 24-27, 2015.

32. R. Al-Haddad, R. S. Oreifej, R. Zand, A. Ejnioui, and R. F. DeMara "Adaptive Mitigation of Radiation-Induced Errors and TDDB in Reconfigurable Logic Fabrics," in *Proceedings of North American Test Workshop (NATW 2015)*, pp. 23 – 32, Johnson City, NY, USA, May 11 – 13, 2015.

33. A. A. Naseer, R. A. Ashraf, D. Dechev, and R. F. DeMara. "Designing Energy-Efficient Approximate Adders using Parallel Genetic Algorithms," in *Proceedings of IEEE SoutheastCon 2015 (SECon-2015)*, pp. 1 – 7, Fort Lauderdale, FL, April 9 – 12, 2015.

34. S. Salehi and R. F. DeMara, "Energy and Area Analysis of a Floating-Point Unit in 15nm CMOS Process Technology," in *Proceedings of IEEE SoutheastCon 2015 (SECon-2015)*, pp. 1 – 5, Fort Lauderdale, FL, USA, April 9 – 12, 2015.

35. K. Zhang, N. Khoshavi, J. M. Alghazo, and Ronald F. DeMara, "Organic Embedded Architecture for Sustainable FPGA Soft-Core Processors," in *Proceedings of IEEE 61st Reliability and Maintainability Symposium (RAMS-2015)*, pp. 1 – 6, Palm Harbor, FL, USA, January 26 – 29, 2015.

36. R. Oreifej, R. Al-Haddad, R. A. Ashraf, and R. F. DeMara, "Sustainability Assurance Modeling for SRAM-based FPGA Evolutionary Self-Repair," in *Proceedings of IEEE International Conference on Evolvable Systems (ICES-2014)*, pp. 17 – 22, Orlando, FL, USA, December 9 – 12, 2014.

37. N. Khoshavi, R. A. Ashraf, and R. F. DeMara, "Applicability of Power-Gating Strategies for Aging Mitigation of CMOS Logic Paths," in *Proceedings of IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS-2014)*, pp. 929 – 932, College Station, TX, USA, August 3 – 6, 2014.

38. R. A. Ashraf, A. Alzahrani, and R. F. DeMara, "Extending Modular Redundancy to NTV: Costs and Limits of Resiliency at Reduced Supply Voltage," in *Proceedings of Workshop on Near Threshold Computing (WNTC-2014)* Minneapolis, MN, USA, June 14, 2014.

39. R. A. Ashraf, A. Alzahrani, and R. F. DeMara, "Exploring Spatial Redundancy to Mitigate Aging-Induced Timing Degradation," *ACM/EDAC/IEEE* 51st *Design Automation Conference (DAC) (poster presentation only)*, San Francisco, California, USA, June 1 – 5, 2014.

40. N. Imran, R. Ashraf, and R. F. DeMara, "Evaluating Quality and Resilience of an Embedded Video Encoder against a Continuum of Energy Consumption," invited submission to *2014*

Workshop on Suite of Embedded Applications and Kernels (SEAK-2014), San Francisco, California, USA, June 1, 2014.

41. M. Alawad, Y. Bai, R. F. DeMara, and M. Lin, "Energy-Efficient Multiplier-Less Discrete Convolver through Probabilistic Domain Transformation," in *Proceedings of 22nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA-14)*, pp. 185-188, Monterey, California, USA, February 27-28, 2014. DOI=10.1145/2554688.2554769 http://doi.acm.org/10.1145/2554688.2554769

42. A. Alzahrani and R. F. DeMara, "Non-Adaptive Sparse Recovery and Fault Evasion using Disjunct Design Configurations," abstract in *Proceedings of 22nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA-14)*, pp 251-251, Monterey, California, USA, February 27 – 28, 2014.

43. R. Ashraf and R. F. DeMara, "Scalability of Modular Redundancy for Near-Threshold Computing," *Workshop on Highly-Reliable Power-Efficient Embedded Designs (HARSH 2014)*, Orlando, Florida, USA, February 16th, 2014.

44. J. Hollister, S. T. Parker, A. J. Gonzalez, and R. F. DeMara, "An Extended Turing Test: A Context Based Approach Designed to Educate Youth in Computing" in *Proceedings of 8th International and Interdisciplinary Conference of Modeling and Using Context (CONTEXT-2013)*, Annecy, France, October 28 – 31, 2013. Reprinted in P. Brézillon, P. Blackburn, and R. Dapoigny, editors, Modeling and Using Context, Springer Berlin Heidelberg Lecture Notes in Computer Science, ISBN: 978-3-642-40971-4, pp. 213 – 221.

45. N. Imran, R. Ashraf, and R. F. DeMara, "On-demand Fault Scrubbing Using Adaptive Modular Redundancy," in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2013)*, Las Vegas, Nevada, USA, July 22 – 25, 2013.

46. R. Ashraf, F. Luna, D. Dechev, and R. F. DeMara, "Designing digital circuits for FPGAs using parallel genetic algorithms," *2012 Spring Simulation Multi-conference (SpringSim 2012)*, Orlando, FL, USA, March 25 – 28, 2012, paper #15.

47. J. Hollister, S. Parker, A. Gonzalez, R. F. DeMara, "Who Says it Best? A Comparison of Four Different Dialog Management Systems," in *Proceedings of 21st Annual Conference on Behavior Representation in Modeling Simulation (BRIMS 2012)*, Amelia Island, FL, USA, March 12–15, 2012, pp. 141 – 146.

48. N. Imran, J. Lee, Y. Kim, M. Lin, and R. F. DeMara, "Area-Efficient Fault-Handling for Survivable Signal-Processing Architectures," in *Proceedings of First International Conference on Advanced Signal Processing (ASP 2012)*, Seoul, Korea, March 30–31, 2012, pg. 37.

49. N. Imran and R. F. DeMara, "Heterogeneous Concurrent Error Detection (hCED) Based On Output Anticipation," in *Proceedings of 2011 International Conference on Reconfigurable Computing and FPGAs (ReConFig'11)*, Cancun, Mexico, November 30, 2011 – December 2, 2011, pp. 61–66.

50. R. A. Ashraf, O. Mouri, R. Jadaa, and R. F. DeMara, "Design-For-Diversity for Improved Fault-Tolerance of TMR Systems on FPGAs," in *Proceedings of 2011 International Conference on Reconfigurable Computing and FPGAs (ReConFig'11)*, November 30, 2011 – December 2, 2011, pp. 99–104.

51. N. Imran and R. F. DeMara, "A Self-Configuring TMR Scheme Utilizing Discrepancy Resolution," in *Proceedings of 2011 International Conference on Reconfigurable Computing and FPGAs (ReConFig'11)*, Cancun, Mexico, November 30, 2011 – December 2, 2011, pp. 398–403.
52. N. Imran and R. F. DeMara, "Cyclic NMR-based Fault Tolerance with Bitstream Scrubbing via Reed-Solomon Codes," *Revolutionary Electronics in Space (ReSpace) / Military and Aerospace Programmable Logic Devices (MAPLD) 2011 Conference*, Albuquerque, NM, August 22-25, 2011. (presentation only – no proceedings at conference)
53. R. A. Ashraf and R. F. DeMara, "Scalability of Sustainable Self-Repair to Mitigate Aging Induced Degradation in SRAM-based FPGA Devices," *Revolutionary Electronics in Space (ReSpace) / Military and Aerospace Programmable Logic Devices (MAPLD) Conference*, Albuquerque, New Mexico, 2011. (presentation only – no proceedings at conference)
54. N. Imran, and R. F. DeMara, "A Fault-Handling Methodology by Promoting Hardware Configurations via PageRank," *Revolutionary Electronics in Space (ReSpace) / Military and Aerospace Programmable Logic Devices (MAPLD) Conference*, Albuquerque, NM, August 22-25, 2011. (presentation only – no proceedings at conference)
55. V. Hung, A. Gonzalez, R. F. DeMara, "Dialog Management For Rapid-Prototyping of Speech-Based Training Agents," in *Proceedings of the Interservice/Industry Training, Simulation & Education Conference*, Orlando, Florida, USA, November 29 – December 2, 2010.
56. R. F. DeMara, J. Lee, R. Al-Haddad, R. Oreifej, R. Ashraf, B. Stensrud, M. Quist, "Dynamic Partial Reconfiguration Approach to the Design of Sustainable Edge Detectors," in the *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA '10)*, Las Vegas, Nevada, USA, July 12 – 15, 2010.
57. V. Hung, M. Elvir, A. J. Gonzalez and R. F. DeMara, "A Method For Evaluating Naturalness in Conversational Dialog Systems", *IEEE International Conference on Systems, Man, and Cybernetics*, San Antonio, Texas, October, 2009.
58. D. Workman, R. F. DeMara, K. Sundaram, D. Turgut, I. Batarseh, and S. Bethel, "Preparing for an Accreditation Visit," presented at *ABET Best Assessment Processes Symposium*, Indianapolis, IN, U.S.A., April 3 – 4, 2009, pp. 1 – 16.
59. V. Hung, A. Gonzalez, and R. F. DeMara, "Towards a Context-Based Dialog Management Layer for Expert Systems," in *Proceedings of the International Conference on Information, Process, and Knowledge Management (eKNOW'09)*, Cancun, Mexico, February 2 – 7, 2009, pp. 60 – 65.
60. R. F. DeMara, A. J. Gonzalez, S. Jones, A. Johnson, J. Leigh, V. Hung, C. Leon-Barth, R. A. Dookhoo, L. Renambot, S. Lee, and G. Carlson, "Towards Interactive Training with an Avatar-based Human-Computer Interface", in *Proceedings of the 2008 Interservice/Industry Training Systems and Education Conference (I/ITSEC'08)*, Orlando, FL, U.S.A., December 1 – 4, 2008.
61. A. Sarvi, C. A. Sharma, R. F. DeMara, "BIST-Based Group Testing For Diagnosis of Embedded FPGA Cores," in Proceedings of the *International Conference on Embedded Systems and Applications (ESA'08)*, Las Vegas, Nevada, U.S.A., July 14 – 17, 2008.

62. J. Huang, M. Parris, J. Lee, and R. F. DeMara, "Scalable FPGA Architecture for DCT Computation using Dynamic Partial Reconfiguration," in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA '07)*, Las Vegas, Nevada, U.S.A., July 14 – 17, 2008.

63. K. Zhang, R. F. DeMara, and J. Alghazo, "FPGA Self-Repair using an Organic Embedded System Architecture," in *Proceedings of the International Workshop on Dependable Circuits Design*, Buenos Aires, Argentina, December 6 – 7, 2007.

64. R. S. Oreifej, R. N. Al-Haddad, H. Tan, R. F. DeMara, "Layered Approach To Intrinsic Evolvable Hardware Using Direct Bitstream Manipulation Of Virtex II Pro Device," in *Proceedings of the 17th International Conference On Field Programmable Logic And Applications (FPL'07*), Amsterdam, Netherlands, August 27 – 29, 2007. Acceptance rate 21%.

    Best Paper of Track and nominated for best of conference.

65. R. N. Al-Haddad, C. A. Sharma, R. F. DeMara, "Performance Evaluation of Two Allocation Schemes for Combinatorial Group Testing Fault Isolation," in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA '07)*, Las Vegas, Nevada, U.S.A., June 25 – 28, 2007.

66. K. Zhang, G. Bedette, R. F. DeMara, "Triple Modular Redundancy with Standby (TMRSB) Supporting Dynamic Resource Reconfiguration," in *Proceedings of IEEE AUTOTESTCON Conference 2006*, September 18 – 21, 2006.

67. R. S. Oreifej, C. A. Sharma, R. F. DeMara, "Expediting GA-Based Evolution Using Group Testing Techniques for Reconfigurable Hardware," in *Proceedings of the IEEE International Conference on Reconfigurable Computing and FPGAs (Reconfig'06)*, pp. 106 – 113, San Luis Potosi, Mexico, September 20 – 22, 2006.

68. R. F. DeMara, "Dynamic Runtime Reconfiguration for Evolvable Hardware," invited presentation at the *IEEE International Conference on Reconfigurable Computing and FPGAs (Reconfig'06)*, San Luis Potosi, Mexico, September 20 – 22, 2006.

    Keynote Speech of the conference.

69. H. Tan, R. F. DeMara, "A Physical Resource Management Approach to Minimizing FPGA Partial Reconfiguration Overhead," in *Proceedings of the IEEE International Conference on Reconfigurable Computing and FPGAs (Reconfig'06)*, pp. 86 – 90, San Luis Potosi, Mexico, September 20 – 22, 2006.

70. H. Tan, R. F. DeMara, A. J. Thakkar, A. Ejnioui and J. D. Sattler, "Complexity and Performance Evaluation of Two Partial Reconfiguration Interfaces on FPGAs: a Case Study," in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'06)*, Las Vegas, Nevada, U.S.A, June 26 – 29, 2006.

71. M. Georgiopoulos, E. Gelenbe, R. F. DeMara, A. J. Gonzalez, M. Kysilka, M. Mollaghasemi,, A. S. Wu, G. Anagnostopoulos, I. Russell, J. Secretan, "Assessing and Evaluating CRCD Experiences at the University of Central Florida: An NSF Project," in *Proceedings of the 2006 American Society for Engineering Education Annual Conference and Exposition (ASEE'06)*, Chicago, Illinois, U.S.A., June 18 – 21, 2006.

72. J. D. Sattler, M. Leftwich, R. F. DeMara, H. Tan, and A. Ejnioui, "Partial Reconfiguration of FPGAs with Software and Hardware Anti-Tamper Considerations," in *Proceedings of the 2006 DoD Anti-Tamper Conference (AT'06)*, Dayton, Ohio, U.S.A., April 25-27, 2006.

73. C. A. Sharma and R. F. DeMara, "A Combinatorial Group Testing Method for FPGA Fault Location," accepted to *International Conference on Advances in Computer Science and Technology (ACST'06)*, Puerto Vallarta, Mexico, January 23 – 25, 2006.

74. C. J. Milliord, C. A. Sharma, R. F. DeMara, "Dynamic Voting Schemes to Enhance Evolutionary Repair in Reconfigurable Logic Devices," in *Proceedings of the International Conference on Reconfigurable Computing and FPGAs (Reconfig'05)*, pp. 8.1.1 – 8.1.6, Puebla City, Mexico, September 28 – 30, 2005.

75. K. Zhang, R. F. DeMara, C. A. Sharma, "Consensus-based Evaluation for Fault Isolation and On-line Evolutionary Regeneration," in *Proceedings of the International Conference in Evolvable Systems (ICES'05*), pp. 12 – 24, Barcelona, Spain, September 12 – 14, 2005.

76. G. Wang, R. F. DeMara, A. J. Rocke, "Mobility-Enhanced File Integrity Analyzer For Networked Environments," in *Proceedings of the 9th World Multi-Conference on Systemics, Cybernetics and Informatics (WMSCI '05)*, pp. 341 – 346, Orlando, FL, U.S.A., July 10 – 13, 2005.

    Best Paper Award, Network Security and Security Technologies track.

77. R. F. DeMara and K. Zhang, "Autonomous FPGA Fault Handling through Competitive Runtime Reconfiguration," in *Proceedings of the NASA/DoD Conference on Evolvable Hardware (EH'05)*, pp. 109 – 116, Washington D.C., U.S.A., June 29 – July 1, 2005.

78. H. Tan and R. F. DeMara, "A Device-Controlled Dynamic Configuration Framework Supporting Heterogeneous Resource Management," in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'05)*, pp. 251 – 254, Las Vegas, Nevada, U.S.A, June 27 – 30, 2005.

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122. R. N. Mercer, M. Ebel, and R. F. DeMara, "Pipelined Architecture for Computational Nanotechnology," in *Proceedings of the 1994 IEEE Southcon Conference (Southcon'94)*, pp. 314 – 319, Orlando, Florida, U.S.A., March 29 – 31, 1994.

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127. R. F. DeMara and H. Kitano, "Benchmarking Performance of Massively Parallel AI Architectures," in *Proceedings of the Fourth Symposium on the Frontiers of Massively Parallel Computation*, pp. 517 – 520, McLean, Virginia, U.S.A., October 19 – 21, 1992.

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129. R. F. DeMara and H. Kitano, "PACE Benchmark Set," in *Proceedings of the 1991 International Joint Conference on Artificial Intelligence (IJCAI'91) – Workshop on Parallel Processing for AI*, pp. 517 – 520, Sydney, Australia, August 24 – 25, 1991.
130. R. F. DeMara and D. I. Moldovan, "Performance Indices for Parallel Marker-Propagation," in *Proceedings of the 1991 International Conference on Parallel Processing (ICPP-91)*, pp. 658 – 659, St. Charles, Illinois, U.S.A., August 12 – 16, 1991.
131. R. F. DeMara and D. I. Moldovan, "A DSP Architecture for Parallel AI Processing," in *Proceedings of the 1991 TMS320 Educators Conference*, Houston, Texas, U.S.A., July 31 – August 2, 1991.
132. R. F. DeMara and D. I. Moldovan, "The SNAP-1 Parallel AI Prototype," in *Proceedings of the Eighteenth Annual International Symposium on Computer Architecture (ISCA'91)*, pp. 2 – 11, Toronto, Ontario, Canada, May 27 – 30, 1991. Also appears in *Computer Architecture News*, Vol. 19, No. 3, pp. 2 – 11, May, 1991.
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F. Patents, Invention Disclosures, and Licenses

1. United States Provisional Patent, *Fault Recovery for Reconfigurable Hardware Devices*, Application No.: 62/271,820, filed December 28, 2015.
2. United States Patent #7,389,460, *Runtime-Competitive Fault Handling for Reconfigurable Logic Devices*, Inventor: R. F. DeMara (Orlando, FL, US), Assignee: University of Central Florida Research Foundation, Inc. (Orlando, FL, US), June 17, 2008.
3. R. F. DeMara and A. Roohi, "A Parity-Preserving Reversible QCA Gate with Cascadable Resilience," Invention Disclosure, UCF Office of Research and Commercialization, April 15, 2015.
4. R. F. DeMara and H. Tan, "Multi-layer Runtime Reconfiguration Architecture for FPGA Resource Management," FPGA circuit environment licensed by University of Central Florida Research Foundation to Space Photonics, Inc., Fayetteville, Arkansas, U.S.A, on September 2, 2005.
5. R. F. DeMara, "Discrepancy Mirror for Self-Checking Fault Detection," Invention Disclosure, University of Central Florida, February 9, 2005. Merged with invention disclosure leading to United States Patent #7,389,460.
6. R. F. DeMara and H. Tan, "Multi-layer Runtime Reconfiguration Architecture," U.S. Federal Software Copyright registered by University of Central Florida on August 30, 2005.

7. R. F. DeMara, "Replicated Global Image Memory System," Invention Disclosure, approved for Patent Application by University of Central Florida Patent Review Committee, 1999.

G. Research Laboratory Leadership

- Founder and Director:
  - *Computer Architecture Laboratory* – University of Central Florida
    Involves 3 other faculty and 8 graduate students, http://cal.ucf.edu
- Co-Founder and Co-Director:
  - *Intelligent Systems Laboratory* – University of Central Florida
    Involves 1 other faculty and several graduate/honors students, http://isl.ucf.edu

H. Post-Doctoral Supervision

- Dr. Jafaar Alghazo, Post-Doctoral Researcher from Southern Illinois University, Carbondale, Illinois, U.S.A., at UCF Campus during 2007 – 2008 academic year.
- Dr. Ayman Alnsour, Post-Doctoral Researcher from Al-Isra University, Amman, Jordan, at UCF Campus during 2007 – 2008 academic year.

VI. Professional Service

A. International

- Keynote Speaker
  - Conference First Keynote Speaker: *24th Annual IEEE Reconfigurable Architectures Workshop*, Orlando, FL, USA, May 29, 2017.
  - Keynote Speaker of the Conference: *IEEE International Conference on Reconfigurable Computing and FPGAs*, San Luis Potosi, Mexico, September 20 – 22, 2006.
- Editorships:
  - **Coordinating Guest Editor** – *IEEE Transactions on Emerging Topics in Computing*, joint with *IEEE Transactions on Computers* Special Section special issue on "Innovation in Reconfigurable Logic Fabrics: from Devices to Architectures" 2015 – 2016 service for June 2017 issue: http://cal.ucf.edu/callforpaper.html
  - **Associate Editor** – *IEEE Transactions on Computers*: 2015 – 2017
  - **Associate Editor** – *IEEE Transactions on Computers*: 2013 – 2015
  - **Associate Guest Editor** – *ACM Transactions on Embedded Computing Systems,* special issue on "Configuring Algorithms, Processes and Architectures," 2009
  - **Associate Editor** – *IEEE Transactions on VLSI Systems:* 2004 – 2007
  - **Editorial Board** – *Microprocessors and Microsystems*: 2006 – 2008
  - **Associate Editor** – *Journal of Circuits, Systems, and Computers*: 2004 – 2006
- Technical Program Committees (TPCs):
  - *IEEE Symposium Series on Computational Intelligence (SSCI-2016):* 2016

- *15th IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2016)*, Digital Circuits and FPGA-Based design tracks: 2016
- *IEEE International Conference on Evolvable Systems (ICES-2015):* 2015
- *14th IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2015)*, Digital Circuits and FPGA-Based design tracks: 2015
- *IEEE Conference on High Performance Compilation, Computing and Communication (HP3C-2014)* - Track 9: High-performance Self-adaptive and Resource-aware Programming, 2014.
- *IEEE Congress on Evolutionary Computation: 2010*
- *International Conference on Field Programmable Logic and Applications*: 2008
- *Genetic and Evolutionary Computation Conference*: 2008, 2009
- *NASA/DoD Conference on Evolvable Hardware*: 2005, 2006, 2007, 2008
- *International Conference on Evolvable Systems*: 2008
- *International Conf. on Parallel and Distributed Proc. Techniques and Appl.* 2004, 2005
- *IEEE World Congress on Computational Intelligence:* 1993

- Panelist *24th Annual IEEE Reconfigurable Architectures Workshop*, Orlando, FL, USA, May 29, 2016.

- Panel Organizer, Panel Chair, and Panelist: "Signal-Image Processing and Dynamic Partial Reconfiguration," *International Conf. on Engineering of Reconfigurable Systems and Algorithms, 2010.*

- Executive Committee – *International Conference on Engr. of Reconfigurable Systems and Algorithms:* 2008

- Steering Committee – *International Conference on Engr. of Reconfigurable Systems and Algorithms:* 2005, 2006, 2007

- Discussion Panelist – *IEEE Conference on AI for Applications, 1993*

- Technical Paper Reviewer/Referee for the following Journals:
  (multiple years of service: 1990 – present)
  - *IEEE Transactions on Parallel and Distributed Systems*
  - *IEEE Transactions on VLSI Systems*
  - *IEEE Transactions on Evolutionary Computation*
  - *IEEE Transactions on Circuits and Systems*
  - *IEEE Transactions on Neural Networks*
  - *IEEE Transactions on Computers*
  - *IEEE Transactions on Aerospace Electronic Systems*
  - *IEEE Micro*
  - *Journal of Parallel and Distributed Computing*
  - *Journal of Autonomous and Multi-Agent Systems*
  - *Journal of Simulation Modeling Practice and Theory*
  - *Journal of Defense Modeling and Simulation*
  - *Journal of Supercomputing*
  - *Microprocessors and Microsystems*
  - *Integration, The VLSI Journal*
  - *ACM Transactions on Design Automation of Electronic Systems*

- *Operating Systems Review*
- *Journal of Supercomputing*
- *IET Circuits, Devices & Systems*
- *IEEE IT Professional magazine*
- *International Journal of Network Management*
- *SciTechnol Journal*

- Technical Paper Reviewer/Referee for the following Conferences, Workshops, and Symposia: (multiple years of service: 1990 – present)
  - *International Symposium on High Performance Computer Architecture (ISHPCA)*
  - *International Conference on Parallel Processing (ICPP)*
  - *International Conference on Parallel and Distributed Computer Systems (ICPDS)*
  - *International Parallel (and Distributed) Processing Symposium (IPDPS)*
  - *International Joint Conference on Artificial Intelligence (IJCAI)*
  - *International Symposium on Computer and Information Sciences (ISCIS)*
  - *International Symposium on Circuits and Systems (ISCS)*
  - *International Symposium on Low Power Electronics and Design (ISPLED)*
  - *International Conference on Engr. of Reconfigurable Systems and Alg. (ERSA)*
  - *NASA/DoD Conference on Evolvable Hardware (EH)*
  - *European Design and Test Conference (EDTC)*
  - *SPIE Aerosense Symposium (Aerosense)*
  - *Hawaii International Conference on Systems Sciences (HICSS)*
  - *International Conference on Field Programmable Logic and Applications (FPL)*
  - *Genetic and Evolutionary Computation Conference (GECCO)*
  - *International Conference on Evolvable Systems (ICES)*
  - *IEEE Symposium Series on Computational Intelligence (IEEE SSCI)*
- Conference Technical Session Chair and/or Organizer:
  - "Runtime Resource Management of Reconfigurable Hardware"– *International Conf. on Engineering of Reconfigurable Systems and Algorithms, 2007*
  - "Runtime Reconfiguration Resource Management"– *International Conf. on Engineering of Reconfigurable Systems and Algorithms, 2006*
  - "Distributed and Heterogeneous Reconfigurable Systems"– *International Conference on Advances in Computer Science and Technology, 2006*
  - "Computer Architecture"– *International Conference on Advances in Computer Science and Technology, 2006*
  - "Adaptive Self-Repair of Reconfigurable Devices" – *NASA/DoD Conference on Evolvable Hardware, 2005*
  - "Device & Circuit Design" – *International Conference on VLSI, 2004*
  - "System/Network-on-a-Chip" – *International Conference on VLSI, 2004*
  - "Logic Design" (with H. Michel) – *International Conference on VLSI, 2004*
- Panelist: IEEE Member Rank Elevation Panel – consisting of IEEE Senior Members and Fellows whom determine increases to Senior Member rank among IEEE applicants, 2005

B. National and Regional

- Proposal/Award Reviewer:
  - National Science Foundation
    - *Computer and Information Science and Engineering (CISE) Division*
    - *U.S.-Argentina Collaborative Research*
    - *Graduate Research Fellowship Program* - panelist
  - American Society for Engineering Education, Southeast Section
    - Referee for *Outstanding Researcher Award*
- President: Computer and Technology Division – ASEE Southeast Section: 1999 – 2000
- Vice President: Computer and Technology Division – ASEE Southeast Section: 1998 – 1999
- Technical Program Committee:
  - *IEEE Southcon / Southeastcon Conference*: 1994, 1998
  - *ASEE Southeastern Conference*: 1998, 1999
- Conference Technical Session Chair/Organizer:
  - "Parallel Processing Architectures" – *IEEE Southcon Conference*: 1994, 1998
  - "Computing in Education" – *IEEE Southcon / Southeastcon Conference*: 1998, 1994
- Technical Paper Reviewer/Referee for Conferences:
  - *IEEE Southcon / Southeastcon*
  - *ASEE Southeastern Conference*
- External Promotion and Tenure Evaluator:
  - Multiple universities
- Textbook Reviewer:
  - McGraw-Hill Publishers: Higher Education Division
  - CRC Press
  - Wiley & Sons (invited for 2 different texts)

C. University-Level

- Undergraduate Course Review Committee: 2015 – 2016
- University TIP/RIA/SOTL Awards Committee: 2014 – 2015
- University Promotion and Tenure Committee: 2007 – 2008
- University SOTL Award Selection Committee: 2011 – 2012
- Graduate Research Forum: 2010 – 2011, 2009 – 2010
- Graduate Council: 2004 – 2005
- Faculty Senate: 2005 – 2006, 2004 – 2005
- Commencement Marshall: 2003, 1997, 1994
- Faculty Advisor to IEEE Student Organization: 1995 – 1996, 1994 – 1995, 1993 – 1994

D. College-Level

- EPC Staff Member Hiring Committee: 2015 – 2016
- Graduate Program College Council: 2009 – 2013

- Teaching Award Criteria Committee: 2007 – 2008, 2003 – 2004, 1999 – 2000
- Accreditation Committee: 2006 – 2007, 2007 – 2008, 2008 – 2009, 2009 – 2010
- Engineering Graduate Council: 2004 – 2005
- In-House Grant Selection Committee: 2004 – 2005, 2003 – 2004
- Research Council: 2003 – 2004
- Teaching Award Selection Committee: 2000 – 2001, 1997 – 1998
- Research Award Selection Committee: 2004 – 2005, 2009 – 2010
- Computing Resources Committee: 2000 – 2001, 1999 – 2000, 1997 – 1998, 1995 – 1996, 1994 – 1995
- Dean's Advisory Board: 1994 – 1995

E. Department-Level

- Academic Issues:
  - Department Chair 5-Year Review Committee: 2015 – 2016
  - State Program Review Committee: 2010 - 2011
  - Lab / Computer Systems Committee: 2016 – 2017, 2015 – 2016, 2010 – 2011, 2009 – 2010, 2008 – 2009, 2007 – 2008, 2006 – 2007, 2005 – 2006, 2004 – 2005, 2003 – 2004, 2000 – 2001, 1999 – 2000, 1998 – 1999, 1997 – 1998, 1996 – 1997, 1995 – 1996, 1994 – 1995, 1993 – 1994
  - Graduate Program Committee: 2014 – 2015, 2010 – 2011, 2009 – 2010, 2005 – 2006, 2004 – 2005, 2003 – 2004, 1999 – 2000, 1998 – 1999, 1994 – 1995, 1993 – 1994
  - Undergraduate Curriculum Committee: 2016 – 2017, 2015 – 2016, 2005 – 2006, 1997 – 1998, 1996 – 1997, 1994 – 1995
  - Accreditation Committee(s): 2014 – 2015, 2013 – 2012, 2012 – 2011, 2010 – 2011, 2009 – 2010, 2008 – 2009, 2007 – 2008, 2006 – 2007, 2000 – 2001, 1997 – 1998, 1994 – 1995
  - Undergraduate Curriculum Revision and Merging: 2009 – 2010, 2006 – 2007
  - Graduate Qualifying Exam Format Ad Hoc Committee: 2007 – 2008, 2006 – 2007
- Planning and Development:
  - Administrative Committee: 2014 – 2015, 2013 – 2012, 2012 – 2011, 2010 – 2011, 2009 – 2010
  - Advsiory Committee: 2016 – 2017, 2015 – 2016, 2014 – 2015, 2013 – 2012, 2012 – 2011, 2010 – 2011, 2009 – 2010
  - Faculty Mentor assigned to Junior ECE Faculty: 2016 – 2017, 2015 – 2016, 2014 – 2015, 2014 – 2013, 2013 – 2012, 2011 – 2012, 2010 – 2011 (2 faculty), 2009 – 2010, 2008 – 2009, 2007 – 2008, 2006 – 2007, 2005 – 2006, 2004 – 2005, 2003 – 2004, 2002 – 2003
  - Strategic Planning Committee: 2013 – 2014, 2010 – 2011, 2004 – 2005
  - Ph.D. Fellowship Committee: 2004 – 2005, 2000 – 2001
  - Industrial Advisory Committee: 2014 – 2015, 1994 – 1995
  - Indonesia Exchange Committee: 1994 – 1995
- Infrastructure and Operations:
  - Engineering III Building Committee: 2004 – 2005
  - Laboratory Committee: 2016 – 2017, 2015 – 2016, 2001 – 2002, 1999 – 2000, 1997 – 1998, 1995 – 1996
  - Computing Resources Committee: 1999 – 2000, 1997 – 1998, 1995 – 1996, 1994 – 1995

  - Lab Director: Microprocessor Lab, Open Computing Lab, Computer Architecture Lab: 1993 – present
  - Lab Faculty: Intelligent Systems Lab, VLSI Lab: 1998 – 2004

- Evaluation and Recognition:
  - Evaluation Standards Committee: 2015 – 2016, 2014 – 2015, 2011 – 2012
  - Faculty Excellence Awards Committee: 2005 – 2006
  - Promotion and Tenure Committee: 2016 – 2017, 2015 – 2016, 2014 – 2015, 2014 – 2013, 2013 – 2012, 2011 – 2012, 2010 – 2011, 2005 – 2006, 2004 – 2005, 2003 – 2004, 2002 – 2003, 1999 – 2000
  - Promotion and Tenure Guidelines Committee: 2005 – 2006, 2004 – 2005
- Merit Raise Guidelines Committee: 2014 – 2005
- Recruiting:
  - Faculty Search Committee: 2015 – 2016, 2014 - 2015, 2009 – 2010, 2006 – 2007, 2005 – 2006, 2003 – 2004, 2000 – 2001, 1998 – 1999, 1997 – 1998, 1996 – 1997, 1995 – 1996, 1994 – 1995
  - Department Chair Search Committee: 2003 – 2004
  - Staff Search Committees: 2015 – 2016, 2010 – 2011, 2009 – 2010, 1995 – 1996, 1994 – 1995

F. Academic Program Leadership

- Computer Engineering Program Coordinator

  Computer Engineering Undergraduate and Graduate Degree Programs and their Administration

  University of Central Florida, Department of EECS: 2010 – 2015
  - Determined CpE course offerings and submit teaching requests
  - Addressed accreditation issues and curriculum renewal specific to CpE degree program and CpE-specific courses
  - Orchestrated allocation of CpE program-specific resources
  - Coordinated strategic planning issues including enrollment trends and faculty recruiting
  - Maintenance of degree requirements, catalogs, and coordination of Bachelors of Science, Masters of Science, and Ph.D degree programs
- Graduate Coordinator

  Master of Science program in Computer Engineering, Masters of Science program in Electrical Engineering, Ph.D. program in Computer Engineering, Ph.D. program in Electrical Engineering, Accelerated BS+MS degree program in Computer Engineering, Accelerated BS+MS degree program in Electrical Engineering

  University of Central Florida, School/Department of EECS: Dec. 2009 – August 2012
  - Chaired and convened the ECE Graduate Committee, taking care of all graduate matters, such as curriculum changes, new course recommendations, new graduate policies, Qualifying review decisions, etc.
  - Processed admissions of new MS and Ph.D. students in EE and CpE Programs on a daily rolling basis
  - Reviewed and approved the Programs of Study for MS and Ph.D. students including revisions

- Assigned and oversaw contracting of 35 to 40 Teaching Assistants and/or Graders each semester to specific courses
- Hired and trained three dedicated staff members to support ECE Graduate Office
- Organized and coordinated the Qualifying Reviews and Annual Reviews of all Ph.D. students
- Reviewed the portfolios of non-thesis Master students
- Oversaw the fellowship and TA stipends' allocation for new incoming Ph.D. students
- Conducted Graduate Orientation seminar each Fall and Spring for newly admitted students
- Advised on daily basis EE and CpE graduate students on questions regarding admissions, programs of study, petitions, etc.
- Certified students for graduation at end of every semester
- Revamped joint faculty appointment criteria
- Processed regular and special topic Course Action Requests, Graduate Scholar requests, and Catalog revisions, and Articulation updates
- Designed an electronic database flow for graduate students towards electronic record-keeping of all their achieved milestones.
- Conducted graduate affairs at ECE faculty meetings.

- Accreditation Coordinator

University of Central Florida, School of EECS: 2009 – 2010, 2008 – 2007 (CpE), 2007 – 2008 (CpE), 2006 – 2007 (CpE)

- organized ABET accreditation and SACS assessment activities
- led curriculum renewal and laboratory revitalization efforts

- Associate Chair and Computer Engineering Program Coordinator

ECE Department, University of Central Florida, ECE Department: 1994 – 1995

- led curriculum renewal and laboratory revitalization efforts
- organized ABET accreditation and SACS assessment activities
- developed advising procedure and determined course scheduling/staffing and petitions
- supervised Computer Technicians, Administrative Staff, Student Assistants

- Founding Director
  - UCF Evaluation and Proficiency Center, 2014-present
  - 120-seat integrated testing and tutoring center

G. Academic Committee Chairship

- Chair, EECS/ECE Department Digital Systems and Computer Architecture Technical Area Committee: 2014 - 2015, 2013 - 2014, 2011 – 2012, 2010 – 2011, 2009 – 2010, 2007 – 2008, 2006 – 2007, 2005 – 2006, 2004 – 2005, 2003 – 2004, 2000 – 2001, 1997 – 1998, 1995 – 1996, 1993 – 1994
- Chair, ECE Department Evaluation Committee: 2004 – 2005
- Chair, School of Electrical Engineering and Computer Science Promotion and Tenure Committee: 2009 – 2010 (evaluated eleven faculty), 2005 – 2006 (evaluated eleven faculty), 2002 – 2003 (evaluated 7 faculty)
- Chair, ECE Department Faculty Search Committee: 2015 – 2016 (2 faculty hired), 2014 – 2015 (1 faculty hired), 2011 – 2012 (1 faculty hired), 2011 – 2012 (1 lecturer hired), 2009 – 2010 (3 faculty hired), 2006 – 2007 (4 faculty hired), 2000 – 2001 (3 faculty hired), 1996 – 1997 (1 faculty hired), 1994 – 1995 (3 faculty hired)

- Chair, College of Engineering Teaching Award Criteria Committee: 2005 – 2006, 1999 – 2000
- Chair, College of Engineering Teaching Award Selection Committee: 1997 – 1998
- Chair, ECE Department Computing Resources Committee: 1997 – 1998, 1995 – 1996, 1994 – 1995
- Chair, ECE Department Technician Search Committee: 1995 – 1996
- Chair, ECE Department Laboratory Committee: 1995 – 1996
- Chair, ECE Department Indonesia Exchange Committee: 1994 – 1995
- Chair, ECE Department Accreditation Committee: 1994 – 1995

VII. Affiliations and Certifications

A. Professional Societies

- Senior Member of *Institute of Electrical and Electronics Engineers (IEEE)* (current)
- Member of *Association for Computing Machinery (ACM)* (current)
- Member of *American Society for Engineering Education (ASEE)* (current)

B. Professional Certification

- State of California, Board of Engineers
  Registered Professional Engineer – Electrical Engineer, License Number E–13860 (current)
- University of Central Florida
  Online Course Development Certification – 80 contact hours IDL6543 completion, May 16, 2016

VIII. Honors and Awards

A. Teaching

- *Scholarship of Teaching and Learning (SoTL) Award*: for "outstanding contributions to the scholarship of teaching and learning within discipline or to the teaching and learning community" University-level, University of Central Florida, 2016 – 2017.
  – Monetary Amount: $5,000 permanent increase to 9-month salary
- *Teaching Initiative Program (TIP) Award:* for "sustaining high levels of teaching effectiveness" University of Central Florida, 2016 – 2017.
  – Monetary Amount: $5,000 permanent increase to 9-month salary
- *Excellence in Undergraduate Teaching:* College of Engineering and Computer Science, University of Central Florida, February, 2017.
  – Monetary Amount: $2,000 award
- *iSTEM Fellow:* 2015-2016 Academic Year
  – Monetary Amount: $20,000 discretionary funding for educational research
- *Outstanding Engineering Educator – IEEE Southeastern United States*:
  Joseph M. Bidenbach Outstanding Engineering Educator Award
  IEEE Professional Society – Region 3, April, 2008.
  – Citation: "For Outstanding Contributions to Engineering Education in Computer Architecture and Intelligent Systems."
  – Award winner chosen from over 30,000 IEEE members in IEEE global Region 3.

– IEEE Region 3 encompasses the southeastern United States and includes the states of Alabama, Florida, Georgia, areas of Indiana, Kentucky, Mississippi, North Carolina, South Carolina, Tennessee, Virginia and the country of Jamaica.

- *Outstanding Engineering Educator – Florida*: IEEE Florida Council, December, 2007.
- *Outstanding Engineering Educator – Orlando Section*: IEEE Orlando Section, September, 2007.
- *Scholarship of Teaching and Learning (SoTL) Award*: for "outstanding contributions to the scholarship of teaching and learning within discipline or to the teaching and learning community" University-level, University of Central Florida, 2008 – 2009.
  – Monetary Amount: $5,000 permanent increase to 9-month salary
- *Teaching Initiative Program (TIP) Award:* for "sustaining high levels of teaching effectiveness" University of Central Florida, 2006 – 2007.
  – Monetary Amount: $5,000 permanent increase to 9-month salary
- *Excellence in Graduate Teaching*: UCF Dept. of Electrical and Computer Engr., 2004 – 2005.
- *Teaching Initiative Program (TIP) Award:* for "sustaining high levels of teaching effectiveness" University of Central Florida, 2001 – 2002.
  – Monetary Amount: $5,000 permanent increase to 9-month salary
- *Web-based Course Development Award*: IEEE Southeastcon, 1998.
- *Teaching Initiative Program (TIP) Award:* for "sustaining high levels of teaching effectiveness" State University System of Florida, 1996 – 1997.
  – Monetary Amount: $5,000 permanent increase to 9-month salary
- Nominated for *Humphrey Teaching Assistant Award*: Lehigh University, 1986 – 1987.

B. Research

- *Paper of the Month:* IEEE Transactions on Computers, May 2017, with hosted companion video featured on IEEE Transactions webpage:
  "Energy-Aware Adaptive Restore Schemes for MLC STT-RAM Cache," accepted to *IEEE Transactions on Computers*, in-press, accepted 1 November 2016.
- *Conference Best Paper Candidate / A Best Paper of Track:*
  "Variation-Immune Resistive Non-Volatile Memory using Self-Organized Sub-Bank Circuit Designs," in *Proceedings of 18th International Symposium on Quality Electronic Design (ISQED-2017)*, Santa Clara, CA, USA, March 13 – 15, 2017.
- *Highlighted Article*: IEEE Circuits and Systems (CAS) Society International Symposium (ISCAS) selection for lecture presentation as a highlighted Transactions article of the past year:
  "Energy and Delay Tradeoffs of Soft Error Masking for 16nm FinFET Logic Paths: Survey and Impact of Process Variation in Near Threshold Region," accepted to *IEEE Transactions on Circuits and Systems II*, in-press, accepted 16 April, 2016.
- *Highlighted Article of Issue:* IET Electronics Letters, June 2016:
  "Compact Low-Power Instant Store and Restore D Flip-Flop using a Self-Complementing Spintronic Device," *IET Electronics Letters (IEEE-indexed)*, Vol. 52, No. 14, pp. 1238 – 1240, June 2016. DOI: 10.1049/el.2015.4114.

- *Paper of the Month*: IEEE Transactions on Computers, June 2016, with hosted companion video featured on IEEE Transactions webpage:

  "Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks," *IEEE Transaction on Computers*, Vol. 65, No. 6, June 2016, pp. 1789 – 1801. DOI: 10.1109/TC.2015.2458866.

- *Best Paper Award*: NASA/ESA Conference on Adaptive Hardware and Systems, Citation: "Best Design Paper of Conference:"

  S. D. Pyle, V. Thangavel, S. M. Williams, and R. F. DeMara, "Self-Scaling Evolution of Analog Computation Circuits with Digital Accuracy Refinement," in *IEEE Proceedings of NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2015)*, Montreal, QC, Canada, June 15 – 18, 2015. *Best paper award of conference, Citation: "Best Design Paper."*

- *Research Initiative Award (RIA):* "for outstanding research, scholarly, and creative activity" University of Central Florida, 2008 – 2009.
  – Monetary Amount: $5,000 permanent increase to 9-month salary

- *Best Paper Award*: International Conference On Field Programmable Logic, Place and Route session

  R. S. Oreifej, R. N. Al-Haddad, H. Tan, R. F. DeMara, "Layered Approach To Intrinsic Evolvable Hardware Using Direct Bitstream Manipulation Of Virtex II Pro Device," in *Proceedings of the 17th International Conference On Field Programmable Logic And Applications (FPL'07*), Amsterdam, Netherlands, August 27 – 29, 2007. Conference acceptance rate 21%. Selected as best paper of track and nominated for best of conference.

- *Distinguished Researcher*: UCF College of Engineering and Computer Science, 2004 – 2005, Associate Professor level.

- *Best Paper Award*: WMSCI'05, Network Security Technologies session
  G. Wang, R. F. DeMara, A. J. Rocke, "Mobility-Enhanced File Integrity Analyzer For Networked Environments," in *Proceedings of the 9th World Multi-Conference on Systemics, Cybernetics and Informatics (WMSCI '05)*, pp. 341 – 346, Orlando, FL, U.S.A., July 10 – 13, 2005. Received *Best Paper Award*, Network Security and Security Technologies.

- *Researcher of the Year*: UCF Department of Electrical and Computer Engr., 2003 – 2004, Associate Professor level

- *Research Initiative Award (RIA):* for *"outstanding research, scholarly, and creative activity"* University of Central Florida, 2003 – 2004.
  – Monetary Amount: $5,000 permanent increase to 9-month salary

- *Distinguished Research Lecturer*: UCF College of Engineering, 2003 – 2004.
  – Monetary Amount: $2,000 one-time award

C. Service

- *Marchioli Collective Impact Innovation Award Finalist*, University of Central Florida, Spring 2017.
- *Excellence in Professional Service*: School of Electrical Engineering and Computer Science, 2008 – 2009.
- *Achievement Award*: International Multiconference in Computer Science and Computer Engineering, 2005.

- *Faculty Advisor of the Year*: UCF College of Engineering, 1994 – 1995.
- *Faculty Advisor of the Year*: UCF Dept. of Electrical and Computer Engineering, 1994 – 1995.
- Nominated for *IEEE Student Organization Advisor of The Year*, 1995.
- *Special Appreciation Award for Outstanding Employee Contribution*, IBM Corporation, Manassas, Virginia, 1989.

D. Other Recognition of Scholarship

- Marquis Who's Who in America
- Marquis Who's Who in Science and Engineering
- Eta Kappa Nu, Tau Beta Pi, and Phi Eta Sigma Honor Societies
- New York State *Regents Scholarship* and *Science Supervisors' Scholarship*
- Lehigh University Dean's List: semesters 1, 2, 3, 4, 6, 7, 8

IX. Personal Information

A. Citizenship

United States of America

B. Foreign Languages

New York Regents Certification in Spanish