

Guest Editorial: *IEEE Transactions on Computers* and *IEEE Transactions on Emerging Topics in Computing* Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures

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As facilitated by increases in integration density from technology scaling and the potential of beyond-CMOS device technologies, emerging innovations in reconfigurable computing fabrics span from the circuit-level through the application level. This Special Section focuses on the advancement of the associated performance and reliability objectives via technology and functional heterogeneity, as well as advanced resilience properties in which reconfigurable fabrics are embarking. Emerging device characteristics such as non-volatility and new static versus dynamic energy consumption profiles, as well as novel interconnect mechanisms, and storage blocks within reconfigurable fabrics, in turn innovate architectural advances that enable new applications. The manuscripts appearing in this Special Section focus on one or more of these innovations during the design-cycle phases including modeling, simulation, design, fabrication, and applications.

The main motivations for embracing reconfigurable fabrics such as Field Programmable Gate Arrays (FPGAs) still solidly remain along two categories of attributes: (1) *flexibility and accessibility*: fabric flexibility allows realization of logic elements at medium and fine granularities while incurring low non-recurring engineering effort and rapid deployment to market, and (2) *resiliency and runtime adaptability*: reconfigurable fabrics have been demonstrated to provide a viable solution for process-voltage-temperature variation induced concerns and can be utilized effectively for fault recovery. However, these advantages have traditionally been achieved at some cost of increased fabric area and power consumption, as well as a decrease in throughput compared to Application-Specific Integrated Circuits (ASICs). Innovations using emerging devices within reconfigurable fabrics which are highlighted in this Special Section have sought to bridge the gaps needed to provide more of these benefits at reduced energy and area costs.

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Currently, Static Random Access Memory (SRAM) cells form the basis for most commercial FPGAs. SRAM cells are employed within programmable switching elements to control the interconnection between logic building blocks. Moreover, they are utilized in Look-Up Tables (LUTs) to store the logic function configuration data, which constitute the primary components in reconfigurable fabrics. In particular, in conventional fabrics, each LUT is comprised by a memory with 2^m cells in which the truth table of an m -input Boolean function is stored. The re-programmability of the SRAM cells, and the fact that they can be readily implemented by highly-scaled CMOS technology, have traditionally resulted in SRAM-based FPGAs being the most popular reconfigurable fabrics on the market. Current challenges addressing SRAM cell are (1) *high static power*: due to the existence of intrinsic leakage current having a proportion that increases significantly with technology scaling, (2) *volatility*: SRAM is volatile, therefore all functions must be reprogrammed upon each power-up cycle, and (3) *low logic density*: SRAM cells are composed of six transistors which ultimately limits the logic density, as well as impacting the energy profile.

This issue highlights innovations in reconfigurable computing fabrics continuing their transition towards embracing the benefits of increased heterogeneity of SRAM and beyond-SRAM technologies, along several cooperating dimensions. These include new device technologies, such as Resistive Random Access Memory (RRAM), Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM), and inkjet configurable devices, as well as architectures and methods for fault-tolerance, and interconnect advancements including Via-based reconfigurability and networks-on-chip, while embracing applications spanning from physically unclonable functions to audio processing on a neuromorphic fabric.

This Special Section attracted roughly 30 submissions along with the involvement of nearly 120 reviewers who were selected for their expertise on the precise topics of each submission. Thus, it represents a collective effort from the research community and industry participants on an international scale. Overall, eleven manuscripts appear in this joint Special Section. Among the submissions, four articles focused on topic areas including beyond-CMOS and alternative device technologies are being published in *IEEE Transactions on Emerging Topics in Computing*. Meanwhile, seven additional manuscripts are published in *IEEE Transactions on Computers* focused on resilience, interconnect design, low-energy reconfigurable devices, and application-specific fabrics. Articles appearing in this Special Section were also invited to prepare companion abstract videos, which if available will

appear on the *IEEE Transactions on Computers* portal page at <http://www.computer.org/web/tc>.

The utilization of emerging devices within reconfigurable fabrics is addressed through several approaches within the articles included in *IEEE Transactions on Emerging Topics in Computing*. The article “A High-performance FPGA Architecture Using One-Level RRAM-based Multiplexers” by Xifan Tang, Giovanni De Micheli, and Pierre-Emmanuel Gaillardon shows how Resistive RAM technology can be successfully applied to the routing of FPGA architectures. In particular, it is shown that RRAM-based routing multiplexers, can be employed to achieve significantly reduced delay compared to state-of-art SRAM-based implementations. Based on the specific features of RRAM multiplexers, the paper introduces FPGA architecture optimizations that significantly improve both Area-Delay Product and Delay-Power Product. Meanwhile, the manuscript “Energy Efficient Reconfigurable Threshold Logic Circuit with Spintronic Devices” by Zhezhi He and Deliang Fan develops an energy-efficient approach by intrinsically-supporting a threshold-based logic model. It focuses on reconfigurable threshold logic gates whereby a spintronic weight device enables the design of Spintronic Threshold Logic Gates (STLGs) within a reconfigurable fabric. This paper shows that the proposed STLG-based reconfigurable logic could provide important improvements with respect to state-of-the-art, including much lower Energy-Delay Product (EDP) compared with CMOS based FPGAs.

Another article addressing emerging technologies, titled “Inkjet-Configurable Gate Arrays” by Jordi Carrabina, Mohammad Mashayekhi, Jofre Pallarès, and Lluís Terés, illustrates how gate array configurations could be applicable to inkjet-printed circuitry. The authors show that using inkjets for the configuration layer of a regular gate array structure allows them to combine low cost of inkjet technology with the higher yield achieved via flexibility of a post-manufacturing reconfiguration phase.

Finally, interconnect innovations for reconfigurable fabrics are showcased within the manuscript “SAT-Based Formulation for Logical Capacity Evaluation of VIA-Configurable Structured ASIC” by Felipe Marranghello, Vinicius Dal Bem, André Reis, and Renato Ribas. It examines reconfigurable fabrics from the perspective of a new Via-Configurable Structured ASIC (VCSA) design. It proposes a satisfiability formulation for determining the logical capacity of a VCSA block template or fabric, thus looking at the optimal configuration of a regular fabric at manufacturing time. The proposed SAT formulation improves the performance over previous solutions while eliminating multiple iterations.

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Sincerely,

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