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Design-For-Diversity for Improved Fault-Tolerance of TMR Systems on FPGAs

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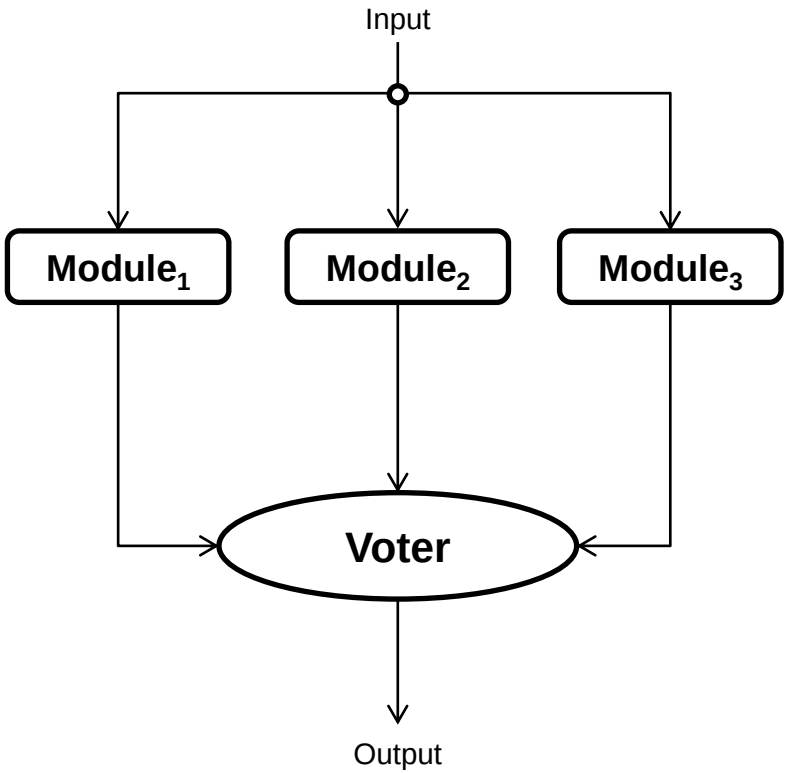
Agenda

- Introduction
- Related Work on Design Diversity Techniques
- Reliability Through Diversity (RTD) approaches
- Experiments & Results
- Conclusions
- References

Introduction

- Significance of Fault-Tolerant (FT) systems
- Redundancy is of the simplest employed methods in FT Systems
  - N-Modular Redundancy: N=2 is an example of a Concurrent Error Detection (CED) system and N=3 is the famous **T**riple **M**odular **R**edundancy (TMR)
- Characteristics of FPGA-based FT systems
  - Re-configurability
  - Quick Time-to-Market
  - Popular in Embedded Mission-Critical Applications



TMR System

Introduction

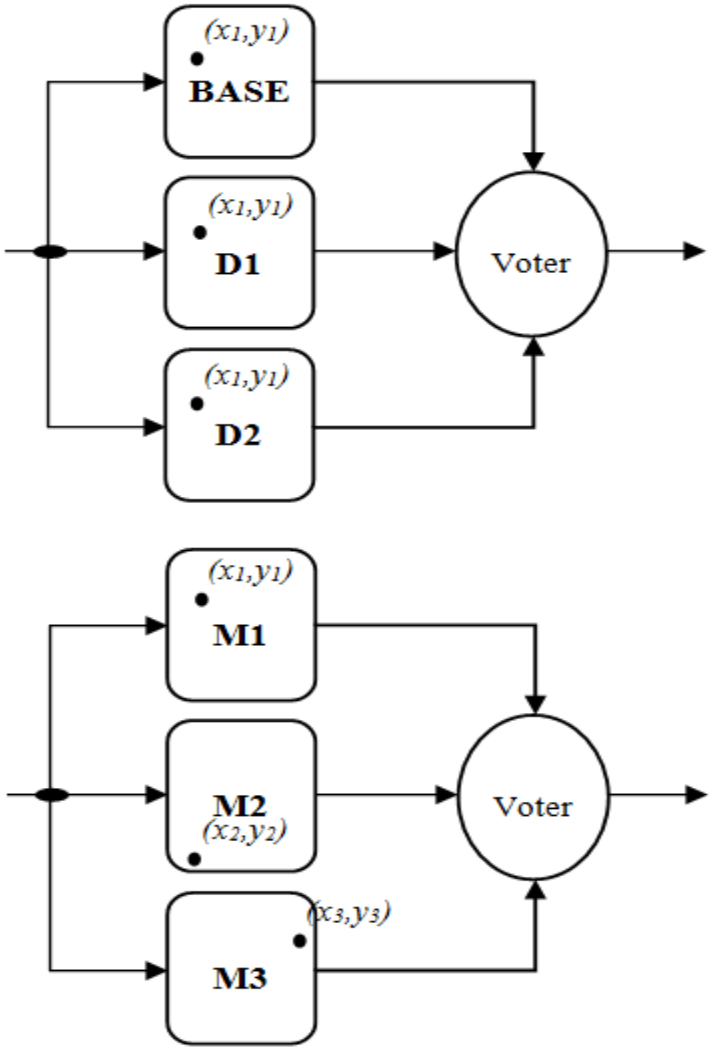
- Failure Modes:
  - Common Mode Failures (CMF):
    - Common?
    - Effects
  - Random Stuck-at Faults (RSF)

<u>Conventional TMR:</u>

- TMR relies on functionally identical systems:
  - Frequently, same “physical” design for all three modules

<u>RTD TMR:</u>

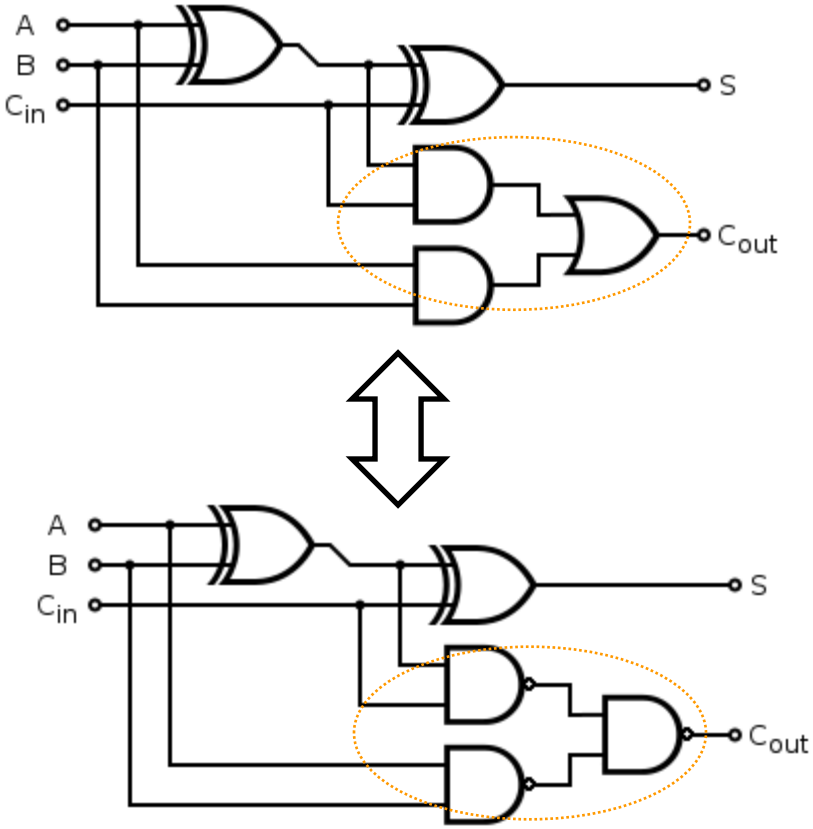
- Can diverse “physical” designs provide better Fault-Tolerance?
  - Concept of *functionally* identical, *physically* different



CMF vs. RSF

Introduction

- Use of **D**esign **D**iversity (DD) for overcoming permanent faults in FPGA
  - Scrubbing with Diverse Designs
  - Evolutionary algorithm based refurbishment
- Two Full-Adder Designs
  - Functionally identical, yet physically distinct



Related Work

- **Vigander[12]**: *Evolutionary-based repair techniques* partially repair the faulty modules in a satellite mission. TMR masks the faults from individual modules as diverse modules fail in different manners

- **Sharma[9]**: Diverse designs are generated through Place & Route to facilitate *Combinatorial Group Testing (CGT)* to isolate faulty modules

- **Keymeulen[5]**: Evolutionary methods are used to create fault-tolerant designs of an analog multiplier and an XNOR function on FPTA

- **Borges[2]**: Design diversity redundancy applied to mixed-signal (MS) circuit blocks, as a proposal to increase system reliability

Motivational Work

- **McCluskey[6]**: Quantify design diversity among designs in a CED configuration

Inputs	Fault-free Outputs	M1 Outputs	M2 Outputs
00	01	00	10
01	10	10	10
10	00	10	10
11	11	10	10

Fault Pair → Joint Detectability → Diversity of a single fault pair → Diversity

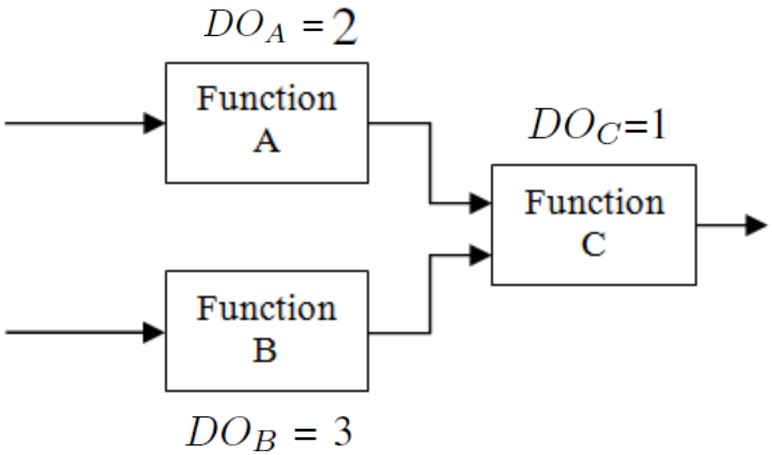
$$(f_i, f_j) \Rightarrow k_{i,j} \Rightarrow d_{i,j} = 1 - \frac{k_{i,j}}{2^n} \Rightarrow D = \frac{1}{m}\sum_{i,j} d_{i,j}$$

$$= 2 \qquad = 1 - \frac{2}{4} = 0.5 \qquad = 0.5$$

$$where, 0 \leq D \leq 1$$

Design Diversity Techniques

- 3 Design families investigated:
  - Template-based (TB)
  - Case-Based/Inverted-Output (CB/IO)
  - NAND/NOR realizations
- Rely on the synthesizer to provide different implementations of the functionality
- **Template-based**: Different designs of internal system blocks. Each implements a sub-functionality differently to precipitate system diversity

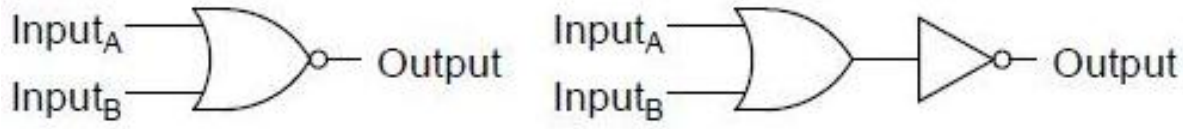


$$DO_{sys} = \prod_{i=A}^{C} DO_i$$

$$= DO_A \times DO_B \times DO_C$$

$$= 6 \text{ designs!}$$

Design Diversity Techniques



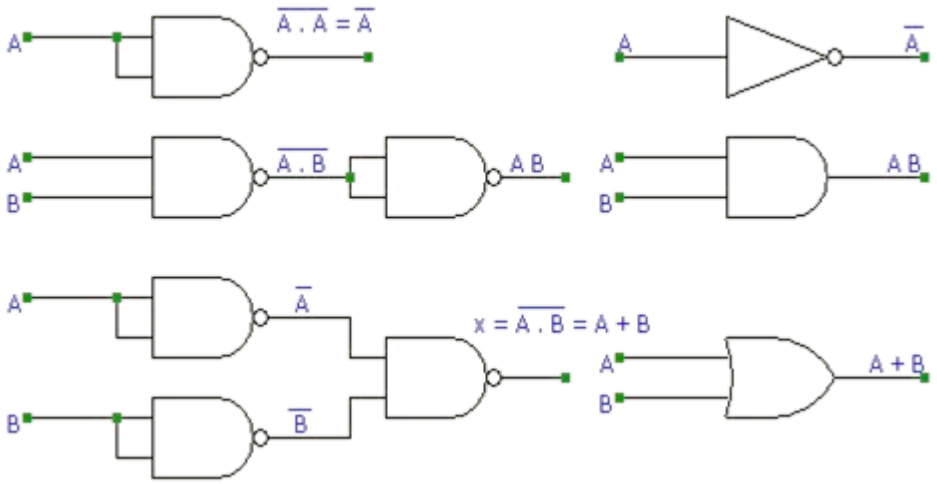
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

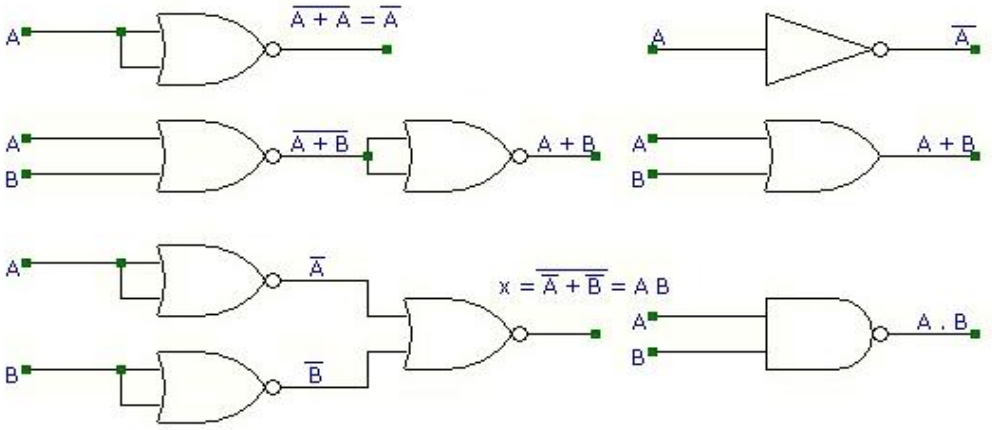
- **Case-based:** Define the functionality using *case* statement
  - **Inverted Output:** The function is described with *inverted* outputs. The final output is obtained through an inverter

DD Techniques

- NAND/NOR-based:
  - NAND/NOR gates can represent any basic Boolean function
  - Can be used to replace all LUTs in a design with NAND/NOR functions
  - This can be done by constraining the synthesizer to sample each LUT as a NAND/NOR, using **.UCF* file
  - Will provide a different design, but at a high area cost, since LUTs configured to emulate these basic gates



NAND-Based

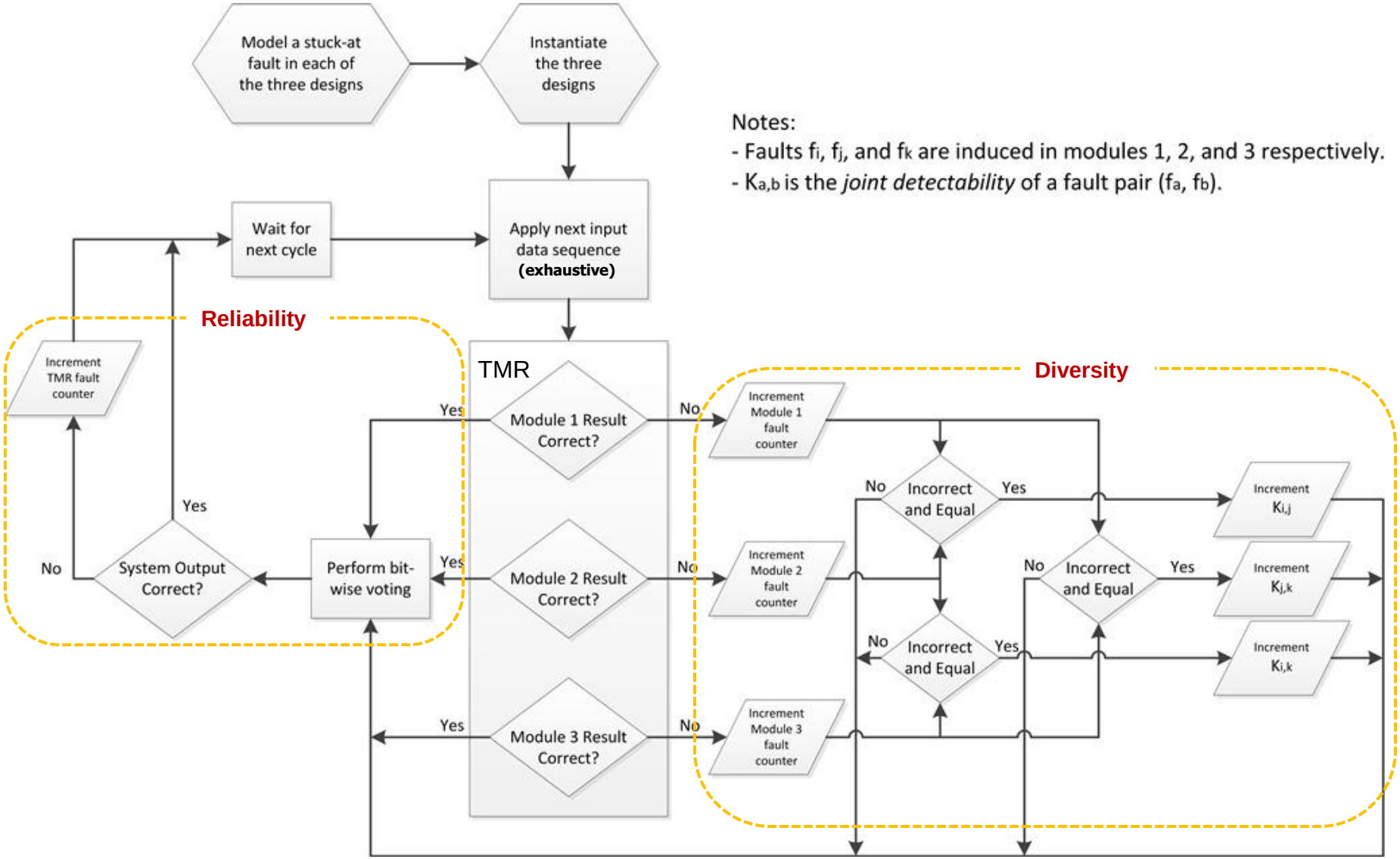


NOR-Based

Experimental Setup

- Xilinx ISE Design Suite 12.2 equipped with the ISim FPGA simulator
- Target configuration of Xilinx Virtex-4 FPGA Device
- Using a single stuck-at-0/1 fault model
- Injecting the fault manually by modifying the output of the post P&R simulation model:
  - Locate LUT to be injected with a fault by ID
  - Inject the fault at one of the LUT inputs (setting it to V_{dd} for 1, GND for 0)
- For CMF:
  - Inject the fault at the same input of the same LUT in all modules
- For RF:
  - Inject the fault at different LUTs in all designs
- Tested Circuits:
  - A 3x3-bit multiplier: A combinational circuit that provides a total of 6 inputs and 6 outputs
  - MCNC dk17 benchmark circuit: An 8-state Finite State Machine (sequential circuit) having 2 inputs and 3 outputs. It is also evaluated for all 32 state transitions

Experimental Flow



Experiments

- *In all experiments:*
  - *Reliability is calculated by:* $R = 1 - \frac{A}{2^n}$, where A is the number of erroneous outputs, and *n* is the number of inputs.
  - *A total of 72 faults are tested = (64 CMF and 8 RSF)*
  - *Bit-wise voter*
- *Experiment#1*:
  - Find inter/intra-design family diversity values
- *Experiment#2:*
  - Reliability of intra-design family TMR system in CMF
- *Experiment#3:*
  - Reliability of intra-design family TMR system in RSF
- *Experiment#4:*
  - Reliability of a homogenous TMR system
- *Experiment#5:*
  - Reliability of inter-design family TMR system in CMF

Results

- **Intra-Diversity**:
  - All design techniques increase diversity to fault pairs injected in different failure modes
  - However, a diversity metric close to 1 doesn't imply two designs are identical

DIVERSITY VALUE OBTAINED THROUGH COMPARISON WITH THE BASE DESIGN (3X3 MULTIPLIER)

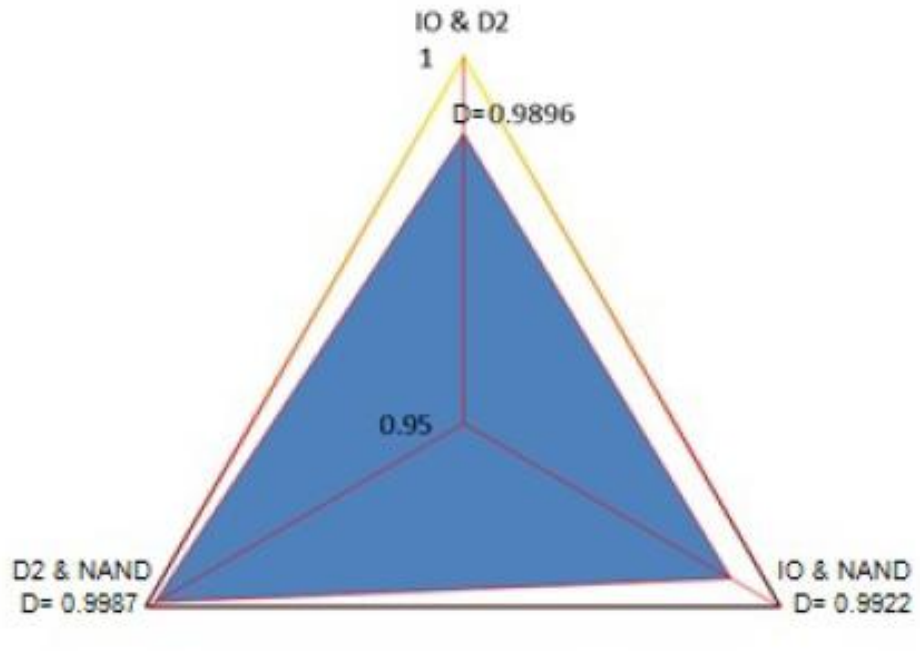
	D1	D2	CB	IO	NAND	NOR
CMF	1	0.996	1	0.987	0.965	0.958
RSF	0.971	1	0.984	1	0.992	1
Average Diversity Value	0.986	0.998	0.992	0.994	0.979	0.979

  - Siblings of the same-design family are diverse among each other

INTRA-DESIGN DIVERSITY VALUES (3X3 MULTIPLIER)

	D1 & D2	CB & IO	NAND & NOR
CMF	0.9956	0.9868	0.9731
RSF	0.9961	0.9844	0.9883
Average Diversity Value	0.9959	0.9856	0.9807

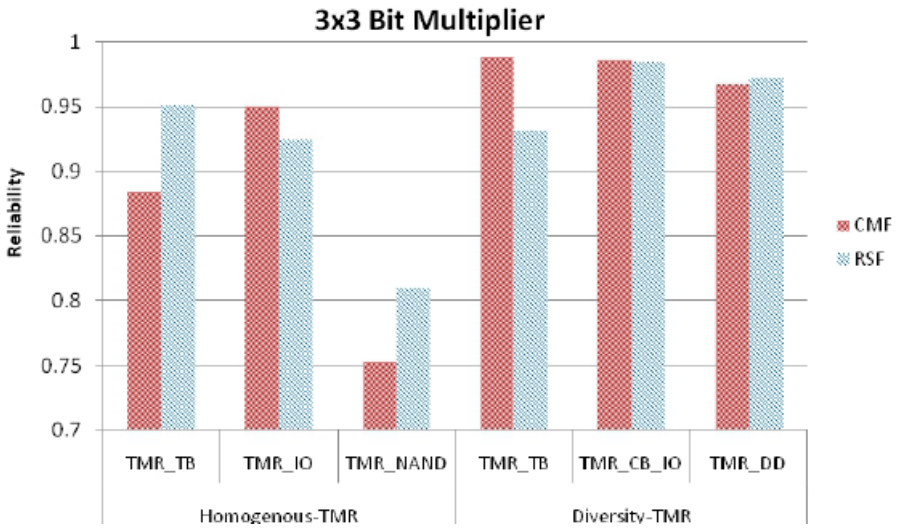
Experiments

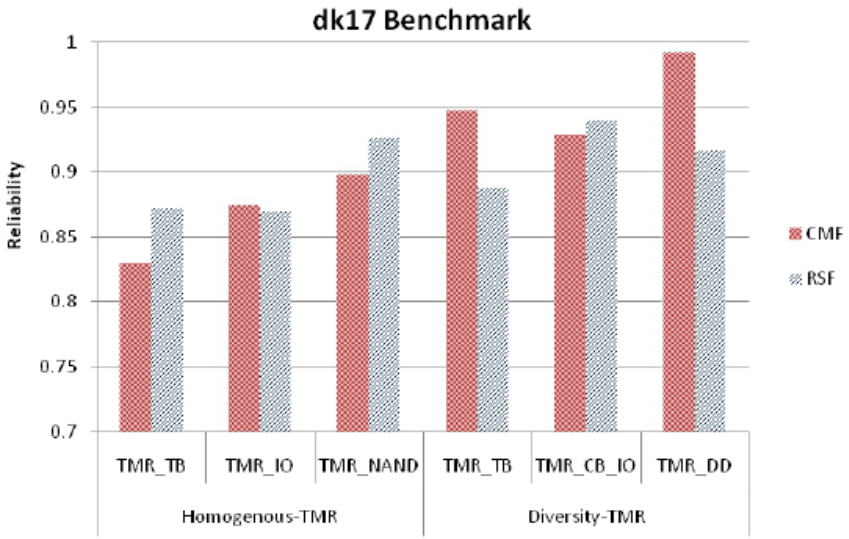


- **Inter-Diversity**:
  - All siblings of design techniques provide diverse designs when compared to each other

Results

- Reliability Value:
  - Homogenous vs. Diverse TMR:
    - All modules use the same physical design vs. using diverse designs
  - Test Modules:
    - **TMR_TB**: One module uses the BASE design and the other two use different designs obtained using template-based method.
    - **TMR_IO**: Inverted/Output
    - **TMR_NAND**: NAND-based.
    - **TMR_CB_IO**: Case-based/Inverted-output
    - **TMR_DD**: Module#1: TB, Module#2: IO, Module#3: NAND
  - Diversity-TMR has better reliability in CMF (~13%) and RSF (~10%) compared to Homogenous-TMR
  - Better overall reliability offered by TMR_DD





Conclusion & Future Work

- Proposed approaches offers **straightforward solutions to realizing diverse designs** with a low overhead (computation and memory) cost compared to other techniques (like evolutionary methods, for example).

- **Diverse-design-based TMR** systems exhibit **higher reliability** to CMF (~13%) and RSF (~10%), and using different design techniques offers improved reliability for randomly injected faults at minimal additional runtime cost and effort

- **Exhaustive testing of RSF** is required to further validate the conclusion

- **Improved design diversity metric is needed**: McCluskey's diversity metric was used by injecting fault pairs and recording exact fault responses of the design pairs. In some cases, the metric has a counterintuitive behavior as same designs show high design diversities when fault pairs were injected at different locations, which hints that this metric might be valid for CMFs only

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