State-Holding Spintronic Logic:

From Current-Based Switching to Voltage-Driven Operation

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Abstract

With semiconductor technology scaling approaching atomic limits, novel materials and physical phenomena are sought in order to realize new logic and memory devices. Spintronic devices offer intriguing avenues to improve digital circuits by leveraging nonvolatility to reduce static power dissipation and enable logic-in-memory approaches to computing. Novel hybrid spintronic-CMOS digital circuits are developed herein that illustrate enhanced functionality at reduced area cost. The developed spin-CMOS D Flip-Flop offers improved power-gating strategies by achieving instant store/restore capabilities while using 10 fewer transistors than typical CMOS-only implementations. The spin-CMOS Muller C-Element developed herein improves asynchronous pipelines by reducing the area overhead while adding enhanced functionality such as instant data store/restore and delay-element-free bundled data asynchronous pipelines. However, the static-current-based operation of contemporary spintronic devices is a great challenge towards realizing energy-efficient circuits.

STATE-HOLDING SPINTRONIC LOGIC:
FROM CURRENT-BASED SWITCHING TO VOLTAGE-DRIVEN OPERATION

by

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ABSTRACT

With semiconductor technology scaling approaching atomic limits, novel materials and physical phenomena are sought in order to realize new logic and memory devices. Spintronic devices offer intriguing avenues to improve digital circuits by leveraging *nonvolatility* to reduce static power dissipation and enable *logic-in-memory* approaches to computing. Novel hybrid spintronic-CMOS digital circuits are developed herein that illustrate enhanced functionality at reduced area cost. The developed spin-CMOS D Flip-Flop offers improved power-gating strategies by achieving instant store/restore capabilities while using 10 fewer transistors than typical CMOS-only implementations. The spin-CMOS Muller C-Element developed herein improves asynchronous pipelines by reducing the area overhead while adding enhanced functionality such as instant data store/restore and delay-element-free bundled data asynchronous pipelines. However, the static-current-based operation of contemporary spintronic devices is a great challenge towards realizing energy-efficient circuits.

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CHAPTER ONE: INTRODUCTION

Scalable, energy-efficient, and enhanced functionality over CMOS technology are all desirable characteristics for future computational devices. Emerging spintronic devices achieve greater functionality through nonvolatility and improved scalability via Back End of Line (BEoL) compatibility, which enables vertical integration. By utilizing these features, area-efficient designs with instant store/restore functionality can be achieved. However, developing an energy-efficient spintronic device has been a critical challenge towards the migration of computer architectures to spintronics. This Chapter introduces the need for spintronic logic devices, provides an overview of current spintronic logic approaches, defines the research objectives, and finally discusses the innovative hybrid spin-CMOS digital circuits developed as well as the novel low-energy spintronic logic device in the Contributions of Dissertation section.

Need for Spintronic Logic Devices

The Moore's Law scaling of CMOS devices has enabled the proliferation of computational technology in every facet of the information processing revolution since the 1960s. However, the fundamental limitations of CMOS scaling has necessitated the semiconductor industry to formally acknowledge that transistors will stop shrinking by the early 2020s, as emphasized by the chairman of the road-mapping organization [1]. Means for continuing Moore's Law could be through the development of a new compact nanoswitch having a lower energy-delay product that dissipates less heat than CMOS devices. Among promising devices, the 2015 International Technology

Roadmap for Semiconductors (ITRS) identifies nanomagnetic, or spintronic, devices as capable post-CMOS candidates [2].

Spintronic devices have the potential to operate at frequencies above 1 GHz and at energies approaching 40kT, where k is Boltzmann's constant and T is temperature [3]. Thus, they provide a direction for a scalable universal memory technology, which is in contrast to today's current memory systems that are segmented between SRAM for high speed/high area, DRAM for moderate speed/low area, and Flash or magnetic platters for very low speed/very low area data storage. Additionally, the features of spintronic devices enable new classes of logic elements that, in contrast with CMOS, intrinsically hold their state without any external power signals. This feature can provide novel circuit and architectural strategies leveraging power-gating for reduced energy consumption and heat generation, as well as the development of computational datapaths that minimize data movement from the computational elements and memory elements since each logical element can act as intermediary memory.

Spintronic Approaches to Logic and Memory

In this Section, the spintronic physical phenomena outlined in Figure 1 is delineated. One of the first mechanisms by which spintronic information is utilized is Spin Transfer Torque (STT). STT is the magnetic force used to switch nanomagnets by injecting a spin-polarized current. Similar to how a polarizer only allows photons of a particular polarization to pass through it, spin-polarization is the effect by which the spin-orientation of electrons align with the spin-orientation of a magnet when a current is passed through it. If electrons of one spin orientation meet an electron

of differing orientation, then a net magnetic torque is applied, which is STT. STT will be used in Chapter 3 to realize novel hybrid spin-CMOS digital circuits.

The Magnetic Tunnel Junction (MTJ) is a physical phenomena whereby a material stack of a thin, one or two nanometers, insulating oxide is sandwiched between two Ferromagnets (FM) has different resistances based on the relative magnetic orientations of the two FMs [4-15,43]. If the two FMs are parallel, then the MTJ has its lowest resistance, and if they are anti-parallel, then the MTJ has its highest resistance. MTJ devices can be switched via STT. MTJs will be used in Chapter 3 to realize novel hybrid spin-CMOS digital circuits.

Domain Wall Motion (DWM) is a phenomena whereby two regions with opposing magnetic orientations in the same FM wire have a region between the two called the domain wall [4, 5]. By applying STT to the domain wall it will move in the direction of the electron flow, which allows current-based manipulation of a magnetic region [42]. DWM will be used in Chapter 3 to realize novel hybrid spin-CMOS digital circuits.

Spin Orbit Coupling (SOC) effects such as the Spin Hall Effect (SHE) and the Rashba-Edelstein Effect (REE) are mechanisms by which particular materials cause electrons of one spin orientation to flow opposite to those of opposite orientation [6-13]. The SHE is a bulk phenomena found in heavy metals such as Pt or beta-W [40-42]. The REE is a surface phenomena found in Topological Insulators (TI) such as Bi_2Se_3. Regardless of the exact phenomena, SOC effects found in spintronic devices operate by either passing a charge current through the material in order to inject a spin current into FMs placed on top of the material or by transducing a spin-state by injecting spin-polarized electrons into the SOC material and reading the charge current produced

[3]. The latter effect is deemed the Inverse Spin Orbit Coupling (ISOC) effect. SOC effects typically result in very high efficiency spin injection and detection and as such has been at the forefront of the latest in spintronic device research. SOC will be used in Chapter 4 to realize an energy-efficient concatenable spintronic device.

The Magnetoelectric Effect (ME) is a highly active area of research towards voltage-controlled manipulation of magnetic states as opposed to current-based methods such as STT [3, 14-30]. A summary description of the ME is that a particular material or heterostructure is able to induce a magnetic field in adjacent magnetic materials based upon an electric field within the ME material/structure. There are two primary mechanisms by which the ME is mediated, the magnetostrictive mechanism and the exchange-bias mechanism. The magnetostrictive mechanism operates with a heterostructure of a piezoelectric material, such as PMN-PT, and a magnetostrictive material such as Terfenol-D [14, 15, 19, 23, 24, 27]. By applying a voltage across the piezoelectric material, the electric field causes a strain that is then transferred to the magnetostrictive material. Due to the strain in the magnetostrictive material, its magnetization will rotate. Although the magnetostrictive mechanism has demonstrated very strong coupling between the electric and magnetic fields, it can only induce a 90 degree rotation of the magnetostrictive layer, whereby it is desired to have deterministic 180 degree rotation in spintronic logic and memory devices. The exchange-bias mechanism is typically found in ferroelectric-antiferromagnetic multiferroic materials [3, 16, 20-22, 24, 26, 29, 30]. Due to the coupling of the ferroelectric and antiferromagnetic domains of the material, a switching of the polarization by an electric field can switch the antiferromagnetic state of the material. If a FM is interfacially coupled

to the multiferroic material, then there is an exchange bias-mediated magnetic field applied to the FM according to the orientation of the interfacial magnetic states of the multiferroic material, which can be switched by switching the polarization with an electric field. Although the exchange-bias mediated ME has demonstrated deterministic 180 degree switching, the coupling between the electric and magnetic fields is much lower than that for the magnetostrictive-mediated ME. The ME will be used in Chapter 4 to realize an energy-efficient concatenable spintronic device.
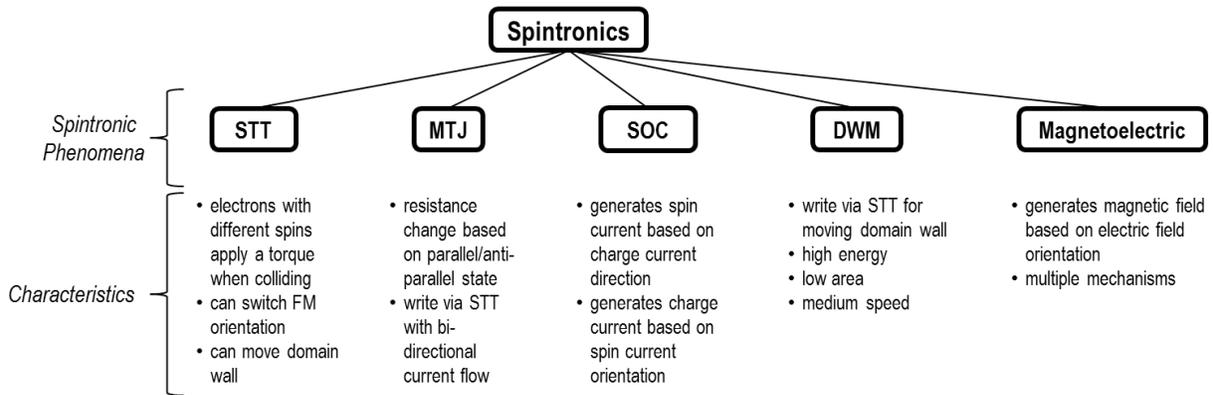

Figure 1: Taxonomy of spintronic phenomena and their characteristics.

CHAPTER TWO: RELATED WORK

Previous Spintronic Logic Device Schemes

The search for energy-efficient spintronic logic devices has produced a number of novel schemes to realize the five essential characteristics of a logic device: concatenability, gain, input/output isolation, non-linearity, and directionality. In this Chapter, several spintronic logic devices utilizing a number of physical phenomena are presented and discussed.

All Spin Logic

All Spin Logic as proposed by Behin-Aein et al. is a method of employing Ferromagnets (FMs) to spin-polarize charge current into a Non-Magnetic (NM) conductor with long spin diffusion lengths, such as Cu, for logic operations [31-35]. The FM acts upon charge current similar to how a polarizer acts on photons; the electrons passed through the FM spin-polarizes to the orientation of the FM. However, this effect does not spin-polarize all electrons, but a majority of them. Thus, by passing electrons through the FM and into a NM conductor, a buildup of electrons with spin orientation of the FM is produced in the NM conductor. This buildup of electrons diffuses across the conductor, which can be described as a spin-current that exponentially decays the further it is from the input FM. By placing an output FM connected to the NM channel close enough to the input FM, the generated spin current can switch the output FM. By connecting multiple input FMs to the same NM channel with an output NM, logical operations based on majority logic can be realized. Thus, a spintronic logic scheme is achieved. However, the static

charge current required for All Spin Logic in conjunction with the exponential decay of spin current in the NM conductor leads to power-inefficient and slow operation with interconnect length constraints.

Spin Switch

The *Spin Switch* as proposed by Datta et el. combines SHE-based switching with MTJ-based state-transduction and dipolar coupling for input/output isolation in order to realize a comprehensive spintronic logic element with charge-mediated interconnects [7, 36]. The Spin Switch is switched by passing a charge current through a SHE material interfacially coupled to a FM called the Write Unit FM (W-FM). Based on the direction of the charge current, a positive or negative spin-current is injected into the FM and is able to switch the FM if the magnitude and pulse duration are great enough based on the STT generated from the SHE material. The W-FM is dipolar coupled to a nearby, but electrically isolated FM called the Read Unit FM (R-FM). The Spin Switch is constructed such that when the W-FM is switched, the R-FM is switched due to the dipolar coupling. The R-FM acts as the free layer to two MTJs with complementary fixed layers. Since the fixed layers are complementary, one will be a high resistance and the other will be a low resistance, exclusively, based on the state of the R-FM. The supply terminal of one MTJ is connected to a positive voltage source and the supply terminal of the other MTJ is connected to a negative voltage source of the same magnitude. The output of the Spin Switch is connected to the R-FM. Based on the state of the R-FM, the direction of the output charge current will be that of the supply terminal connected to the MTJ in a low-resistance state. Since the output of the Spin

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Switch achieves a bi-directional current, it can be used as the input to following devices, enabling a spintronic logic element with charge-based interconnects, which mitigates the interconnect length issues associated with All Spin Logic. However, the Spin Switch operates based on static charge current flow, which limits the energy-efficiency of the device.

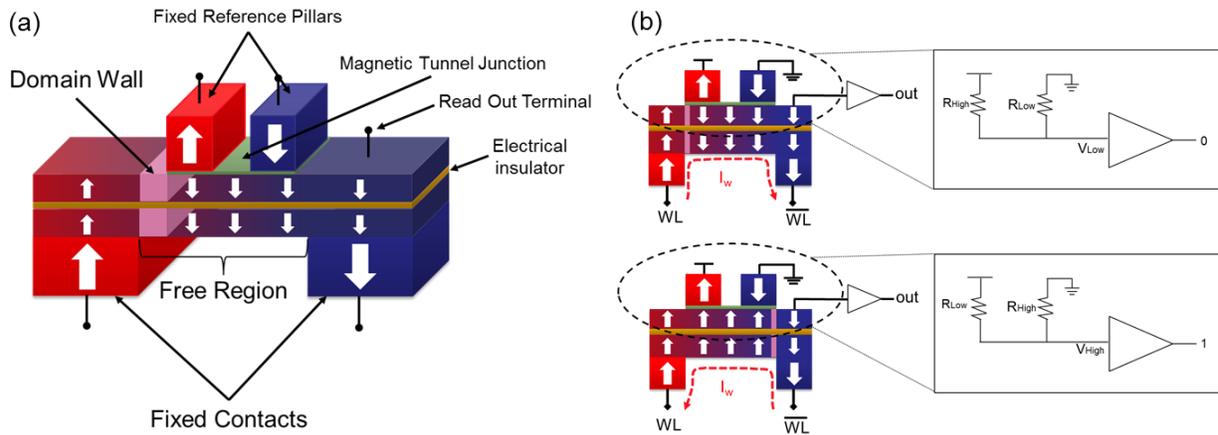Domain Wall Coupled Spin Transfer Torque Device

Figure 2 (a): Domain Wall Coupled Spin Transfer Torque Device; (b): Low and High states

The *Domain Wall Coupled Spin Transfer Torque (DWCSTT)* device shown in Figure 2a uses two electrically isolated, but magnetically coupled FM domain wall layers to isolate the read and write mechanisms of the device similar to the Spin Switch [5]. The device state is sensed through the two anti-parallel fixed reference pillars, which have MTJs with the underlying domain-wall-based free layer. The domain wall only has two stable states as shown in Figure 2b, and therefore one fixed reference pillar will always be R_{High} and the other will be R_{Low}, exclusively, and they will alternate depending upon the location of the domain wall. If the TMR of the MTJs is large enough (~100%), then we can use the two MTJs of the DWCSTT device as a voltage

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divider to output a V_{low} or a V_{high}, which can switch a CMOS inverter as shown in Figure 2b [37]. The write operation of the device is performed by passing a current through the lower domain wall FM, denoted as the write layer, which is first spin-polarized through the fixed contact layers, and then exerts a STT on the write layer, which can move the domain wall according to the LLG equation. Since the upper domain wall FM layer, denoted as the free layer, has strong dipolar coupling with the write layer, its magnetization will rotate in conjunction with the write layer as it undergoes STT. The velocity of the domain wall is linearly related to the current density applied to the write layer, and experimental results show that domain wall velocities up to 125 m/s is achievable with current densities near 1.8e8 A/cm^2 [38]. Using 16nm PTR CMOS models [39] with a supply voltage of 0.7V, respectable write speeds are achieved by simply applying logic "1" or "0" (*vdd* or *gnd*) to the device inputs. By varying the driving transistor widths, the speed and power draw of the device are able to be adjusted. Seo et al. utilized the self-referencing differential nature of the device to read the state of the device by fixing the read out terminal to ground and then comparing the currents of the two fixed reference pillars when a fixed voltage is applied to both [5]. However, with proper read and write path optimization of the DWCSTT, 16nm CMOS gates with balanced transistor widths are capable of both writing to and reading from the device in lieu of using a sense amplifier to compare relative current levels.

Magneto-Electric Spin Orbit Device

The *Magnetoelectric Spin Orbit (MESO)* device has been proposed by Manipatruni et al. as a spintronic device that combines ME switching with Inverse Spin Orbit Coupling (ISOC) state

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transduction [3]. The MESO device combines two heterostructures, one for the read unit and the other for the write unit, with a single FM shared between them. The read unit utilizes an exchange-bias mediated ME material such as Bismuth Ferrite to generate a bi-directional magnetic field based upon the electric field induced in the ME material from a voltage applied to the input terminal to switch the FM shared between the read and write unit. The write unit transduces the state of the shared FM by passing a charge current through the shared FM in order to spin polarize it and then passes that spin polarized current through an ISOC material, such as a SHE material or a TI material, which then converts the spin current into a lateral charge current at the output. Therefore, based on the state of the FM, either a positive or negative output charge current is generated. By utilizing the output charge current to switch cascaded devices by inducing a voltage on the write unit, a spintronic logic element with low energy switching can be realized. However, the static charge current required for the write unit of the MESO device limits the energy efficiency of the state-transduction mechanism for concatenation.

Domain Wall Logic Device

The *Domain Wall Logic Device (DWLD)* proposed by Chang et al. utilizes the ME and the inverse ME to both induce and detect a domain wall within a FM wire [17]. By applying a voltage to a ME material interfacially coupled to a small portion of a long FM free layer, the region nearby the ME material is switched and therefore a domain wall between the two magnetic orientations in the FM is induced. By the mechanism of domain wall automotion, the domain wall quickly propagates to the opposite side of the FM, where the output ME material is interfacially coupled

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to a small portion of the FM. The resulting magnetization change underneath the output ME material invokes the inverse ME, which changes the polarization of the ME material based on the magnetization change. This polarization change results in a buildup of positive or negative charge at the output, which can be shared with cascaded devices as inputs. Since the shared charge is much smaller than what is needed to switch a following DWLD of the same dimensions, following DWLDs must be much smaller than the preceding, and the insertion of repeaters can be used to amplify the signal once device dimensions have become too small. By using the ME as an input, the inverse ME as an output, and domain wall automotion as the interconnect and computation mechanism, a low-energy charge-current-free spintronic device is realized. However, it requires complex clocking, transistors within the logic path, and realizes gain based upon device size and the insertion of repeaters, which limits the potential benefits of the device scheme.

Summary

Table 1: Comparison of Previous Spintronic Logic Devices to CMOS and the SPLD

Logic Device	Input Signal	Output Signal	Drive Signal	State Transduction	Source of Gain
CMOS	Voltage	Voltage	Voltage	Directionality	Independent Supply
All Spin Logic [31-35]	Spin Current	Spin Current	Charge Current	Spin Polarization	Independent Supply
Spin Switch [7, 36]	Charge Current	Charge Current	Charge Current	MTJ	Independent Supply
DWCSTT [17]	Charge Current	Voltage	Charge Current	MTJ	Independent Supply
MESO [3]	Voltage	Voltage	Charge Current	ISOC	Independent Supply
DWLD [17]	Voltage	Voltage	Voltage	IME	Capacitance ratio/repeater

In this chapter several related works towards the realization of a spintronic logic device are presented and discussed. Table 1 compares a selection of spintronic logic devices with CMOS on the basis of input/output signals, drive signal, the method of state transduction, and the source of gain. CMOS logic devices such as Boolean gates propagate signals by connecting the output to V_{DD} or GND exclusively based on the input, which leads to the volatility of CMOS logic. The static-current-based switching of All Spin Logic, the Spin Switch, and the DWCSTT device prevents those schemes from low-energy operation. The voltage-controlled switching of the MESO device provides an intriguing method for low energy switching and concatenation, yet the

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static-current-based magnetic state transduction still prevents a complete low-energy device. The DWLD presents a novel scheme to use the ME with the IME to both switch, read, and perform logical operations through domain wall automotion in a low-energy package. However, the complex clocking scheme combined with the limitations of charge-sharing for concatenation are challenging for realizing a next-generation logic device.

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