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Arman Roohi

Education

2015 – Expected 2018 **PhD**, *Computer Engineering*, EECS Department, University of Central Florida, Orlando, FL.
Advisor: Dr. Ronald F. DeMara

- **Thesis Title:** Non-Volatile Logic-In-Memory Computation Using Spin-Hall-Effect-Based Datapaths.

2009 – 2011 **MSc**, *Computer Architecture*, Science and Research Branch, Islamic Azad University, Tehran, Iran.
Advisor: Dr. Keivan Navi

- **Thesis Title:** Designing a Logic Circuit With Reconfiguration Capability at Nano-scale Using QCA Technology.

2003 – 2008 **BSc**, *Computer Engineering*, Shiraz University, Shiraz, Iran.
Advisor: Dr. Fariborz Sobhanmanesh

- **Thesis Title:** Design and Implementation of Power Line Data Transmission (PLDT).

- **Coursework:** Special Topics in Emerging Computing Architectures, Neuromorphic Computing Architecture, Complex Adaptive Systems, CMOS Analog and Digital Circuits, VLSI Design, Advanced Computer Architectures, and Advanced Programming.

Research Interests

- Analog and Digital Circuits Design
- Reconfigurable and Adaptive Computer Architectures
- Emerging Nanoscale Computing Architectures
- Low Power and Reliability-Aware VLSI circuits

Research Experience

2015 - Present **Graduate Research Assistant**, "Computer Architecture Lab (CAL)", Electrical Engineering and Computer Science Department, University of Central Florida, Orlando, Florida, USA.

- Conducted Research: in Adaptive Processor Architectures for High Reliability and Improved Energy Consumption wherein a circuit-level approach and its corresponding synthesis flow has been developed to simultaneously improving lifetime-energy consumption for emerging switching devices.

2010-2013 **Research Assistant**, "Nanotechnology and Quantum Computing Laboratory (NQC Lab).", Department of Electrical and Computer Engineering, Shahid Beheshti University, Tehran, Iran.

- Conducts high quality research in various areas of Nanotechnology and Quantum Computing such as QCA and CNT.

Selected Publications

- R. Zand, **A. Roohi**, and R. F. DeMara, "Energy-Efficient and Process Variation-Resilient Write Circuit Schemes for Spin Hall Effect-MRAM," *IEEE Transactions on VLSI*, 2017.
- **A. Roohi**, R. Zand, D. Fan, and R. F. DeMara, "Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2017.
- R. Zand, **A. Roohi**, D. Fan, and R. F. DeMara, "Energy-Efficient Nonvolatile Reconfigurable Logic using Spin Hall Effect-based Lookup Tables," *IEEE Transactions on Nanotechnology*, 2017.
- M.K.Krishna, **A. Roohi**, R.Zand, and R.F. DeMara, "Heterogeneous Energy-Sparing Reconfigurable Logic:Spin-based Storage and CNFETbased Multiplexing," *IET Circuits, Devices & Systems*, 2017.

- A. M. Chabi, **A. Roohi**, H. Khademolhosseini, S. Sheikhfaal, S. Angizi, K. Navi, and R. F. DeMara, "Towards Ultra-efficient QCA Reversible Circuits," *Microprocessors and Microsystems*, 2017.
- **A. Roohi**, R. Zand, and R. F. DeMara, "A Tunable Majority Gate based Full Adder using Current-Induced Domain Wall Nanomagnets," *IEEE Transactions on Magnetics*, 2016.
- R. Zand, **A. Roohi**, S. Salehi, and R. F. DeMara, "Scalable Adaptive Spintronic Reconfigurable Logic using Area-Matched MTJ Design," *IEEE Transactions on Circuits and Systems II*, 2016.
- **A. Roohi**, R. Zand, and R. F. DeMara, "A Parity Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency," *IEEE Transactions on Emerging Topics in Computing*, 2016.
- H.Shabani, **A. Roohi**, A.Reza, M.Reshadi, N.Bagherzadeh, and R.F. DeMara, "Loss- Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks," *IEEE Transactions on Computers*, 2016. June featured paper.

before 2016

Please see my Google scholar page.

Professional Services

Editorial Board

International Journal of Advanced Computer Research (IJACR).

International Journal of VLSI Design & Communication Systems (VLSICS).

Technical Program Committees

International Conference on Semiconductor Devices, Circuits and Systems (SDCS-2014).

Second International Conference on Soft Computing, Artificial Intelligence and Applications (SCAI-2013).

International Conference On Emerging Trends, Technology and Research (ICETTR-2013).

First International Conference on Emerging Trends and Technology (ICETT-2012).

Technical Paper Reviewer

IEEE Transactions on Computer.

IEEE Transactions on VLSI Systems.

IEEE Transactions on Nanotechnology.

IEEE Transactions on Circuits and Systems II.

IEEE Transactions on Emerging Topics in Computing.

IET Computers & Digital Techniques.

Journal of Computational Electronic.

Microelectronics Journal.

Microprocessors and Microsystems .

Canadian Journal of Physics.

International Journal of Electronics Letters.

Journal of Nanoelectronics and Optoelectronics.

Ain Shams Engineering Journal.

Sub-reviewer for IEEE Computer Society Annual Symposium on VLSI (ISVLSI).

Selected Academic Projects

Ph.D.

2016-present **Spin-based ASIC design for energy-harvesting applications**.

- Develop an evolutionary Optimization approach to Synthesis of Logic-in-Memory architectures in Python.
- Develop a spin-based gate library containing the complete set of Boolean functions.

2015-2016 **Modeling the bahavior of Magnetic Tunnel Junctions (MTJs)**.

- Verilog-A model of 2-terminal and 3-terminal Magnetic Random Access Memories (MRAMs).
- Matlab model of Spin Hall Effect(SHE) assisted Spin Transfer Torque (STT) switching approach.

2014-2016 **Spin-based Circuit Design**.

- Voltage-controlled Concatenable SHE-MRAM based 1-bit Full-Adder(FA) circuit.
- Current-mode Tunable Domain Wall Nanomagnet based 1-bit Full-Adder(FA) circuit.
- 8-input Adaptive STT-MRAM based Lookup Table (LUT) circuit.
- 6-input fracturable SHE-MRAM based Lookup Table (LUT) circuit.

M.Sc.

- Implementation of digital circuits in UHF-band RFID chip (ISO 18000).
- Design and Verification of 3-stage pipelined MIPS processor using VHDL.
- Context Free Grammar Parser Project in Theory of Languages & Machines.

Talks & Presentations

2016 **Review of Spintronics and functionalities of circuit based on Spin Hall Effect MTJ**, *University of Central Florida, Orlando, USA.*

2016 **Spin-Based Neuron Model With Domain-Wall Magnets as Synapse, Tehran, Iran**, *University of Central Florida, Orlando, USA.*

2015 **Domain Wall LFSR: a Novel Spintronic Circuit for Generating Weakly-Chaotic Signatures**, *University of Central Florida, Orlando, USA.*

2015 **Dual Computational Layer Based Logic Design for QCA Circuits**, *52nd Design Automation Conference (DAC), Work-in-Progress Session, San Francisco, CA, USA, DAC-WIP 2015.*

2010 **An Analytic Model of TCP Performance Over Multi-hop Wireless Links**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Ring Generator: New Devices for Test Applications**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Performance Evaluation of Anonymous Routing Protocols in WSN**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Multi-path GEM for Routing in Wireless Sensor Networks**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Wireless Sensor Network (WSN), Structure**, *Science and Research Branch of IAU, Tehran, Iran.*

2007 **Decision Support System (DSS) & Its Structure**, *Shiraz University, Shiraz, Iran.*

2006 **Embedded System & Microcontrollers, An Introduction**, *Shiraz University, Shiraz, Iran.*

2005 **Bluetooth Devices**, *Shiraz University, Shiraz, Iran.*

Technical Skills

- **Hardware Description and behavioral Languages:** Verilog, Verilog-A.
- **Scripting Languages:** Matlab, Python.
- **Programming Languages:** C, Assembly.
- **Design and Verification Tools:** HSPICE, Synopsys Design Compiler, Cadence Virtuoso, Xilinx-ISE, Quartus, ModelSim.
- **IDE & Compilers:** NetBeans, gcc.
- **Operating Systems:** Windows, Linux.