Arman Roohi

Curriculum Vitae

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Education

2015–present **Ph.D, Computer Engineering**, *University of Central Florida* , Orlando, FL , USA.
Thesis title *"Non-Volatile Logic-In-Memory Computation Using Spin-Hall-Effect-Based Datapaths"*
Advisor Dr. Ronald F. DeMara

2009–2011 **M.Sc., Computer Architecture**, *Science and Research Branch, Islamic Azad University*, Tehran, Iran.
Thesis title *"Designing a Logic Circuit With Reconfiguration Capability at Nano-scale Using QCA Technology"*
Advisor Dr. Keivan Navi

2003–2008 **B.Sc., Computer Engineering, Hardware**, *Shiraz University*, Shiraz, Iran.
Thesis title *"Design and Implementation of Power Line Data Transmission (PLDT)"*
Advisor Dr. Fariborz Sobhanmanesh

Research Interests

- Emerging Nanoscale Electronics including Spin-based Devices
- Reconfigurable and Adaptive Computer Architectures
- Low Power and Reliability-Aware VLSI Circuits
- Digital Circuit Design Techniques

Publications

Journal Papers

2018 **A. Roohi**, and R. F. DeMara, "NV-Clustering: Normally-Off Computing Using Non-Volatile Datapaths," *IEEE Transactions on Computers*, in press, accepted 14 January 2018.

2017 R. Zand, **A. Roohi**, and R. F. DeMara, "Energy-Efficient and Process-Variation-Resilient Write Circuit Schemes for Spin Hall Effect MRAM Device," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 9, pp. 2394-2401, Sept. 2017.

2017 **A. Roohi**, R. Zand, D. Fan, and R. F. DeMara, "Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 12, pp. 2134-2138, Dec. 2017.

2017 M. K.Krishna, **A. Roohi**, R. Zand, D. Fan, and R. F. DeMara, "Heterogeneous Energy-Sparing Reconfigurable Logic:Spin-based Storage and CNFET-based Multiplexing," *IET Circuits, Devices & Systems*, vol. 11, no. 3, pp. 274-279, 5 2017.

2017 R. Zand, **A. Roohi**, D. Fan, and R. F. DeMara, "Energy-Efficient Nonvolatile Reconfigurable Logic using Spin Hall Effect-based Lookup Tables," *IEEE Transactions on Nanotechnology*, vol. 16, no. 1, pp. 32-43, Jan. 2017.

2017 A.M. Chabi, **A. Roohi**, H. Khademolhosseini, Sh. Sheikhfaal, Sh. Angizi, K. Navi, and R. F. DeMara, Towards Ultra-efficient QCA Reversible Circuits," *Microprocessors and Microsystems*, Volume 49, 2017, Pages 127-138

2016 **A. Roohi**, R. Zand, Sh. Angizi, and R. F. DeMara, "A Parity-Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency," *IEEE Transactions on Emerging Topics in Computing*, Special Issue on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, in press, accepted 18 July 2016.

2016 **A. Roohi**, R. Zand, and R. F. DeMara, "A Tunable Majority Gate based Full Adder using Current-Induced Domain Wall Nanomagnets," *IEEE Transactions on Magnetics* 52 (8).

2016 R. Zand, **A. Roohi**, S. Salehi, and R. F. DeMara, "Scalable Adaptive Spintronic Reconfigurable Logic using Area-Matched MTJ Design," *IEEE Transactions on Circuits and Systems II: Express Briefs* 63 (7), 678 - 682.

2016 H. Shabani, **A. Roohi**, A. Reza, M. Reshadi, N. Bagherzadeh, and R. F. DeMara, "Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks," *IEEE Transactions on Computers*, 65 (6), 1789-1801. **June featured paper**.

2015 **A. Roohi**, H. Thapliyal, and R. F. DeMara, "Wire Crossing Constrained QCA Circuit Design using Bilayer Logic Decomposition," *IET Electronics Letters*, Vol 51, No. 21, P. 1677.

2015 Sh. Angizi, S. Sayedsalehi, **A. Roohi**, N. Bagherzadeh, K. Navi, "Design and verification of new n-bit quantum-dot synchronous counters using majority function-based JK flip-flops," *Journal of Circuits, Systems and Computers*, Vol 24, No. 10, P. 1550153.

2015 **A. Roohi**, R. F. DeMara,and N. Khoshavi, ''Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder," *Microelectronics Journal*, Vol 46, No. 6, P. 531.

2014 **A. Roohi**, H. Khademolhosseini, S. Sayedsalehi, and K. Navi, ''A Symmetric Quantum-dot Cellular Automata Design for 5-input Majority Gate," *Journal of Computational Electronics*, Vol 13, No. 3, P. 701.

2014 **A. Roohi**, H. Khademolhosseini, ''Quantum-Dot Cellular Automata: Computing in Nanoscale," *Reviews In Theoretical Science (RITS)*, Vol 2, No. 1, P. 46.

2013 **A. Roohi**, B. Menbari, E. Shahbazi, and M. Kamrani, ''A Genetic Algorithm Based Logic Optimization for Majority Gate-Based QCA Circuits in Nanoelectronics," *Quantum Matter*, Vol.2, No.3, P. 219.

2013 H. Shabani, **A. Roohi**, A. Reza, H. Khademolhosseini, and M. Reshadi, ''Parallel-XY: a novel loss-aware non-blocking photonic router for silicon nano-photonic networks-on-chip," *Journal of Computational and Theoretical Nanoscience*, Vol.10, No.6, P. 1510.

2013 K. Navi, **A. Roohi**, and S. Sayedsalehi, ''Designing Reconfigurable Quantum-dot Cellular Automata Logic Circuits," *Journal of Computational and Theoretical Nanoscience*, Vol.10, No.5, P. 1137.

2013 **A. Roohi**, S. Sayedsalehi, H. Khademolhosseini, and K. Navi, ''Design and Evaluation of a Reconfigurable Fault Tolerant Quantum-dot Cellular Automata Gate," *Journal of Computational and Theoretical Nanoscience*, Vol.10, No.2, P. 380.

2011 S. Sayedsalehi, **A. Roohi**, and K. Navi, ‘‘A different design approach for high performance in nanostructure using Quantum Cellular Automata,” *Canadian Journal on Electrical and Electronics Engineering*, Vol.2, No.11, P. 526.

2011 **A. Roohi**, H. Khademolhosseini, S. Sayedsalehi, and K. Navi, ‘‘A Novel Architecture for Quantum-Dot Cellular Automata Multiplexer,” *International Journal of Computer Science Issues*, Vol.8, No.6, P. 55.

Conference Papers

2018 **A. Roohi**, R. Zand, and R. F. DeMara, “Logic-Encrypted Synthesis for Energy-Harvesting-Powered Spintronic-Embedded Datapath Design,” 28th ACM *Great Lakes Symposium on VLSI (GLSVLSI 2018)*, Chicago, Illinois, USA, May 23-25, 2018.

2018 **A. Roohi**, R. Zand, and R. F. DeMara, “Synthesis of Normally-Off Boolean Circuits: An Evolutionary Optimization Approach Utilizing Spintronic Devices,” The 19th *International Symposium on Quality Electronic Design*, Santa Clara, CA, USA, ISQED 2018.

2017 R. F. DeMara, **A. Roohi**, R. Zand, and S. D. Pyle, “Heterogeneous Technology Configurable Fabrics for Field Programmable Co-design of CMOS and Spin-based Devices,” in Proceedings of *IEEE International Conference on Rebooting Computing (ICRC-2017)*, Washington, DC, USA, November 8 – 9, 2017.

2017 **A. Roohi**, L. Wang, S. Kose, and R. F. DeMara, “Secure Intermittent-Robust Computation for Energy Harvesting Device Security and Outage Resilience,” The 14th *IEEE International Conference on Advanced and Trusted Computing*, San Francisco, CA, USA, ATC 2017.

2015 A.M.Chabi, **A. Roohi**, H. Khademolhosseini, Sh. Angizi, R. F. DeMara, and K. Navi, “Cost-Efficient QCA Reversible Combinational Circuits Based on a New Reversible Gate,” The 18th *CSI Symposium on Computer Architecture & Digital Systems*, Tehran, Iran, CADS 2015 (best paper nominated).

2015 R. A. Ashraf, A. Al-Zahrani, N. Khoshavi, R. Zand, S. Salehi, **A. Roohi**, M. Lin, and R. F. DeMara, “Reactive Rejuvenation of CMOS Logic Paths using Self-Activating Voltage Domains,” *IEEE International Symposium on Circuits and Systems*, Lisbon, Portugal, ISCAS 2015.

2015 **A. Roohi**, R. F. DeMara, and N. Khoshavi, “Dual Computational Layer Based Logic Design for QCA Circuits,” 52nd *Design Automation Conference (DAC)*, Work-in-Progress Session, San Francisco, CA, USA, DAC-WIP 2015.

2015 S.Sayedsalehi, and **A. Roohi**, “Modeling an Improved Modified Type in Metallic Quantum-dot Fixed Cell for Nano Structure Implementation,” 23rd *Euromicro International Conference on Parallel, Distributed and Network-based* Processing, Turku, Finland, PDP 2015.

2013 S. Sayedsalehi, **A. Roohi**, H. Khademolhosseini, and M. Kamrani, “Design of Nanoelectronic Circuits Using an Efficient Reversible Gate,” 9th *International Nanotechnology Symposium*, Dresden, Germany, Nanofair 2012.

2012 **A. Roohi**, H. Khademolhosseini, S. Sayedsalehi, and K. Navi, ‘‘Implementation of Reversible Logic Design in Nanoelectronics on Basis of Majority Gates,” The 16th *CSI Symposium on Computer Architecture & Digital Systems*, Shiraz, Iran, CADS 2012.

2011 **A. Roohi**, M. Kamrani, S. Sayedsalehi, and K. Navi, ''A Combinational Logic Optimization for Majority Gate-Based Nanoelectronic Circuits Based on GA," *International Semiconductor Device Research Symposium*, The University of Maryland, USA, ISDRS 2011.

2011 H. Khademolhosseini and **A. Roohi**, ''A New Redundant Method on Representing Numbers with Moduli Set $\{3^n, 3^n-1, 3^n-2$ " *Computer, Communication and Electrical Technology (ICCCET 2011)*, IEEE International Conference on, pp. 163-166.

Book Chapter

2012 M. Kamrani, H. Khademolhosseini, **A. Roohi**, and P. Aloustanimirmahalleh, ''A Novel Genetic Algorithm Based Method for Efficient QCA Circuit Design," *Advances in Computer Science, Engineering & Applications*. vol. 166, D. C. Wyld, et al., Eds., ed: Springer Berlin / Heidelberg, 2012, pp. 433-442.

Professional Activities

2017 **Tutor/Proctor/Coordinator**, UCF College of Engineering, Evaluation and Proficiency Center.

2017 **STEM Assessment Assistant:** Advisement of faculty at all levels (Lecturer through Professor) on digitization of engineering assessments, construction of computer-based exams, and remediation methods.

2016-present **Graduate Research Assistant**, Department of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL, USA.

2015 **Graduate Teaching Assistant**, Department of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL, USA.

2015 **Graduate Assistant**, Department of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL, USA.

2014 Member of School of Computer Science, Institute for Research in Fundamental Sciences (**IPM**), Tehran, Iran.

2011 Senior research assistant at Nanotechnology and Quantum Computing Laboratory, Shahid Beheshti University, G.C., Tehran, Iran.

Editorial Board

- International Journal of Advanced Computer Research (**IJACR**).
- International Journal of VLSI Design & Communication Systems (**VLSICS**).

Technical Program Committees

- International Conference on Semiconductor Devices, Circuits and Systems (**SDCS-2014**).
- Second International Conference on Soft Computing, Artificial Intelligence and Applications (**SCAI-2013**).
- International Conference On Emerging Trends, Technology and Research (**ICETTR-2013**).
- First International Conference on Emerging Trends and Technology (**ICETT-2012**).

Technical Paper Reviewer

- IEEE Transactions on Computers
- IEEE Transactions on VLSI Systems

- IEEE Transactions on Nanotechnology
- IEEE Transactions on Emerging Topics in Computing
- IET Computers & Digital Techniques
- Journal of Computational Electronics (Springer)
- Microelectronics Journal (Elsevier)
- Microprocessors and Microsystems (Elsevier)
- Ain Shams Engineering Journal (Elsevier)

Talks & Presentations

2016 **Review of Spintronics and functionalities of circuit based on Spin Hall Effect MTJ**, *University of Central Florida, Orlando, USA.*

2016 **Spin-Based Neuron Model With Domain-Wall Magnets as Synapse, Tehran, Iran**, *University of Central Florida, Orlando, USA.*

2015 **Domain Wall LFSR: a Novel Spintronic Circuit for Generating Weakly-Chaotic Signatures**, *University of Central Florida, Orlando, USA.*

2010 **An Analytic Model of TCP Performance Over Multi-hop Wireless Links**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Ring Generator: New Devices for Test Applications**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Performance Evaluation of Anonymous Routing Protocols in WSN**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Multi-path GEM for Routing in Wireless Sensor Networks**, *Science and Research Branch of IAU, Tehran, Iran.*

2010 **Wireless Sensor Network (WSN), Structure**, *Science and Research Branch of IAU, Tehran, Iran.*

2007 **Decision Support System (DSS) & Its Structure**, *Shiraz University, Shiraz, Iran.*

2006 **Embedded System & Microcontrollers, An Introduction**, *Shiraz University, Shiraz, Iran.*

2005 **Bluetooth Devices**, *Shiraz University, Shiraz, Iran.*

Honors

- 2018 Frank Hubbard Engineering Endowed Scholarship for the 2018- 2019 academic year. This Scholarship is offered for 7 undergraduate and graduate students from the UCF College of Engineering each year.
- Vice President of Students Laureates of STEM Teaching and Learning (SLSTL) Registered Student Organization, Summer 2017-Present.
- Treasurer of Students Laureates of STEM Teaching and Learning (SLSTL) Registered Student Organization, Summer 2016-2017.
- Co-Established Students Laureates of STEM Teaching and Learning (SLSTL) as a Registered Student Organization, Summer 2016.
- Worked closely with my advisor in order to prepare technical and educational proposals since Fall 2014.

- Received Master Degree with the Highest Honors from Department of Computer Engineering, Islamic Azad University, Science and Research Branch, Due to the Best Research Results, 2011.
- Semifinalist of the national Mathematics Olympiad, 2001.
- Semifinalist of the national Physics Olympiad, 2001.

Additional Scientific & Research Activities

- SPICE-Compatible Magnetic Tunnel Junctions Compact Model Including STT and SHE-assisted Switching Approaches.
- Invention Disclosure, UCF Office of Research and Commercialization, "A Parity-Preserving Reversible QCA Gate with Cascadable Resilience," April 15, 2015.
- Co-supervised one Master Thesis, UCF.
- Design & develop of Computer Architecture Laboratory (CAL) website.
- Iran Nanotechnology Initiative Council award for selected journal publications.
- Implementation of digital circuits in UHF-band RFID chip (ISO 18000).
- Being the member of Hardware group in CSE dep., Shiraz University.
- Signal projects (Filtering and FFT).
- Context Free Grammar Parser Project in Theory of Languages & Machines.
- MIPS Architecture project.

Technical Skills

- **Hardware Description and behavioral Languages:** Verilog, Verilog-A.
- **Scripting Languages:** Matlab, Python.
- **Programming Languages:** C, Assembly.
- **Design and Verification Tools:** HSPICE, Synopsys DC, Cadence Virtuoso, Xilinx-ISE, Quartus, ModelSim.
- **IDE & Compilers:** NetBeans, gcc.
- **Operating Systems:** Windows, Linux.

References

Dr. Ronald F. DeMara, *University of Central Florida; Professor.*
Email: ronald.demara@ucf.edu

Dr. Deliang Fan, *University of Central Florida; Assistant Professor.*
Email: dfan@ucf.edu

Dr. Nader Bagherzadeh, *University of California, Irvine; Professor.*
Email: nader@uci.edu

Taees Eimuri, *Software Developer, IBM Security.*
Email: taees.eimouri1@ibm.com