FARIS ALGHAREB

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EDUCATION

Ph.D.| Computer Engineering, ECE Department, University of Central Florida, Orlando, FL.

ADVISOR: DR. RONALD F. DEMARA

SPRING 2014 – Present

Conducted research on (Design and Evaluation of Soft-Error Resilient and Energy-Efficient Circuits and Systems for Contemporary Robust Computing) as a research assistant on full scholarship. In addition, I was the lead author of a highlighted article of 2017 in IEEE Transactions on Circuits and Systems II selected by IEEE international Symposium on Circuits & Systems (ISCAS) Program Committee for presentation as a highlighted paper at the ISCAS-2017 conference. Moreover, I have published my research work in top technical journals like IEEE transactions on Sustainable Computing, as my paper was selected to IEEE Transactions Special Issue on Low Power Dependable Computing. Maintained a 4.0/4.0 GPA throughout all the taken coursework at University of Central Florida.

M.Sc.| Computer Engineering, University of Mosul, Mosul, Iraq.

FALL 2007 – FALL 2009

Maintaining an overall average of 81.44% for coursework and research work.

Thesis Title: Design and Implementation of an Efficient Architecture Using FPGA (Spartan-3E) for Image Processing by Sliding Window.

B.Sc.| Computer Engineering, University of Mosul, Mosul, Iraq.

FALL 2003 – SUMMER 2007

Title of Senior Design Project: Design of Real Time Control System for DC Servo Motor Based on LabVIEW.

RESEARCH INTERSET

- Radiation-based Soft-error mitigation techniques for resilient circuits and systems
- Energy-efficient computing designs for reliable computer architectures
- VLSI design with particular emphasis on low-power and high-performance
- Emerging spin-based non-volatile latching circuits
- Approximate computing architectures
- Imprecise signal/image processing algorithms

EXPERIENCE

Graduate Research Assistant | **Computer Architecture Lab (CAL), Electrical and Computer Engineering Department, University of Central Florida, Orlando, Florida, USA.**

SPRING 2014 – Present

Conducted Research:

- Designs to reduce soft-error impacts on process variation in near-threshold voltage region.
- Temporal self-voting logic circuits.
- Single/double node upset mitigation strategies for flip-flops in both highly-scaled CMOS technology and spintronic magnetic tunnel junction technology memories.

Assistant Lecturer | Computer and Informatics Engineering Department, University of Mosul, Mosul, Iraq.

APRIL 2011 – DECEMBER 2012

Developed new laboratory for FPGAs design and implementation. Teaching classes and labs in Computer and Informatics Engineering Department, including the following subjects:

- Digital Logic Design (3 hours lab weekly)
- Computer Organization and Design (3 hours lecture weekly)
- FPGA Design and Programming (4 hours lecture and lab weekly)
- Digital Signal Processing (DSP) Applications and Analysis (4 hours lab weekly)
- Principles of Math (2 hours lecture weekly)

Assistant Lecturer | Dijlah University Collage, Erbil, Iraq.

SEPTEMBER 2010 – APRIL 2011

Received outstanding teaching evaluations and ranking. Teaching classes and labs in Computer Science Department, including the following subjects:

- Digital Systems Fundamentals (3 hours lecture weekly)
- Principles of Math (6 hours lecture weekly)

SKILLS

- Hardware Description and behavioral Languages: Verilog, VHDL.
- Design and Verification Tools: HSPICE, Synopsys Design Compiler, Cadence Virtuoso, Xilinx-ISE, ModelSim.
- Modeling and Simulation: MATLAB, LabVIEW.
- Programming Languages: C, Assembly.
- Document Production: LATEX, Microsoft Office

PUBLICATIONS

- Faris S. Alghareb, R. A. Ashraf, and Ronald F. DeMara, "Designing and Evaluating Redundancy-based Soft Error Masking on a Continuum of Energy and Robustness," Accepted to *IEEE Transactions on Sustainable Computing Special Issue on Low-Power Dependable Computing*, Sep 2017.
- Faris S. Alghareb, R. A. Ashraf, A. Al-Zahrani, and R. F. DeMara, "Energy and Delay Tradeoffs of Soft-Error Masking for 16-nm FinFET Logic Paths: Survey and Impact of Process Variation

in the Near-threshold Region," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no.6, pp.695-699, June 2017.

- Faris S. Alghareb, Mingjie Lin, and R. F. DeMara, "Soft Error Effect Tolerant Temporal Self-Voting Checkers: Energy vs. Resilience Tradeoffs," in *Proceedings of the International Symposium on VLSI (ISVLSI-2016)*, Pittsburgh, Pennsylvania, U.S.A., July 11-13, 2016.
- Faris S. Alghareb, Ramtin Zand, and R. F. DeMara, "Energy-Efficient and Soft-Error Resilient Non-Volatile Spintronic Flip-Flop Designs," Submitted to *IEEE Transactions on Circuit and Systems I*, Feb. 2018.

PROFESSIONAL SERVICE

- Reviewer for IEEE Transactions on Circuits and Systems II: Express Briefs, 2016.
- Sub-reviewer for IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2016).
- Sub-Reviewer for IEEE Symposium Series on Computational Intelligence (SSCI-2016).
- Manuscript Reviewer for IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2017).

SELECTED GRADUATE COURSEWORK

I completed the coursework listed below to improve my theoretical research background and become more familiar with many practical aspects of CMOS-based full-custom VLSI design ranging from numerous technology libraries to Predictive Technology Models (PTMs) via simulation. These studies extended my previous knowledge of FPGA devices from Xilinx device family up through partial runtime reconfiguration. Thus, my expertise extends beyond how the logic gates are functioning, down to the details of how the cell libraries are designed, various schematic and layout design methods and tools, and how synthesizable Verilog code can be implemented and converted to a layout design via the designed library using Cadence and Synopsys Design Compiler. Together these equip me with a deep understand of how large designs are constructed, validated, and optimized. Finally, I applied all of these skills together to advance contemporary computing techniques such as soft-error resilient circuits and systems, low power designs, and parallel architectures.

- CDA 5106 - Advanced Computer Architecture (Grade A)
- EEE 5390 - Full-Custom VLSI Design (Grade: A)
- EEL 5820 - Image Processing (Grade: A)
- EEE 5378 - CMOS Analog and Digital Circuit design (Grade: A)
- EEL 5722C - FPGA Design (Grade: A)
- ECM 6308 - Current Topics in Parallel Processing (Grade: A)

SELECTED PROJECTS

Doctoral:

- Present, Spin-based Latching Circuit Design: Developed a spin-based soft-error resilient (for both SEU and DNU) and energy-efficient Non-Volatile Flip-Flop (NVFF) Designs. (Advisor: Prof. Ronald F. DeMara)
- 2017, Energy versus Robustness: identified of redundancy-based hardening techniques that can deliver increased benefits in terms of the Fault Coverage Energy Ratio (FCER) for the leveraged tradeoffs within iso-energy constraints at Near-Threshold Voltage (NTV). (Advisor: Prof. Ronald F. DeMara)

- **2016, Reliability of Soft-Error Resilient Designs**: Investigated the Impact of Process Variation (PV) at NTV on redundancy-based soft error mitigation techniques. (Advisor: Prof. Ronald F. DeMara)
- **2015, Soft-Error Tolerant Circuit Design**: Employed Self-Voting with spatial and temporal redundancy to develop resilient circuits that tolerate single and double error. (Advisor: Prof. Ronald F. DeMara)
- **Spring 2014**, **Full Custom VLSI Design,** Design and implementation an 8x16-bit Reconfigurable Linear Feedback Shift Register (RLFSR) of Galios structure using Cadence Virtuoso. (Supervisor: Prof. Yier Jin)
- **Spring 2014, Image Processing,** Seam Carving for Content-Aware Image Resizing (Supervisor: Prof. Hassan Foroosh)
- **Fall 2014, Field-Programmable Gate Array (FPGA) Design,** Design and Simulate the JPEG Huffman Decoder with Verilog HDL (Supervisor: Prof. Mingjie Lin)

M.Sc.

- Spring 2008, **Parallel Architecture,** FPGA Implementation: High Speed Parallel Architecture for Image Processing Rank Order Filter.
- Fall 2008, **Parallel Architecture,** Design and Implementation the Systolic Architecture of 2-D Convolution for Real Time Edge Detection.

PROFESSIONAL ACTIVITIES

Presentation/Participation in Conferences:

- International Symposium on VLSI (ISVLSI-2016), Pittsburgh, Pennsylvania, U.S.A., July 11-13, 2016.
- IEEE International Symposium on Circuits and Systems (ISCAS-2017), Baltimore, Maryland, USA, May 28-31, 2017. My paper was selected by ISCAS Program Committee for Lecture Presentation as an IEEE Transactions on Circuits and Systems highlighted article of 2017.

Certifications:

- Completed GPD 501: Online Graduate Grantsmanship - Fall 2017