# Faris S. Alghareb

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## Education

- **University of Central Florida** Orlando, FL
  **P.hD.** Computer Engineering, Spring 2014-now
  **Advisor:** Prof. Ronald F. DeMara **GPA:** 4/4

- **Mosul University (Engineering collage)** Mosul, Iraq
  **M.Sc.** Computer Architecture, 2007-2009
  **Thesis:** Design and Implementation of an Efficient Architecture **Average:** 81.44%
  Using FPGA (Spartan-3E) for Image Processing by Sliding Window.
  **Advisor:** Prof. Shefa A. Dawwd

  **B.Sc.** Computer Architecture 2003-2007
  Ranked 6th among B.Sc. students of Computer Engineering. **Average:** 75.63%

## Research Interest

- Energy efficient and high performance circuit technologies
- VLSI Design with particular emphasis on low-power, high-performance
- Reliable Computer Architectures
- Approximate Computing Architectures
- Imprecise Signal Processing/Image Processing Algorithms

## Work Experiences

- Assistant Lecturer, Dijlah University Collage (Sep. 2010- March 2011)
  - Digital Logic Design
  - Principles of Math
- Assistant Lecturer, Mosul University (April 2011- Dec. 2012)
  - Digital Logic Design
  - Computer Architecture
  - FPGA Design and Programming
  - Signals and Systems

## Selected Graduate Coursework

- Advanced Computer Architecture (CDA 5106 )
- Full-Custom VLSI Design (EEE5390)
- Image Processing (EEL 5820)
- CMOS Analog and Digital Circuit design (EEE 5378)
- FPGA Design (EEL 5722C)
- Current Topics in Parallel Processing (ECM 6308)

## Selected Projects

- Spring 2014, Full Custom VLSI Design, Design and implementation a 8x16-bit Reconfigurable Linear Feedback Shift Register (RLFSR) of Galios structure using Cadence Virtuoso (Advisor: Prof. Yier Jin)
- Spring 2014, Image Processing, Seam Carving for Content-Aware Image Resizing (Advisor: Prof. Hassan Foroosh)
- Fall 2014, Field-Programmable Gate Array (FPGA) Design, Design and Simulate the JPEG Huffman Decoder with Verilog HDL (Advisor: Prof. Mingjie Lin)
- Spring 2008, Parallel Architecture, FPGA Implementation: High Speed Parallel Architecture for Image Processing Rank Order Filter.

## Research Publications

### Journals

F. S. Alghareb, R. A. Ashraf, A. Al-Zahrani, and R. F. DeMara, "Energy and Delay Tradeoffs of Soft Error Masking for 16nm FinFET Logic Paths: technique survey and process variation impact in near threshold region," submitted to the *IEEE Transactions on Circuits and Systems II: Express Briefs, May 2015.*

## Technical Skills

- Tools and Systems
  - EDA: Xilinx tools (ISE), Cadence Virtuoso, Synopsys Design Compiler
  - Modeling and Simulation: HSPICE, MATLAB, LabVIEW, Multisim
- Processor Hardcores and Fabrics
  - Xilinx Spartan-3E, Virtex II Pro, Virtex 4 FPGAs, Intel x86
- Programming Languages
  - Hardware: Verilog HDL, VHDL
  - Software: C/C++, Visual Basic, OpenGL, Assembly Language (80x86, MIPS)
- Document Production
  - LATEX, Microsoft Office