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Ramtin Zand

Technical Interests

- Machine Learning and Neuromorphic Computing Systems
- Emerging Nanoscale Electronics including Spin-based Devices
- Reconfigurable and Adaptive Computer Architectures
- Low Power and Reliability-Aware VLSI Circuits

Education

2014 – Present **Ph.D.**, *Computer Engineering*, ECE Department, University of Central Florida, Orlando, FL. Advisor: Dr. Ronald F. DeMara

- **GPA:** 4.0
- **Dissertation Title:** Heterogeneous Reconfigurable Fabrics for In-Circuit Training and Evaluation of Neuromorphic Architectures.

2010 – 2012 **M.Sc.**, *Electrical Engineering*, Sharif University of Technology, Iran.

- **Thesis Title:** FPGA Implementation of a Robust Fuzzy Logic Controller for a Quadruped Robot using Human Knowledge of Walking.

2005 – 2010 **B.Sc.**, *Electrical Engineering*, Imam Khomeini International University (IKIU), Iran.

- **Thesis Title:** Optimization of the Short-Term Electricity Price Forecasting Using Neural Networks and Evolutionary Algorithms.

Research Experience

2017 - Present **NSF/SRC Senior Graduate Research Assistant**, "Computer Architecture Lab (CAL)", ECE Department, UCF, Orlando, Florida, USA.

- Research in neuromorphic computing architectures for low-energy post-Moore processing approaches using beyond-CMOS devices.
- Model- , circuit- , and tool-level innovation for probabilistic spin logic devices with lowered energy barriers of commercial MTJs and other emerging devices.
- Power, delay, and area benchmarking and optimization for classification and recognition applications including impacts of noise and process variation.
- Mentoring 2 first-year Ph.D. students.
- Mentoring 2 REU students on an NSF-funded project.
- Co-Mentoring 1 M.S. student.

2016 - 2017 **Research Group Leader (During Prof. DeMara's Sabbatical)**, "Computer Architecture Lab (CAL)", ECE Department, UCF, Orlando, Florida, USA.

- Leading the creation of preliminary results and assisting end-to-end logistics of NSF and SRC proposals and various white paper submissions.
- Managing weekly meetings.

- Task-level mentoring of graduate and undergraduate students.
- Coordinating group publications.

2014 - Present **Graduate Assistant**, "Computer Architecture Lab (CAL)", Electrical Engineering and Computer Science Department, UCF, Orlando, Florida, USA.

- Conducted Research: Realizing the cooperating strength of charge-based and spin-based devices to design a reconfigurable spintronic fabric.

2010-2012 **Graduate Research Assistant**, "Artificial Creatures Lab.", Electrical Engineering Department, Sharif University of Technology, Tehran, Iran.

- Conducted Research: Extracting the human knowledge of walking and utilizing it to design a robust controller for a quadruped robot using fuzzy logic.

Teaching Experience

2015 - 2018 **Computer Organization and Design Course**, *Lab Instructor*, UCF.

- Teaching weekly labs to ∼70 students per semester.
- Preparing a 14-Week Lab Manual for the required laboratory components.
- Designing Projects and Lab Assessments using Mars Assembler and Xilinx ISE Design Suite with C, Verilog, and MIPS Assembly programming Languages.
- Received outstanding student feedback regarding lab instruction (available upon request).

2015 - 2018 **Computer Organization and Design Course**, *Teaching Assistant*, UCF.

- Working with two faculty members to develop syllabus and course contents including projects, assignments, and exams in an electronically-delivered format for $\sim$ 140 students per semester.
- Designing the course webpage and online evaluation instruments.

Summer 2017 **STEM Assessment Assistant**, Advisement of faculty at all levels (Lecturer through Professor) on digitization of engineering assessments, construction of computer-based exams, and remediation methods.

2011 - 2012 **Artificial Neural Networks**, *Teaching Assistant*, Sharif University of Technology.

- Designing Projects and Assignments.
- Grading Quizzes and Exams.

2011 - 2012 **Fuzzy Systems**, *Teaching Assistant*, Sharif University of Technology.

- Designing Projects and Assignments.
- Grading Quizzes and Exams.

2011 - 2013 **Electronics I and II, Digital Logic Circuits, Electrical Networks, Computer Architecture, Signals and Systems**, *Instructor*, Semi-Private Classes.

- Teaching more than 50 undergraduate students in semi-private classes.
- Preparing students for the Iranian Graduate School Entrance Exam.

Industry Experience

2011-2013 **Senior Hardware Designer**, "Mechatronic Research Laboratory (MRL)", Qazvin Azad University, Qazvin, Iran.

- Parax hybrid vehicle: FPGA Implementation of an Engine Control Unit (ECU).

- Small size soccer robot: FPGA Implementation of a control and activity log system.
- Humanoid soccer robot: FPGA Implementation of a real time object tracking system.

2008-2013 **R&D Engineer**, Noafarin-Sepehr Research and Manufacturing Company, Karaj, Iran.

- Responsibilities: Provide design documentation and technical support for clinical laboratory robotic systems including Tissue Processors, Slide Stainers, and Biochemistry Analyzers.

Selected Academic Projects

2017-Present **Machine Learning and Neuromorphic Computing Systems**.

- Development of a Probabilistic Inference Network Simulator (PIN-Sim) in Python, which provides a circuit-level implementation of Deep Neural Networks (DNNs) in SPICE with spintonic-based stochastic neurons libraries and Memristive crossbars.
- FPGA Design and Implementation of a Finite State Machine (FSM) for in-circuit training and evaluation of Deep Belief Networks (DBNs).
- Development of a Genetic Algorithms (GAs)-based design space exploration strategy to optimize DNN topologies for MNIST and CIFAR-10 pattern recognition applications.

2014-Present **Hybrid Spintronic/CMOS Circuit Design**.

- Development of radiation-hardened non-volatile spintronic-based Flip-Flop circuit for energy-harvesting applications.
- Development of a Transmission-Gate based Magnetic Random Access Memory (MRAM) bit-cell, including performance optimization through transistor sizing, Monte-Carlo simulation for process variation analysis, and layout design.
- Designing adaptive and fracturable STT-MRAM and SHE-MRAM based Lookup Table (LUT) circuits as building blocks for reconfigurable spintronic fabrics.
- Development of spin-based Full-Adder(FA) circuits for logic-in-memory application, including timing analysis, and clocking/signaling circuitry.

2010-2016 **VLSI and FPGA design**.

- Design/Verification of USB 2.0 Protocol Layer using Verilog HDL.
- Design/Verification of 5-stage pipelined MIPS processor, including scoreboarding and dynamic branch prediction.
- Design/Verification of a floating Point arithmetic unit including single and double precision add/subtract, multiplication, and devision operations using Verilog HDL.
- FPGA implementation of Wild Leitz measurement principle for a laser rangefinder using.

2015-2016 **Device Modeling**.

- Verilog-A model of 2-terminal and 3-terminal Magnetic Tunnel Junction (MTJ) devices.
- Matlab model of Spin Hall Effect (SHE) assisted Spin Transfer Torque (STT) switching method for MTJ devices.

2016 **Microelectronic Fabrication**.

- Fabrication of 200μm MOS transistor using photolithography and single diffusion process.
- Fabrication of BJT transistors and diodes using photolithography and double diffusion process.

Publications

Book Chapter.

[B1] **R. Zand**, A. Roohi, and R. F. DeMara, "Fundamentals, Modeling and Application of Magnetic Tunnel Junctions", *Nanoscale Devices: Physics, Modeling, and Their Application*, CRC Press, 1^{st} edition, pp. 357-388, 16 November 2018. https://www.taylorfrancis.com/books/9781351670227.

Journal Publications.

[J13] **R. Zand**, K. Y. Camsari, S. Datta, and R. F. DeMara, "Composable Probabilistic Inference Networks Using MRAM-based Stochastic Neurons," minor revision pending to *ACM Journal on Emerging Technologies in Computing Systems*, 31 October 2018. **(Selected to Special Issue on Hardware and Algorithms for Energy-Constrained On-chip Machine Learning)**

[J12] F. S. Alghareb, **R. Zand**, and R. F. DeMara, "Non-Volatile Spintronic Flip-Flop Design for Energy-Efficient SEU and DNU Resilience," accepted for publication in *IEEE Transactions on Magnetics*, 9 Nov 2018.

[J11] S. Salehi, **R. Zand**, and R. F. DeMara, "Clockless Spin-based Look-Up Tables with Wide Read Margin," submitted to *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2 Nov 2018.

[J10] S. Salehi, N. Khoshavi, **R. Zand**, and R. F. DeMara, "Self-Organized Sub-bank SHE-MRAM-based LLC: an Energy-Ecient and Variation-Immune Read and Write Architecture," *Integration the VLSI journal*, 2018. doi: 10.1016/j.vlsi.2018.03.001.

[J9] **R. Zand**, and R. F. DeMara, "Radiation-hardened MRAM-based LUT for non-volatile FPGA soft error mitigation with multi-node upset tolerance," *Journal of Physics D: Applied Physics*, vol. 50, no. 50, 2017. url: http://stacks.iop.org/0022-3727/50/i=50/a=505002

[J8] **R. Zand**, A. Roohi and R. F. DeMara, "Energy-Efficient and Process-Variation-Resilient Write Circuit Schemes for Spin Hall Effect MRAM Device," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 9, pp. 2394-2401, Sept. 2017. doi: 10.1109/TVLSI.2017.2699579

[J7] **R. Zand**, A. Roohi, D. Fan and R. F. DeMara, "Energy-Efficient Nonvolatile Reconfigurable Logic Using Spin Hall Effect-Based Lookup Tables," in *IEEE Transactions on Nanotechnology*, vol. 16, no. 1, pp. 32-43, Jan. 2017. doi:10.1109/TNANO.2016.2625749

[J6] R. S. Oreifej, R. Al-Haddad, **R. Zand**, R. A. Ashraf, and R. F. DeMara, "Survivability Modeling and Resource Planning for Self-Repairing Reconfigurable Device Fabrics," in *IEEE Transactions on Cybernetics*, vol. 48, no. 2, pp. 780-792. doi:10.1109/TCYB.2017.2655878

[J5] A. Roohi, **R. Zand**, D. Fan, and R. F. DeMara, "Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 12, pp. 2134-2138. doi: 10.1109/TCAD.2017.2661800

[J4] M. Krishna Gopi Krishna, A. Roohi, **R. Zand**, and R. F. DeMara, "Heterogeneous energy-sparing reconfigurable logic: spin-based storage and CNFET-based multiplexing," in *IET Circuits, Devices and Systems*, vol. 11, no. 3, pp. 274-279, 5 2017. doi: 10.1049/iet-cds.2016.0216

[J3] **R. Zand**, A. Roohi, S. Salehi and R. F. DeMara, "Scalable Adaptive Spintronic Reconfigurable Logic Using Area-Matched MTJ Design," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 7, pp. 678-682, July 2016. doi: 10.1109/TCSII.2016.2532099

[J2] A. Roohi, **R. Zand**, and R. F. DeMara, "A Tunable Majority Gate-Based Full Adder Using Current-Induced Domain Wall Nanomagnets," in *IEEE Transactions on Magnetics*, vol. 52, no. 8, pp. 1-7, Aug. 2016. doi: 10.1109/TMAG.2016.2540600

[J1] A. Roohi, **R. Zand**, S. Angizi and R. F. DeMara, "A Parity-Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency," in *IEEE Transactions on Emerging Topics in Computing*, vol. PP, no. 99, pp. 1-1. doi: 10.1109/TETC.2016.2593634

Technical Conference Publications.

[C11] **R. Zand**, and R. F. DeMara, "SNRA: A Spintronic Neuromorphic Reconfigurable Array for In-Circuit Training and Evaluation of Deep Belief Networks," in *2018 IEEE International Conference on Rebooting Computing (ICRC)*, Tyson, VA, 2018.

[C10] **R. Zand**, K. Y. Camsari, I. Ahmed, S.D. Pyle, C. H. Kim, S. Datta, and R. F. DeMara, "Low-Energy Deep Belief Networks using Intrinsic Sigmoidal Spintronic-based Probabilistic Neurons," in *2018 ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Chicago, IL, 2018. **(Best Paper of track and Best Paper Runner-up of conference; 2nd place technical paper recognition.)**

[C9] **R. Zand**, H. Li, and R. F. DeMara, "MRAM-Enhanced Low Power Reconfigurable Fabric with Multi-Level Variation Tolerance," submitted to *56th Design Automation Conference (DAC 2019)*, Las Vegas, NV.

[C8] **R. Zand**, and R. F. DeMara, "HSC-FPGA: A Hybrid Spin/Charge FPGA Leveraging the Cooperating Strengths of CMOS and MTJ Devices," accepted for poster presentation in *27th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2019)*, Seaside, CA, 15 November 2018.

[C7] A. Roohi, **R. Zand**, and R. F. DeMara, "Logic-Encrypted Synthesis for Energy-Harvesting-Powered Spintronic-Embedded Datapath Design," *2018 ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Chicago, IL, 2018.

[C6] A. Roohi, **R. Zand**, and R. F. DeMara, "Synthesis of Normally-O Boolean Circuits: An Evolutionary Optimization Approach Utilizing Spintronic Devices," *2018 19th International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, 2018.

[C5] F. S. Alghareb, **R. Zand**, and R. F. DeMara, "High-Performance Double Node Upset-Tolerant Non-Volatile Flip-Flop Design," *IEEE SoutheastCon 2018*, Tampa Bay, FL, 2018.

[C4] R. F. DeMara, A. Roohi, **R. Zand**, and S. D. Pyle, "Heterogeneous Technology Configurable Fabrics for Field-Programmable Co-Design of CMOS and Spin-Based Devices," *2017 IEEE International Conference on Rebooting Computing (ICRC)*, Washington, DC, 2017.

[C3] R. Al-Haddad, R. S. Oreifej, **R. Zand**, A. Ejnioui and R. F. DeMara, "Adaptive Mitigation of Radiation-Induced Errors and TDDB in Reconfigurable Logic Fabrics," *2015 IEEE 24th North Atlantic Test Workshop*, Johnson City, NY, 2015.

[C2] R. A. Ashraf, A. Al-Zahrani, N. Khoshavi, **R. Zand**, S. Salehi, A. Roohi, M. Lin, and R. F. DeMara, "Reactive rejuvenation of CMOS logic paths using self-activating voltage domains," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015.

[C1] **R. Zand** and S. B. Shouraki, "Designing a fuzzy logic controller for a quadruped robot using human expertise extraction," *2013 21st Iranian Conference on Electrical Engineering (ICEE)*, Mashhad, 2013.

STEM Educational Publications.

[STEM2] S. Salehi, **R. Zand**, and R. F. DeMara, "Hierarchical Approach to Integrating Research into Undergraduate Core Courses: Graduate Assistant Focus Topics in Learner Capstone Paper Panels," Accepted for presentation in *the 2019 American Society for Engineering Education annual conference & exposition*, 3 November 2018.

[STEM1] R. F. DeMara, R. Hartshorne, B. Chen, and **R. Zand**, "Digitizing and Remediating Engineering Assessments: An Immersive and Transportable Faculty Development Workshop," *Proceedings of the American Society for Engineering Education annual conference & exposition*, June 28, 2017.

Selected Proposals and White Papers

Spring 2017 **NSF-SRC Energy-Efficient Computing: from Devices to Architectures (E2CDA) Collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Probabilistic Spin Logic for Low-Energy Boolean and Non-Boolean Computing" **(Award #1739635 for total amount of $3,680,631 to Purdue University's PI of which my UCF Doctoral Advisor directs $308K as Co-PI over a period of 3 years)**.

Fall 2017 **NSF Software and Hardware Foundations (SHF-small) collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Elastic Intermittent Computation for Energy-Harvesting-Powered Devices using Selectively Non-Volatile Datapaths".

Fall 2016 **NSF Software and Hardware Foundations (SHF-medium) collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Ultra-Low Energy Computing using Magnetoelectric-based Concatenable Switching Elements".

Spring 2016 **Air Force Research Laboratory (AFRL) White Paper**, Leading the student contributions to prepare the white paper titled "Pinpoint Vertical Integration of Spintronic Devices for Runtime Adaptive Resiliency".

Spring 2015 **Semiconductor Research Corporation (SRC) Proposal**, Leading the student contributions to prepare the proposal titled "U-shaped Magnetic Tunnel Junction Memory Cell".

Honors, Awards, and Recognitions

2018 **Best Paper Award Recognition**, *Runner-Up of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, for the paper titled "Low-Energy Deep Belief Networks using Intrinsic Sigmoidal Spintronic-based Probabilistic Neurons".

2018-2019 **Alireza Seyedi Doctoral Research Innovation Endowed Scholarship**.

2018-2019 **Daniel D Hammond Graduate Scholarship**.

2017-2018 **UCF College of Graduate Studies Conference Presentation Fellowship**.

2017-2018 **UCF Student Government Association Conference Presentation Fellowship**.

2018 **Microelectronics Journal**, Outstanding Reviewer Recognition.

2016-2017 **UCF Student Government Association Registered Student Organization Conference Participation Fellowship**.

2017 **Integration, the VLSI Journal**, Outstanding Reviewer Recognition.

2016 **Ph.D. Forum at Design Automation Conference (DAC) Travel Award**.

2013 **Robocup World Championship**, 3rd place in Small Size League as a member of MRL team.

2013 **Iran Open Robocup Competitions**, 1st place in Humanoid Robot League.

2013 **Iran Open Robocup Competitions**, 2nd place in Small Size Robot League.

2011 **Iranian Machine Design Competitions**, 1st place with Parax hybrid vehicle.

2010-2012 **Iranian Ministry of Science, Research and Technology scholarship for M.Sc. degree**.

2010 **Nationwide Iranian Graduate School Entrance Exam**, Ranked 96th among more than 28000 participants in the field of Electrical Engineering.

2005-2010 **Iranian Ministry of Science, Research and Technology scholarship for B.Sc. degree.**.

2005 **Nationwide Iranian Undergraduate School Entrance Exam**, Ranked among top 0.1% of approximately 300,000 participants in the field of Mathematics and Physics.

Professional Services and Activities

IEEE Transactions on Computer, Reviewer.

IEEE Transactions on VLSI, Reviewer.

IEEE Transactions on Circuits and Systems I, Reviewer.

IEEE Transactions on Circuits and Systems II, Reviewer.

IEEE Transactions on Emerging Topics in Computing, Reviewer.

Elsevier Integration, the VLSI Journal, Reviewer.

Elsevier Microelectronics Journal, Reviewer.

IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Sub-Reviewer.

Fall 2014 **2014 IEEE International Symposium Series on Computational Intelligence (SSCI)**, Volunteer work for providing information and assistance to conference attendees.

Invited Talks, Panels, and Presentations

2018 **NSF/SRC Computing Advances by Probabilistic Spin Logic (CAPSL) Center**, *Poster Presentation*, title: Low-Energy Deep Belief Networks using Intrinsic Sigmoidal Spintronic-based Probabilistic Neurons.

2016, 2017, 2018 **Stem Graduate Scholar Assistant Roles of the Future**, *Panelist*, University of Central Florida, Orlando, FL, USA.

2016 **Ph.D. Forum at Design Automation Conference (DAC)**, *Poster Presentation*, title: Scalable Spintronic Reconfigurable Logic for Next Generation Reconfigurable Computing.

2016 **Invited talk at UCF Graduate Student Symposium**, Title: Scalable Spintronic Reconfigurable Logic for Next Generation Reconfigurable Computing.

Patent Activity

2016 **United States Patent #9,395,285**, Tissue Processing and Slide Staining Apparatus with Robotic Arm Having Three Degrees of Freedom, contribution as a member of the R&D section in *Noafarinsepehr* Company.

Technical Skills

- **Hardware Description and behavioral Languages:** Verilog, Verilog-A.
- **Scripting Languages:** Matlab, Python.
- **Programming Languages:** C, Assembly.
- **Design and Verification Tools:** HSPICE, Synopsys Design Compiler, Cadence Virtuoso, Xilinx-ISE, Quartus, ModelSim.
- **Parallel Programming:** MPI, Pthread, CUDA.

Coursework

- **Ph.D. Degree:** Special Topics in Emerging Computing Architectures, Neuromorphic Computing Architecture, Current Topics in Parallel Processing, Complex Adaptive Systems, Fabrication of Solid-State Devices, and CMOS Analog/Digital Circuits.
- **M.Sc. Degree:** Neural Networks, Fuzzy Systems, VLSI Design, Advanced Microprocessors, Advanced Computer Architectures, Digital Signal Processors, and Advanced Programming.

References

Dr. Ronald F. DeMara (Advisor), *Professor*, University of Central Florida.

- e-mail: ronald.demara@ucf.edu
- Office Phone: (407) 823-5916
- Research Webpage: http://www.cal.ucf.edu/

Dr. Supriyo Datta, *Thomas Duncan Distinguished Professor of Electrical and Computer Engineering*, Purdue University.

- e-mail: datta@purdue.edu
- Office Phone: (765) 494-3511
- Research Webpage: https://nanohub.org/groups/supriyodatta

Dr. Chris Kim, *Professor*, University of Minnesota.

- e-mail: chriskim@umn.edu
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- Research Webpage: http://chriskim.umn.edu/

Dr. Annie S. Wu, *Associate Professor*, University of Central Florida.

- e-mail: aswu@cs.ucf.edu
- Office Phone: (407) 823-5922
- Research Webpage: http://www.cs.ucf.edu/ ecl/index.html

Dr. Behtash Behin-aein, *Senior Member of Technical Staff, STT-MRAM Data Analytics and Predictive Models*, GlobalFounderies.

- e-mail: behtash.behin-aein@globalfoundries.com