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Ramtin Zand

Education

2014 – Present **PhD**, *Computer Engineering*, EECS Department, University of Central Florida, Orlando, FL.
Advisor: Dr. Ronald F. DeMara

- **Thesis Title:** Pinpoint Vertical Integration of Spintronic Devices for Reconfigurable Resiliency.
- **Coursework:** Fabrication of Solid-State Devices, Special Topics in Emerging Computing Architectures, Neuromorphic Computing Architecture, Advanced Topics in Microelectronics, Current Topics in Parallel Processing, Complex Adaptive Systems, and CMOS Analog and Digital Circuits.

2010 – 2012 **MSc**, *Digital Electronics Engineering*, EE Department, Sharif University of Technology, Iran.

- **Thesis Title:** FPGA Implementation of a Robust Fuzzy Logic Controller for a Quadruped Robot using Human Knowledge of Walking.
- **Coursework:** VLSI Design, Advanced Microprocessors,Advanced Computer Architectures, Digital Signal Processors, Digital Signal Processing, and Advanced Programming.

2005 – 2010 **BSc**, *Electrical Engineering*, College of Engineering, Imam Khomeini International University, Iran.

- **Thesis Title:** Optimization of the Short-Term Electricity Price Forecasting Using Neural Networks and Evolutionary Algorithms.
- **Coursework:** Circuits and Electronics, Digital Integrated Circuits, Electromagnetics,Signals and Systems, and Communication Circuits.

Research Interests

- Emerging Nanoscale Computing Architectures
- Spintronic Reconfigurable Fabrics
- Energy and Reliability-Aware VLSI circuits
- Heterogeneous Technology Fabrics
- Beyond-CMOS Technologies

Research Experience

2014 - Present **Graduate Research Assistant**, "Computer Architecture Lab (CAL)", Electrical Engineering and Computer Science Department, University of Central Florida, Orlando, Florida, USA.

- Conducted Research: Realizing the cooperating strength of charge-based and spin-based devices to design a heterogeneous technology reconfigurable fabric.

2010-2012 **Graduate Research Assistant**, "Artificial Creatures Lab.", Electrical Engineering Department, Sharif University of Technology, Tehran, Iran.

- Conducted Research: Extracting the human knowledge of walking and utilizing it to design a robust controller for a quadruped robot using fuzzy logic.

Work Experience

2011-2013 **Senior Hardware Designer**, "Mechatronic Research Laboratory (MRL)", Qazvin Azad University, Qazvin, Iran.

- Parax hybrid vehicle: Design, verification, and implementation of an Engine Control Unit (ECU) on Cyclone II FPGA.
- Small size soccer robot: Design, verification, and implementation of a control and activity log system on Cyclone II FPGA.
- Humanoid soccer robot: Design, verification, and implementation of a real time object tracking system.

2007-2012 **R&D Engineer**, Noafarin-Sepehr Research and Manufacturing Company, Karaj, Iran.

- Responsibilities: Providing technical support for clinical and diagnostics laboratory robotic systems including Tissue Processors, Slide Stainers, and Biochemistry Analyzers.

Publications

- **R. Zand**, A. Roohi, and R. F. DeMara, "Energy-Efficient and Process Variation-Resilient Write Circuit Schemes for Spin Hall Effect-MRAM," *IEEE Transactions on VLSI*, 2017.
- **R. Zand**, A. Roohi, D. Fan, and R. F. DeMara, "Energy-Efficient Nonvolatile Reconfigurable Logic using Spin Hall Effect-based Lookup Tables," *IEEE Transactions on Nanotechnology*, 2017.
- R. S. Oreifej, R. Al-haddad, **R. Zand**, R. A. Ashraf, and R. F. DeMara, "Survivability Modeling and Resource Planning for Self-Repairing Reconfigurable Device Fabrics," *IEEE Transactions on Cybernetics,*, 2017.
- A. Roohi, **R. Zand**, D. Fan, and R. F. DeMara, "Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2017.
- M. Krishna, A. Roohi, **R. Zand**, and R. F. DeMara, "Heterogeneous Energy-Sparing Reconfigurable Logic:Spin-based Storage and CNFET-based Multiplexing," *IET Circuits, Devices and Systems*, 2017.
- A. Roohi, **R. Zand**, R. Ewetz, and R. F. DeMara, "An Evolutionary Optimization Approach to Implement Logic-in-Memory Architecture Using Spintronic Devices," *ICCAD*, 2017,*under review.*
- **R. Zand**, A. Roohi, S. Salehi, and R. F. DeMara, "Scalable Adaptive Spintronic Reconfigurable Logic using Area-Matched MTJ Design," *IEEE Transactions on Circuits and Systems II*, 2016.
- A. Roohi, **R. Zand**, and R. F. DeMara, "A Tunable Majority Gate based Full Adder using Current-Induced Domain Wall Nanomagnets," *IEEE Transactions on Magnetics*, 2016.
- A. Roohi, **R. Zand**, and R. F. DeMara, "A Parity Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency," *IEEE Transactions on Emerging Topics in Computing*, 2016.
- R. Al-haddad, R. S. Oreifej, **R. Zand**, A. Ejnioui, and R. F. DeMara, "Adaptive Mitigation of Radiation-Induced Errors and TDDB in Reconfigurable Logic Fabrics," *EEE North Atlantic Test Workshop (NATW), 2015.*
- R. A. Ashraf, A. Al-Zahrani, N. Khoshavi, **R. Zand**, S. Salehi, A. Roohi, M. Lin, and R. F. DeMara, "Reactive Rejuvenation of CMOS Logic Paths using Self-Activating Voltage Domains," *IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal*, 24-27 May, 2015.
- **R. Zand**, S.B. Shouraki, "Designing a Fuzzy Logic Controller for a Quadruped Robot Using Human Expertise Extraction," *21st Iranian Conference on Electrical Engineering, 2013.*

Professional Services

IEEE Transactions on Circuits and Systems II, Reviewer.

IEEE Transactions on Emerging Topics in Computing, Reviewer.

IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2016 & 2017), Sub-Reviewer.

Spring 2017 **NSF-SRC Energy-Efficient Computing: from Devices to Architectures(E2CDA) Collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Probabilistic Spin Logic for Low-Energy Boolean and Non-Boolean Computing".

Fall 2016 **NSF Software and Hardware Foundations (SHF-medium) collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Ultra-Low Energy Computing using Magnetoelectric-based Concatenable Switching Elements".

Fall 2016 **NSF Software and Hardware Foundations (SHF-small) collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Elastic Intermittent Computation for Energy Harvesting Powered Devices".

Spring 2016 **Air Force Research Laboratory White Paper**, Leading the student contributions to prepare the white paper titled "Pinpoint Vertical Integration of Spintronic Devices for Run-time Adaptive Resiliency".

Spring 2016 **NSF-SRC Energy-Efficient Computing: from Devices to Architectures(E2CDA) Collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Belief Networks with Voltage Controlled Switches".

Fall 2015 **NSF Software and Hardware Foundations (SHF) Proposal**, Leading the student contributions to prepare the proposal titled "Heterogeneous Technology Fabrics for Next Generation Reconfigurable Computing".

Honors and Awards

2016 **Ph.D. Forum at DAC Scholarship**, with acceptance rate around 30%.

2016 **Invited talk at UCF Graduate Student Symposium**, Title: Scalable Spintronic Reconfigurable Logic for Next Generation Reconfigurable Computing.

2013 **Robocup World Championship**, 3rd place in Small Size League as a member of MRL team.

Selected Academic Projects

Ph.D.

2016-present **Spin-based ASIC design for adaptive resiliency and energy-harvesting applications**.

- Develop a spin-based majority logic synthesis and optimization tool using Genetic Algorithm in Python.
- Develop a spin-based gate library containing the complete set of Boolean functions.

2016 **Microelectronic Fabrication**.

- Seminar on Fundamentals of Magnetic Tunnel Junctions and their fabrication process.
- Fabrication of 200um and 400um MOS transistors using photolithography and single diffusion process.
- Fabrication of BJT transistors and diodes using photolithography and double diffusion process.

2015-2016 **Modeling the bahavior of Magnetic Tunnel Junctions (MTJs)**.

- Verilog-A model of 2-terminal and 3-terminal Magnetic Random Access Memories (MRAMs).
- Matlab model of Spin Hall Effect(SHE) assisted Spin Transfer Torque (STT) switching approach.

2014-2016 **Spin-based Circuit Design**.

- 6-input fracturable SHE-MRAM based Lookup Table (LUT) circuit.
- 8-input Adaptive STT-MRAM based Lookup Table (LUT) circuit.
- Voltage-controlled Concatenable SHE-MRAM based 1-bit Full-Adder(FA) circuit.
- Current-mode Tunable Domain Wall Nanomagnet based 1-bit Full-Adder(FA) circuit.

M.Sc.

- **Digital ASIC Design:**Design and Verification of USB 2.0 Protocol Layer using Verilog HDL.
- **FPGA Design:** Design and Verification of 5-stage pipelined MIPS processor including scoreboarding and dynamic branch prediction.
- **FPGA Design:** Design and Verification of a floating Point ALU using Verilog HDL.

Technical Skills

- **Hardware Description and behavioral Languages:** Verilog, Verilog-A.
- **Scripting Languages:** Matlab, Python.
- **Programming Languages:** C, Assembly.
- **Design and Verification Tools:** HSPICE, Synopsys Design Compiler, Cadence Virtuoso, Xilinx-ISE, Quartus, ModelSim.
- **Parallel Programming:** MPI, Pthread, CUDA.
- **Operating Systems:** Windows, Linux.