Rizwan A. Ashraf

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Education

- **University of Central Florida (UCF)** Orlando, FL
  Ph.D. Computer Engineering, May 2015
  - Dissertation: "Adaptive Architectural Strategies for Resilient Energy-Aware Computing"
  - Advisor: Professor Dr. Ronald F. DeMara
  - Research Interests: Low Power and Reliability-aware Embedded Systems, High Performance Computing, Reliable Computer Architectures, Adaptive Computing Systems, FPGAs

  M.S. Computer Engineering, May 2013
  - GPA: 4.0/4.0
- **University of Engineering & Technology (UET)** Lahore, Pakistan
  B.S. Electrical Engineering, Jan. 2007
  - Overall Score: 81/100
  - Top 10% of Graduating Class

Professional Experience

- **University of Central Florida** Orlando, FL
  Graduate Research Assistant *Jan 2015 – Present*
  - Collaborative Dissertation Research with PNNL
  - Project:"Adaptive Techniques for Resiliency in HPC Systems"
- **Pacific Northwest National Laboratory (PNNL)** Richland, WA
  Ph.D. Intern *June 2014 – Dec 2014*
  - Mentor: Dr. Roberto Gioiosa
  - Developed LLVM-based framework to 'inject and track' transient faults in HPC Applications to assess vulnerability on large-scale systems and tradeoff Performance-Resiliency at Runtime
  - Conducted research on Adaptive Runtime Systems with focus on 'Resiliency'
  - Participated in biweekly research meetings with IBM T. J. Watson Research Center
  - Co-authored research publication
- **University of Central Florida** Orlando, FL
  Graduate Research Assistant *Jan 2014 – May 2014*
  - Conducted Reconfigurable Architecture and VLSI circuit research, simulation, and submitted four publications
  - Project:"Critical Path Adaption for Datapath Resilience and Lifetime Energy Reduction"

  Graduate Teaching Assistant *Jan 2010 – Dec 2013*
  - Taught weekly labs to about 80 students per semester; including grading of assignments

- **Computer System Design II (EEL-4768)**: assisted in development of labs for implementation of a RISC processor on an FPGA board
- **Embedded Systems (EEL-4742)**: the lab included extensive programming tasks for interfacing to TI's MSP430 Microcontroller
- **Digital Systems (EEE-3342)**: the lab included programming Xilinx FPGAs using Verilog
- **Computer Organization (EEL-3801)**: assisted in design of class notes; the course covered MIPS programming tasks
- **Electronics I (EEE-3307)**: the labs included breadboard prototyping of electronic circuits

- **University of Engineering & Technology** Lahore, Pakistan
  Lecturer *May 2007 – Aug 2009*
  - Instructor of Record for B.S. level courses: Digital Signal Processing, Digital Systems, Electric Circuits; prepared lecture material, homework and exam contents, and assigned grades
  - Assisted in upgrade of lab equipment such as Xilinx FPGA boards

- **Wateen Telecom** Lahore, Pakistan
  Test Engineer *Jan 2007 – May 2007*
  - Responsible for testing Voice over IP services on a WiMAX (IEEE 802.16) network

Research Publications

Journal Articles

1. **R. A. Ashraf**, A. Al-Zahrani, N. Imran, N. Khoshavi, M. Lin and, R. F. DeMara, "Autonomous Circuit-level Adaptation for Datapath Resilience and Lifetime Energy Reduction," *IEEE Transactions on Computers (under Review)*, Jan 2015.

2. N. Imran, **R. A. Ashraf**, J. Lee and R. F. DeMara, "Activity-Based Resource Allocation for Motion Estimation Engines," *Journal of Circuits, Systems and Computers*, vol.24, no.1, pp.1550004 (32 pages), 2015.

3. N. Imran, **R. A. Ashraf**, and R. F. DeMara, "Power and Quality-Aware Image Processing Soft-Resilience using Online Multi-Objective GAs," *International Journal of Computational Vision and Robotics (in Press)*, Feb 2014.

4. **R. A. Ashraf** and R. F. DeMara, "Scalable FPGA Refurbishment Using Netlist Driven Evolutionary Algorithms," *IEEE Transactions on Computers*, vol.62, no.8, pp.1526–1541, Aug 2013.

5. R. Al-Haddad, R. Oreifej, **R. A. Ashraf**, and R. F. DeMara , "Sustainable Modular Adaptive Redundancy Technique Emphasizing Partial Reconfiguration for Reduced Power Consumption," *International Journal of Reconfigurable Computing*, vol. 2011, July 2011.

Peer-Reviewed Conferences and Workshops

1. **R. A. Ashraf**, R. Gioiosa, G. Kestor, and R. F. DeMara, "Impact of Compiler Optimizations on the Vulnerability of HPC Applications," *submitted to the 5th Fault Tolerance for HPC at eXtreme Scale Workshop (FTXS 2015)*, held in conjunction with 24th International ACM Symposium on High Performance Distributed Computing, Portland, OR, June 15, 2015.

2. **R. A. Ashraf**, R. Gioiosa, G. Kestor, and R. F. DeMara, "Understanding the propagation of transient errors in HPC Applications," *submitted to the 29th International Conference on Supercomputing (ICS 2015)*, Newport Beach, CA, June 8-11, 2015.

3. **R. A. Ashraf**, A. Al-Zahrani, N. Khoshavi, R. Zand, S. Salehi, A. Roohi and R. F. DeMara, "Reactive Rejuvenation of CMOS Logic Paths Using Self-Activating Voltage Domains," *accepted to the IEEE International Symposium on Circuits & Systems (ISCAS 2015)*, Lisbon, Portugal, May 24-27, 2015.

4. R. Oreifej, R. Al-Haddad, **R. A. Ashraf**, and R. F. DeMara, "Sustainability Assurance Modeling for SRAM-based FPGA Evolutionary Self-Repair," *IEEE International Conference on Evolvable Systems (ICES 2014)*, Orlando, FL, Dec 9-12, 2014.

5. N. Khoshavi, **R. A. Ashraf**, and R. F. DeMara, "Applicability of Power-Gating Strategies for Aging Mitigation of CMOS Logic Paths," *IEEE 57th Int'l Midwest Symposium on Circuits and Systems (MWSCAS 2014)*, College Station, TX, August 2014.

6. **R. A. Ashraf**, A. Al-Zahrani and R. F. DeMara, "Extending Modular Redundancy to NTV: Costs and Limits of Resiliency at Reduced Supply Voltage," *2nd Workshop on Near Threshold Computing (WNTC 2014)*, held in conjunction with 41st International Symposium on Computer Architecture (ISCA), Minneapolis, MN, June 2014.

7. N. Imran, **R. A. Ashraf**, and R. F. DeMara, "Evaluating Quality and Resilience of an Embedded Video Encoder against a Continuum of Energy Consumption," *DAC Workshop on Suite of Embedded Applications and Kernels (SEAK 2014)*, held in conjunction with DAC 2014, San Francisco, CA, June 2014.

8. **R. A. Ashraf**, A. Al-Zahrani, and R. F. DeMara, "Exploring Spatial Redundancy to Mitigate Aging-Induced Timing Degradation," poster presentation in *Design Automation Conference (DAC 2014)*, San Francisco, CA, June 2014.

9. **R. A. Ashraf** and R. F. DeMara, "Scalability of Modular Redundancy for Near-Threshold Computing," *2nd Workshop on Highly-Reliable Power-Efficient Embedded Designs (HARSH 2014)*, held in conjunction with 20th International Symposium on High-Performance Computer Architecture (HPCA), Orlando, FL, Feb 2014.

10. N. Imran, **R. A. Ashraf**, and R. F. DeMara, "On-demand Fault Scrubbing Using Adaptive Modular Redundancy," *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2013)*, Las Vegas, NV, July 2013.

11. **R. A. Ashraf**, F. Luna, D. Dechev and R. F. DeMara, "Designing digital circuits for FPGAs using Parallel Genetic Algorithms," *Symposium on Theory of Modeling and Simulation (TMS 2012)*, Orlando, FL, Mar 2012.

12. **R. A. Ashraf**, O. Mouri, R. Jadaa and R. F. DeMara, "Design-For-Diversity for Improved Fault-Tolerance of TMR Systems on FPGAs," *International Conference on ReConFigurable Computing and FPGAs (ReConFig 2011)*, Cancun, Mexico, Dec 2011.

13. **R. A. Ashraf**, R. Oreifej and R. F. DeMara, "Scalability of Sustainable Self-Repair to Mitigate Aging Induced Degradation in SRAM-based FPGA Devices," *ReSpace/Military Aerospace Programmable Logic Devices (MAPLD) 2011 Conference*, Alburburque, NM, Aug 2011.

14. R. F. DeMara, J. Lee, R. Al-Haddad, R. Oreifej, **R. A. Ashraf**, et al., "Dynamic Partial Reconfiguration Approach to the Design of Sustainable Edge Detectors," *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2010)*, Las Vegas, NV, June 2010.

15. F. A. Khan, **R. A. Ashraf**, et al., "Resource Efficient Parallel Architectures for Linear Matrix Algebra in Real-time Adaptive Control Algorithms on Reconfigurable Logic," *2nd International Conference on Electrical Engineering (ICEE 2008)*, Lahore, Pakistan, March 2008.

Presentations/Participation in Conferences

- **41st Int'l Symposium on Computer Architecture** — Minneapolis, MN, *June 16 – 18, 2014*
- **Second Workshop on Near-Threshold Computing** — Minneapolis, MN, *June 14, 2014*
- **51st Design Automation Conference** — San Francisco, CA, *June 3 – 5, 2014*
- **DAC Workshop on Suite of Embedded Applications and Kernels** — San Francisco, CA, *June 1, 2014*
- **20th Int'l Symposium On High Performance Computer Architecture** — Orlando, FL, *Feb 17 – 19, 2014*
- **2nd Workshop on Highly-Reliable Power-Efficient Embedded Designs** — Orlando, FL, *Feb 16, 2014*
- **NSF I/UCRC - Multi-Functional Integrated System Conference** — Gainesville, FL, *Nov 19 – 20, 2013*
  University of Florida
- **Symposium on Theory of Modeling & Simulation** — Orlando, FL, *March 26, 2012*
- **Int'l Conference on ReConFigurable Computing and FPGAs** — Cancun, Mexico, *Nov 30 – Dec 2, 2011*

Academic Service/Development

- Refereed papers for the following journals/conferences:
  - **IEEE Transactions on Computers** (Years 2012, 2013, 2014)
  - **IEEE Computer Society Annual Symposium on VLSI** (ISVLSI 2011)
- Student Member IEEE
- Training Course: *Preparing Tomorrow's Faculty*
  May 2012 – August 2012

Selected Graduate Coursework

- **Full-Custom VLSI Design (EEE-5390) – Audit** — Spring 2013
  - Taped out a LFSR design, which was fabricated using the AMI C5F/N Process (MOSIS)
- **Performance Models of Computers & Networks (CDA-6530)** — Fall 2011
  - Analysis techniques including probability, stochastic and queuing network techniques
- **Parallel Computer Architecture (CDA-6107)** — Spring 2011
  - Principles and tradeoffs in the design of data-parallel architectures, cache-coherence protocols

  - Programming tasks (Matrix Algebra) for shared-memory and message-passing machines
- **Parallel Architecture and Algorithms (CDA-5110)** Spring 2011
  - Implementation of various Parallel Algorithms using pthreads in C++
- **Current Topics in Parallel Processing (ECM-6308)** Fall 2010
  - FPGA-based Intrinsic/Extrinsic Evolution; Autonomous Regeneration Techniques
- **Neuroevolution and Generative and Developmental Systems (CAP-6616)** Fall 2010
  - Research seminars on automated techniques for generating Artificial Neural Networks
- **Design of Video Coding Systems (EEE-6327)** Spring 2010
  - Study of H.264/AVC components such as motion estimation, transforms, entropy coding
- **Field Programmable Gate Array Design (EEL-5722C)** Fall 2009
  - Projects implemented tasks such as FPGA interfacing to VGA, keyboard, and image filtering
- **Advance Computer Architecture (CDA-5106)** Fall 2009
  - Superscalar processors; Instruction Level Parallelism (ILP); Thread Level Parallelism (TLP)

Selected Research Projects

Logic Design

- Implementation and Fabrication of a LFSR Integrated Circuit containing a **Hardware Trojan**
- Development of an **Electronic Measurement System** for DC Voltage, Current, Power and Frequency interfaced with a PC using 8051 microcontroller

Evolvable Hardware

- Explored fault tolerance capabilities of **Neuro-evolutionary** based robot controllers
- **Transient Fault Recovery** capability prototyped in a Xilinx Virtex-4 FPGA device for autonomous computing applications
- Extended support for **dynamic faults** during FPGA regeneration operation

Computer Architecture

- Developed a **Reconfigurable Motion Estimation (H.263) Engine** in Verilog HDL supporting scalable block sizes, search sizes and various search patterns
- **Split D-Cache**: Data cache split into multiple sub-caches for increased performance demonstrated through implementation on SimpleScalar simulator
- Performance of **PageRank** and Hyperlink-Induced Search Algorithms compared using multiple web-graphs generated through the internet
- FPGA based Scalable, Systolic, Pipelined implementation of **Discrete-Time Kalman filter** using floating point and fixed point arithmetic

Technical Skills

- **Tools and Systems**
  - **EDA:** Xilinx tools (ISE, EDK), Berkeley ABC (synthesis and verification tool), Synopsys Design Compiler, Cadence Virtuoso
  - **Modeling and Simulation:** HSPICE, MOSRA (reliability analysis tool), MATLAB, NS2
  - **Compiler Systems:** LLVM compiler infrastructure, LLFI compiler-level fault injector
- **Processor Hardcores and Fabrics**
  - Xilinx Spartan 3, Virtex II Pro, Virtex 4 FPGAs, Intel x86, TI MSP430
- **Programming Languages**
  - **Hardware:** Verilog HDL, Spice
  - **Software:** Assembly Language (x86, MIPS), LLVM-IR, C/C++ (Intel TBB, OpenMP, Open MPI), Java, TCL, Python, Perl
- **Document Production**
  - LaTeX, WinEdt, Gnuplot, Microsoft Office