

Steven D. Pyle

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Education

- 2015 – Present **PhD**, *Computer Engineering*, EECS Department, University of Central Florida, Orlando, FL.
Advisor: Dr. Ronald F. DeMara
- **Coursework:** Fabrication of Solid-State Devices, Special Topics in Emerging Computing Architectures, Neuromorphic Computing Architectures, Modeling Neuronal Systems, Full-Custom VLSI Design, Current Topics in Parallel Processing, and Complex Adaptive Systems.
- 2014 – 2015 **MSc**, *Electrical Engineering*, EECS Department, University of Central Florida, Orlando, FL.
Advisor: Dr. Ronald F. DeMara
- **Thesis Title:** Self-Scaling Evolution of Analog Computation Circuits.
- 2011 – 2014 **BSc**, *Electrical Engineering*, EECS Department, University of Central Florida, Orlando, FL.
- 2008 – 2011 **AA**, *Electrical Engineering Track*, Valencia Community College, Orlando, FL.

Research Interests

- Emerging Nanoscale Electronics, particularly Spintronic Devices
- Intelligent, Reconfigurable, and Adaptive Computer Architectures
- Neuromorphic Algorithm and Hardware Co-Design
- In-Memory Computing

Research Experience

- Fall 2016 - Present **Publication Coordinator**, "COMPUTER ARCHITECTURE LAB (CAL)", Electrical Engineering and Computer Science Department, University of Central Florida, Orlando, Florida, USA.
- Responsibilities: In-depth editing and review of all group publications. Maintenance of group publication calendar.
- 2014 - Present **Graduate Research Assistant**, "COMPUTER ARCHITECTURE LAB (CAL)", Electrical Engineering and Computer Science Department, University of Central Florida, Orlando, Florida, USA.
- Lead the architectural portion of a successfully funded multi-million dollar collaborative NSF-SRC Proposal (E2CDA). Developed novel circuit, architecture, and algorithm research towards future computational hardware utilizing spintronic devices.

Work Experience

- 2014-Present **Graduate Assistant**, "EVALUATION AND PROFICIENCY CENTER (EPC)", University of Central Florida, Orlando, FL.
- Plays a pivotal role in the development of infrastructure, procedures, and online question content for secure quiz delivery interwoven with post-testing review.
 - Lead assistant in 120-seat testing center to proctor computer-based examinations for Electrical and Computer Engineering undergraduate courses.
 - Provide review-based tutoring for students.
 - Developed high-quality electronically-delivered question content used in Electrical and Computer Engineering undergraduate courses.

Publications

Journal Publications

- R. Zand, K. Y. Camsari, I. Ahmed, **S. D. Pyle**, C. H. Kim, S. Datta, and R. F. DeMara, "R-DBN: A Resistive Deep Belief Network Architecture Leveraging the Intrinsic Behavior of Probabilistic Devices," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, under review.
- **S. D. Pyle**, K. Y. Camsari, and R. F. DeMara, "Hybrid Spin-CMOS Stochastic Spiking Neuron for High-Speed Emulation of In-Vivo Neuron Dynamics," in *IET Computers and Digital Techniques SI: Bio-Inspired Hardware and Evolvable Systems*, under review.
- **S. D. Pyle**, D. Fan, and R. F. DeMara, "Compact Spintronic Muller C-Element with Near-Zero Standby Energy," accepted to *IEEE Transactions on Magnetics* on 23 October 2017.
- **S. D. Pyle**, H. Li, and R. F. DeMara, "Compact Low-Power Instant Store and Restore D Flip-Flop using a Self-Complementing Spintronic Device," *IET Electronics Letters (IEEE indexed)*, Vol. 52, No. 14, pp. 1238 - 1240, June 2016. DOI: 10.1049/el.2015.4114. **Featured Paper of the Issue**, including author interview of topic area and field outlook.

Conference Publications

- **S. D. Pyle** and P. K. Douglas, "Evolution of Biologically-Inspired Ion Channel Neural Networks for Simple Brain Behaviours," in *Cognitive Computational Neuroscience (CCN 2017)*, Poster with abstract. New York, NY, USA, September 6 - 8, 2017.
- **S. D. Pyle**, V. Thangavel, S. M. Williams, and R. F. DeMara, "Self-Scaling Evolution of Analog Computation Circuits with Digital Accuracy Refinement," in *IEEE Proceedings of NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2015)*, pp. 1 - 8, Montreal, QC, Canada, June 15 - 18, 2015. **Best paper award**, Citation: "Best Design Paper."

STEM Educational Publications

- R. F. DeMara, N. Khoshavi, **S. Pyle**, J. Edison, R. Hartshorne, B. Chen, M. Georgiopoulos, "Redesigning Computer Engineering Gateway Courses using a novel Remediation Hierarchy," in *Proceedings of American Association for Engineering Education National Conference (ASEE-16)*, New Orleans, LA, USA, June 26 - 29, 2016.

Professional Services

IEEE Transactions on Computers, Reviewer.

IEEE Transactions on Emerging Topics in Computing, Reviewer.

ASEE Annual Conference 2016 & 2017, Reviewer.

- Summer 2017 **STEM Assessment Assistant**, Advisement of faculty at all levels (Lecturer through Professor) on digitization of engineering assessments, construction of computer-based exams, and remediation methods.
- Spring 2017 **NSF-SRC Energy-Efficient Computing: from Devices to Architectures (E2CDA) Collaborative Proposal**, Lead the circuit and architectural contributions to prepare the proposal titled "Probabilistic Spin Logic for Low-Energy Boolean and Non-Boolean Computing".
- Fall 2016 **NSF Software and Hardware Foundations (SHF-medium) collaborative Proposal**, Provided significant contributions to prepare the proposal titled "Ultra-Low Energy Computing using Magnetoelectric-based Concatenable Switching Elements".
- Spring 2016 **NSF-SRC Energy-Efficient Computing: from Devices to Architectures(E2CDA) Collaborative Proposal**, Lead the circuit and architectural contributions to prepare the proposal titled "Belief Networks with Voltage Controlled Switches".
- Fall 2015 **NSF Software and Hardware Foundations (SHF) Proposal**, Contributed to the proposal titled "Heterogeneous Technology Fabrics for Next Generation Reconfigurable Computing".
- Spring 2015 **Air Force Research Laboratory White Paper**, Contributed to prepare the white paper titled "Reconfigurable Spintronic Fabric using Domain Wall Nanomagnet-based Ladders".

Fall 2014 **2014 IEEE International Symposium Series on Computational Intelligence (SSCI)**, Volunteer work for attendee registration and distribution of conference materials. Ensured that the services provided by the hosting hotel were of highest quality. Resolved any issues that arose with participants.

Invited Talk and Technical Presentations

2016, 2017 **Panelist**, STEM GRADUATE SCHOLAR ASSISTANT ROLES OF THE FUTURE., *University of Central Florida*, Orlando.

Awards and Recognitions

2016 **Featured Paper and Interview**, IET Electronics Letters.

2015 **Best Paper Award**, NASA/ESA Conference on Adaptive Hardware and Systems, Best design paper of conference.

Technical Skills

- **Hardware Description and Behavioral Languages:** Verilog, Verilog-A, VHDL.
- **Programming Languages:** C, C++, Assembly, Matlab, Python, Javascript.
- **Design and Verification Tools:** HSPICE, Cadence Virtuoso, Xilinx-ISE, EAGLE.
- **Micromagnetic Simulation:** MuMax3, OOMMF.

Additional Works

2017 **Actor**, EVALUATION AND PROFICIENCY CENTER, University of Central Florida, Orlando, FL. Video of Procedures for Digitized STEM Assessments in the Evaluation and Proficiency Center

References

Ronald F. DeMara, Ph.D, *Professor*, EECS Department, University of Central Florida.
E-Mail: rdemara [AT] ucf.edu

Parveen F. Wahid, Ph.D, *Professor*, EECS Department, University of Central Florida.
E-Mail: parveen.wahid [AT] ucf.edu

Deliang Fan, Ph.D, *Assistant Professor*, EECS Department, University of Central Florida.
E-Mail: dfan [AT] ucf.edu