Abstract—Aggressive Metal Oxide Semiconductor (MOS) technology scaling in digital circuits has resulted in important challenges including significant increase in leakage currents, short-channel effects, and drain saturation growth while reducing the power supply voltage for digital applications. Furthermore, by extensions to sub 10-nm regimes, error resiliency has become a major challenge for microelectronics industry, particularly mission critical systems, e.g. space and terrestrial applications. Therefore, emerging devices and technologies have attracted considerable attention in recent years as an alternative for CMOS based technologies such as spintronic [1-6], resistive random access memory (RRAM) [7-10], phase change memory (PCM) [11, 12], and Quantum Cellular Automata (QCA) [13-18]. Among promising devices, the 2014 Magnetism Roadmap [19] identifies nanomagnetic devices as capable post-CMOS candidates, of which Magnetic Tunnel Junctions (MTJs) are considered as one of the most promising technologies spanning both logic [20-22] and memory functionalities [23-26]. MTJs are characterized by non-volatility, near-zero standby power, high integration density, and radiation-hardness, as a technology progression from CMOS. Moreover, MTJ can be readily integrated at the back-end process of the CMOS fabrication, due to its vertical structure [27, 28]. In this book chapter, we will focus on fundamentals and modeling of the MTJs using precise physics equations. Moreover, some of their applications in reconfigurable fabrics and logic-in-memory architectures will be studied.
SUMMARY

In this chapter, first we have focused on the fundamentals and modeling of both Spin Transfer Torque (STT)-based and Spin Hall Effect (SHE)-based Magnetic Tunnel Junctions (MTJs), which have recently attracted significant attentions as promising alternatives for CMOS devices in both memory and logic applications. Next, MTJ-based Lookup Table (LUT) circuits were studied as the primary building blocks for reconfigurable fabrics namely Field Programmable Gate Arrays (FPGAs). In particular, detailed descriptions were provided regarding the structure of adaptive STT-MTJ based LUT and fracturable SHE-MTJ based LUT circuits which are proposed by authors in [94] and [57], respectively. Moreover, we have explained the structure of a Logic-In-Memory (LIM) SHE-MTJ based Full Adder (FA) circuit proposed by authors in [21], which implements one of the most important mathematical operation, i.e. binary addition. SHE-based Majority Gates (MGs) were utilized as the building blocks of the proposed SHE-FA. SHE-MTJ based MGs can be cascaded to realize conjunctive/disjunctive Boolean gate realizations enabling the implementation of larger scale logic designs. Herein, we have described the application of MTJs in reconfigurable fabrics and LIM architectures, and provided some examples of the corresponding MTJ-based circuits. However, the application of MTJ devices are not limited to these examples, and there are a wide range of applications that have been studied in recent years, including: neuromorphic computing [115-120], associative computing [52, 121, 122], and secure and intermittent computing for energy-harvesting-powered Internet-of-Things (IoT) devices [123-128]. Readers are referred to the mentioned references for additional information regarding the recent application of MTJ devices.
REFERENCES


