# MISC: A MASSIVELY PARALLEL ARCHITECTURE FOR ASSOCIATIVE-BASED ARTIFICIAL INTELLIGENCE

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## Abstract

Parallel architectures are required to provide the computational power for future artificial intelligence research and applications. Massively parallel processing is emerging as an important alternative to prior approaches to parallel AI. Unfortunately, contemporary general-purpose machines are optimized for numeric codes while application-specific machines do not fully address the wide variety of algorithms needed by large-scale knowledge processing. This dissertation investigates overcoming these limitations through associative content-based processing of complex dynamic data objects, focusing on retrieval from large knowledge bases. Analysis of algorithm-architecture-technology interactions is the foundation of the MISC architecture development. To accomplish this, we develop an associative pseudocode, new parallel algorithms, and an enhanced design tool. The SEGUL pseudocode features nested multisets, allowing the expression of knowledge processing algorithms in a machine-independent manner for subsequent characterization. Three algorithms serve as the focus of the analysis: an associative memory neural network, a semantic network, and a graph knowledge-base. Suspense, the early analysis tool, projects speed and cost measures for architectural alternatives. Functional-level simulation combined with early analysis of a hypothetical implementation provide cost-performance projections for evaluating the resulting architecture. The MISC system architecture is comprised of multiple small data-parallel arrays, as the the number of processors required by any one of the algorithms scales sublinearly with respect to the knowledge base size. The array processors feature a general-purpose core and additional functional units to improve content-based knowledge processing. Each processor also has high bandwidth access to a large off-chip memory, and inter-processor communication is by a wide-link extended mesh network. Analysis shows that advanced packaging is a cost-effective means of achieving the required high connectivity. Simulation of the MISC architecture for the suite of three algorithms indicates more than a factor of ten improvement in both speed and cost-performance over a massively parallel architecture tailored for numeric codes.

## References

R. F. DeMara, and Dan I. Moldovan. "The SNAP-1 parallel AI prototype." *Parallel and Distributed Systems, IEEE Transactions on* 4, no. 8 (1993): 841-854.