ALLNODE Barrier Synchronization Network

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Abstract

This paper presents a proposed hardware solution using an existing multi-stage switching network for synchronizing N multiple processors at predetermined programmable barriers The technique permits all N processors to access the network simultaneously and to perform synchronization in parallel using only several network cycles The synchronization requires no additional network facilities, and consumes usually less than *5%* of the bandwidth when merged onto the same multi-stage network that handles normal message traffic. The approach permits up to 2048 harriers, but can be expanded. The network is based oil the Allnode Switch and Network concepts [l], a circuit-switching implementation that permits a special barrier synchronization mode where all N processors are simultaneously attached to the network and can interact as if they were attached to a multi-drop bus.

References

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