Computer Architecture Lab's Citings through 2019: Group Seven

Arman Roohi, Webmaster
Computer Architecture Lab
University of Central Florida
Orlando, Florida 32816-2362
E-mail: aroohi@knights.ucf.edu

Abstract — **Citations which have been made. yet were not indexed, are summarized herein. The citing document is listed and the cited articles are noted. These are compiled and thus indexed for rapid identification within both printed and electronically-formatted books. By checking each of the entries, the hyperlink may be followed to view the book and cited articles. Only items which are not proceedings volumes have been included. These entries may be readily obtained at oversea.cnki.net**

Keywords — Citing article, Citation index, Cited articles, Book citations.

1.0 Introduction

In this paper, the primary focus is to identify book citations for rapid retrieval. The paper provides a concise list of them that would not otherwise be available in a single document. Sources listed were obtained via web search and then filtered as indicated below. Searches included "R.F. DeMara" and "DeMara, R" as well as "R DeMara" which were then inspected manually for matching content.

2.0 Google Books and Related Citings

The graduate thesis "Research on Evolutionary Adaptive System Based on Digital Circuit" by Xiaoyan Yang at Wuhan University was published in 2018 which cited [1][2][3].

The graduate thesis "Research on Circuit Testing Technology of Dynamic Reconfigurable FPGA" by Lou Yi Yang at University of Electronic Science and Technology in China was published in 2009 which cited [4].

The graduate thesis "Design of Asynchronous Zero Protocol Arithmetic Logic Unit" by Haixiang Pan from Jiangnan University was published in 2008 which cited [5][6].

The graduate thesis "Simulation Research on Queuing Problem of Passenger and Freight Ro-Ro Transportation in Qiongzhou Strait" by Zhenyu Guo from South China University of Technology was published in 2015 which cited [7].

The graduate thesis "The Study of Design Method for Circuit Fault-tolerance Based on Association Selection Strategy" by Jie Yu from Hebei University of Science Technology was published in 2019 which cited [9].

The graduate thesis “Research on Data Mining-Based Suspicious Money Laundering Transactional Behavioral Patterns Recognition” by Zhiqiang Li from Southwest Jiaotong University was published in 2008 which cited [10].

The graduate thesis “Heterogeneous Multi-processor Paltform for Dynamic Reconfigurable Technology Research” by Yuanzhi Lai from] Harbin Institute of Technology was published in 2014 which cited [11].

3.0 Conclusion

Citations appear on the pages as mentioned. Based on the citations above, it is possible to rapidly locate the articles by google scholar search using the stated booked titles. The cited articles are listed as indicated.

References

[1] R. Al-Haddad, R. Oreifej, R. A. Ashraf, and R. F. DeMara, “Sustainable Modular Adaptive Redundancy Technique Emphasizing Partial Reconfiguration for Reduced Power Consumption,” *International Journal of Reconfigurable Computing*, Article ID 430808, June, 2011, pp 1 – 25, 2011. doi:10.1155/2011/430808.

[2] R. F. DeMara, K. Zhang, and C. A. Sharma “Autonomic Fault-Handling and Refurbishment Using Throughput-Driven Assessment,” *Applied Soft Computing,* Volume 11, Issue 2, March 2011, pp. 1588 – 1599.

[3] R.S. Oreifej and R.F. DeMara, “Intrinsic Evolvable Hardware Platform For Digital Circuit Design And Repair Using Genetic Algorithms,” *Applied Soft Computing*, 2012, doi:10.1016/j.asoc.2012.03.032, Vol. 12, Issue 8, August 2012, pp. 2470 – 2480.

[4] R. F. DeMara and K. Zhang, “Autonomous FPGA Fault Handling through Competitive Runtime Reconfiguration,” in *Proceedings of the NASA/DoD Conference on Evolvable Hardware*, pp. 109 – 116, Washington D.C., U.S.A., June 29 – July 1, 2005.

[5] S. C. Smith, R. F. DeMara, J. S. Yuan, M. Hagedorn, and D. Ferguson, “Speedup of Delay-Insensitive Digital Systems Using NULL Cycle Reduction,” in *Proceedings of the 2001 International Workshop on Logic and Synthesis (IWLS’01)*, pp. 185 – 189, Granlibakken, California, U.S.A., June 12 – 15, 2001.

[6] S. C. Smith, R. F. DeMara, J. S. Yuan, D. Ferguson, and D. Lamb, “Optimization of NULL Convention Self-timed Circuits,” *Integration, The VLSI Journal*, Vol. 37, No. 3, August, 2004, pp. 135 – 165.

[7] H. A. Bahr and R. F. DeMara, “Smart Priority Queue Algorithms for Self-optimizing Event Storage,” *Simulation Modeling Practice and Theory*, Vol. 12, No. 1, April, 2004, pp. 15 – 40.

[8] A. J. Rocke and R. F. DeMara, “CONFIDANT: Collaborative object notification framework for insider defense using autonomous network transactions,” *Journal of Autonomous Agents and Multi-Agent Systems*, Vol. 12, No. 1, January, 2006, pp. 93 – 114.

[9] C. A. Sharma, A. Sarvi, A. Al-Zahrani, and R. F. DeMara, “Self-Healing Reconfigurable Logic using Autonomous Group Testing,” Microprocessors and Microsystems, Volume 37, Issue 2, March 2013, pp. 174 – 184.

[10] R. C. Watkins, K. M. Reynolds, R. F. DeMara, M. Georgiopoulos, A. J. Gonzalez, and R. Eaglin, “Exploring Data Mining Technologies as Tools to Investigate Money Laundering,” *Journal of Policing Practice and Research: An International Journal*, Vol. 4, No. 2, January, 2003, pp. 163 – 178.

[11] J. Huang, M. Parris, J. Lee, and R. F. DeMara, "Scalable FPGA Architecture for DCT Computation using Dynamic Partial Reconfiguration," in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA '07)*, Las Vegas, Nevada, U.S.A., July 14 – 17, 2008.