# Mousam Hossain

## CONTACT INFORMATION:

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## EDUCATION:

**Ph.D. Computer Engineering** **August 2019- Present**
University of Central Florida, Orlando, FL, US
Advisor: **Dr. Ronald DeMara**

**M.S. Electrical and Computer Engineering** **August 2017- July 2019**
GPA- **4.0/4.0**
North Dakota State University (NDSU), Fargo, ND, US
Advisors: **Dr. Sudarshan K. Srinivasan and Dr. Scott C. Smith**
Research focus: Asynchronous circuit design, Formal verification and advanced digital systems.
Dissertation: *Formal Verification Methodology for Asynchronous Sleep Convention Logic (SCL) circuits based on equivalence verification.* Consisted of developing:

- A fast and scalable verification methodology for SCL circuits based on equivalence checking, which ensures both safety and liveness.

**B.Tech. Electronics and Communication Engineering** **August 2009- June 2013**
GPA- **8.95/10**
Inst. Of Engineering & Management (IEM), West Bengal University of Technology (WBUT), Kolkata, WB, India.
Advisor: Dr. Malay Ganguly (Professor, H.O.D, ECE Dept.)
Senior Design Project: *Optimization of the performance of Microstrip Patch Antenna (MPA) using Particle Swarm Optimization (PSO) Algorithm /IE3D*

## RESEARCH EXPERIENCE:

**Graduate Research**, Advanced Digital Design and Verification Lab, NDSU **Aug 2017 – May 2019**

- Conducting research for a project on formal verification of Quasi-Delay Insensitive (QDI) asynchronous circuits **funded** by National Science Foundation (NSF)**.**
- Developed first-ever formal verification methodology for Sleep Convention Logic (SCL) QDI asynchronous Circuits. Developed a verification methodology and verified numerous benchmarks by testing bugs during circuit synthesis. Used Python, SMT-LIB language, Z3 SAT solvers.

**Undergraduate Research Assistant,** Dept. of Electronics & Communication Engineering, IEM, India **2012-2013**

- Worked with the Electromagnetics and Antenna Design group of the dept. of Electronics and Communication Engineering at IEM, Kolkata, India.
- Focused on the optimization of antenna parameters to improve the performance of Microstrip Patch Antennas based on Particle Swarm Optimization (PSO) Algorithm.

## AREAS OF RESEARCH INTEREST:

Asynchronous Logic, High performance Computer Architecture, FPGAs, Low-Power Designs, Reconfigurable and Evolvable Hardware, Digital Design, and Advanced Digital Design.

## PUBLICATION AND PRESENTATIONS:

1. **Refereed Technical Conference: M. Hossain,** A. A. Sakib, S. K. Srinivasan and S. C. Smith, "*An Equivalence Verification Methodology for Asynchronous Sleep Convention Logic Circuits*," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-5.
2. **Invited speaker** for Women in Research, North Dakota State University **March 2019**

## SKILLS:

**Languages:** VHDL, Python, Satisfiability Modulo Theories Library Language (SMT-LIB), Java, C, Assembly.
**Formal Verification:** Equivalence checking, Z3 SMT Solver.
**Application Tools & Software:** Quartus II, ModelSim, MATLAB, Cadence Virtuoso (DRC, LVS), COMSOL.
**Hardware Packages:** FPGA (ALTERA DE2 series), Microcontrollers.

## RELATED MASTER'S COURSEWORK:

Advanced Digital Design, Computer Architecture, Low power Circuits and Systems design, Introduction to Lab-on-a-chip Technology, Introduction to Semiconductor devices, VLSI Design.

## COURSEWORK RELATED PROJECTS:

1. Computer Architecture (ECE 474/774): **Tomasulo's algorithm Simulator** - Developing a simple simulator in C++ to demonstrate Tomasulo's algorithm in a processor capable of performing basic integer arithmetic operations. The processor restraints were pre-specified such as the number of Reservation Stations, number of entries in Register Alias table, computational units, cycles of executions for each arithmetic operation etc.
2. Computer Architecture (ECE 474/774): **Tomasulo's algorithm with Re-Order Buffer implementation –** Extending the previous project to make the processor capable of handling divide by zero exceptions.
3. Advanced Digital Design (ECE 475/773) **NCL 2's Complement MAC** designed in VHDL. Testing it using exhaustive testbench and simulation macro.

## TEACHING EXPERIENCE:

**Teaching Assistant,** North Dakota State University **2017-2019**

- Guiding students on FPGA Architecture and Programming, RTL simulation, Gate-Level Circuit Design, Transistor-Level Circuit Design, and VHDL Coding by using design and simulation tools such as Quartus and ModelSim.
- Updating laboratory assignments and experiments, assisting students in the laboratory, and grading.
- **Courses taught** (SS- Spring Semester, FS- Fall Semester)**:**
  - I. ECE 374 - **Computer Organization**- SS'19, SS'18; Topics covered: R-type/I-type instructions, pipelines, processor design, FPGA implementations, VHDL, Hazards etc.
  - II. ECE 475/773 - **Advanced Digital Design**, SS'19; Topics covered: FPGA implementations, ASM, FSM, Asynchronous Logic, VHDL etc.
  - III. ECE 275 - **Digital Design**- FS'17, FS'18; Topics covered: FPGA implementations, VHDL, Combinational & Sequential circuits, Boolean simplifications, Counters etc.
  - IV. ECE 376 - **Embedded Systems** - SS'18; Topics covered: Assembly programming, stepper motors, interrupts, TIMER interrupts etc.

**Tutor,** IEEE Eta-Kappa-Nu, NDSU **2017-2019**

- Lectured on multiple topics on Computer Organization, Computer Architechture, Digital Design, Advanced Digital Design; organized by the gamma Tau Chapter of IEEE-HKN at NDSU.
- Assisted students with better understand critical concepts, solving example problems to clarify doubts, and providing guidelines for their class projects.

## WORK EXPERIENCE:

**Associate (Programmer), Cognizant Technology Solutions Corporation (CTS)**, India **Dec 2013- May 2017**
**Clients:** (Banking and Financial Services)

- **Fuse box Maintenance App**- The back-office application of a major credit card processor and merchant acquirer in the USA. Provided highly successful deliverables for defects and enhancements.

**Projects:**

1. **Intelligent defaulting system in Online Case Management module- (Role: Module Lead, Programmer):** Implementation of an intelligent defaulting system to auto-populate data satisfying all the complex business rules of the client by a set of defaulting rules set up in the database. This innovation reduced typing effort, time and manual mistakes to a remarkable extent while filling online forms.
2. **GWT Migration project (Role: Programmer)**- Successfully delivered migration of software application from licensed software GXT to open source GWT (Google Web Toolkit). All the components of GXT were custom made into GWT with a plethora of added features.
3. **JBOSS Migration project (Role: Programmer) –** Successfully delivered migration of software application from licensed Tomcat to open-sourced JBOSS application server resulting in cost saving for client. Maven was used as the new build tool for project instead of Apache ANT.

- **First Data**
  **Projects worked on: (Role: Team Member)**
  **Cross Site Request Forgery protection** – Worked on the security of User Admin, Funding and Settlement Management, Rewards website modules based on issues reported by Fortify and Secure Assist tools such as dead codes/SQL injections/Password leaks etc.

## INDUSTRIAL TRAINING:

**Trainee,** Centre for Electronics and Test Engineers (CETE), Ministry of IT, Govt. of West Bengal, India **Dec'12- Jan'13**

- Received training on different microcontrollers and microprocessors, coding in assembly language, and finishing different projects based on microcontrollers.
- Final Project: *An intelligent, real-time Traffic Control System based on Microcontrollers*.

**Trainee,** Circle Telecom Training Centre (CTTC), Bharat Sanchar Nigam Limited, Govt. of India **Dec'11- Jan'12**

- Received training on different telecommunication technologies, fiber-optic communication, information encoding decoding techniques, mobile communications.
- Field study: Live telecommunication equipment deployed at BSNL headquarters, West Bengal Branch.

## COMMUNITY SERVICES

- **Sales Coordinator,** Distressed Children and Infants International (DCI), ND Chapter **2019-Present**
  - Being a part of the leadership group and successfully organizing multiple fundraising events;

- **Volunteer,** Science Olympiad, North Dakota **2018**

## AWARDS AND HONORS:

- Graduate Teaching Assistantship, Dept. of Electrical and Computer Engineering, NDSU (2017-2019).
- West Bengal Board of Secondary Education Scholarship for outstanding result, Govt. of West Bengal, India, 2006.

## PROFESSIONAL AFFILIATIONS:

- **IEEE- Eta Kappa Nu:** Electrical and Computer Engineering Honor Society.
- **Member,** The HONOR Society.
- **Member,** Institute of Electrical and Electronics Engineers (IEEE).