A Tunable Majority Gate based Full Adder using Current-Induced Domain Wall Nanomagnets

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***Abstract*— Domain Wall NanoMagnet (DWNM) based devices have been studied extensively as a promising alternative to conventional CMOS technology in both memory and logic implementations due to their non-volatility, near-zero standby power, and high integration density characteristics. In this paper, we leverage a physics-based model of DWNM device to design a highly scalable current mode majority gate to achieve a novel 1-bit Full-Adder (FA) circuit. The modeled DWNM specifications are calibrated with the experimentally measured data. The functionality of the proposed DWNM based FA (DWNM-FA) is verified using SPICE circuit simulator. Detailed analysis and calculations have been performed to realize the proposed DWNM-FA delay and power consumption corresponding to various induced input currents at different operating temperatures. The Power-Delay Product (PDP) of DWNM-FA is examined to tune the operation within the optimum induced input current region to obtain desired power-delay requirements over a range of 200 µA to 1 mA at temperatures from 298K to 378K. Finally, the comparison results exhibit 52% and 49% area improvement as well as 41% and 31% improvement in device count complexity over CMOS-based and Magnetic Tunnel Junction (MTJ) based FA designs, respectively.**

***Index Terms*— Domain wall nanomagnet, domain wall motion, magnetic majority gate, magnetic full adder, high density logic.**

I. Introduction

Spintronic devices are characterized by non-volatility, near-zero standby power, high integration density, and radiation-hardness, as a technology progression from CMOS [1], [2]. Spintronic devices are capable of performing both Boolean and non-Boolean computation, however, ultra-low voltage current-mode operation of spintronic devices like Domain Wall NanoMagnet (DWNM) can potentially be highly suitable for realizing Boolean representations in future nanocomputing architectures [3]-[5].

In recent years, spintronic devices has been significantly researched to be employed in magnetic Arithmetic Logic Units (ALUs). Since, Binary addition could be considered as the most important operation of an ALU, several researches have been studied on magnetic Full-Adders (FAs) [6]-[11]. In this paper, we propose a new current mode FA design which is based on the DWNM Majority Gates (MGs). The functionality of the proposed circuit is verified using SPICE circuit simulator and detailed simulations and calculations have been achieved to evaluate the performance of the proposed FA under different input currents. It results in a wide tuning range for both induced input current and operating temperature.

The remainder of this paper is organized as follows. In Section II, review and precise model of a DWNM devices are provided. Section III introduces the current mode DW based FA circuit design. Simulation results and detailed analysis are summarized in Section IV including functional and timing analysis. Finally, Section V concludes the paper by highlighting the advantages and features of the proposed architecture.

II. Domain-Wall Nano Magnet Characteristics

Current-Induced magnetic Domain Wall (CIDW) device is a transistor-less element, which leverages a new switching mechanism that has been proposed to overcome low-speed magnetic switching concerns. Each ferromagnetic domain can store a bit while each DW is a mobile interface between regions of oppositely-aligned magnetization, which can be shifted laterally between two antiferromagnetic contacts by applying a current [12] as described below.

A. Fundamental of Domain-Wall Motion

CIDW devices consist of a ferromagnetic nanowire in which opposite magnetic polarities form the Domain Walls (DWs) as

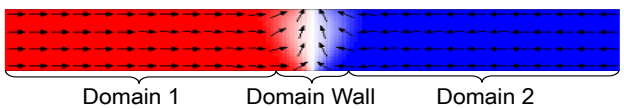

Fig. 1. STT-driven Domain Wall motion.

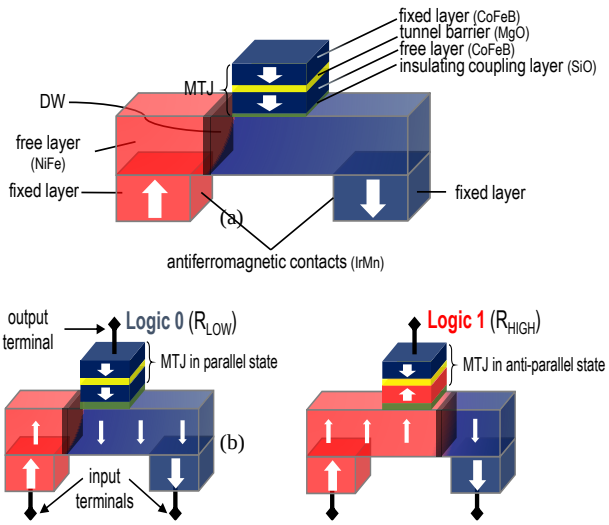

Fig. 2. (a) Schematic illustration of DWNM device, (b) construction of a DWNM logic gate suitable for Boolean logic implementation.

shown in Fig. 1. The DW can be moved within the nanowire according to the Spin Transfer Torque (STT) switching method utilizing an applied spin-polarized current [13]. The applied current only changes the orientation of the spin, thus DWs are not subjected to physical shift. A number of innovative proposals have been developed which use DWs in nanowires to denote the information bits for both memory [14] and logic devices [15]-[17].

Figure 2 shows a DWNM device in which antiferromagnetic contacts are utilized at both its ends and fixed in antiparallel direction relative to each other to ensure the existence of a single DW in the device. To realize writing operation of a single bit, a bidirectional current is used. The bit value of logic "0" is indicated upon shifting the DW to the left, and vice versa for logic "1". For reading operations, a unidirectional current is applied to the Magnetic Tunnel Junction (MTJ) to sense the device state based on the Tunnel Magneto-Resistance (TMR) between MTJ's fixed and free layers [4].

DWNM could be utilized as a logic gate, in which the states of the gate depend on the position of the DW in nanowire and is sensed using MTJ. The output of the gate is obtained based on the parallel (P) or antiparallel (AP) magnetization configuration of the MTJ fixed layer and DWNM nanowire, as shown in Fig. 2(b).

Some recent surveys discussing the feasibility of integrating DWNM with CMOS address the interaction between their circuit design and manufacturing aspects [1], [18-21]. For instance, the DWNM cell and cross-section view of its magnetic layers are shown in Fig. 3, which depicts the DWNM integration at the back-end process of CMOS fabrication. Read and write operations are controlled by the Read/Write Word Lines connected to the gates of the access transistors, which share a common Bit Line. Read access transistor is connected to MTJ that is integrated between the second and third metal layers. The nanowire is built in the third metal layer and controlled by Source Line, Bit Line, and the write access transistor, as shown in Fig. 3(b). Readers may refer to [20] for more details.

B. Domain-Wall Model

As it was mentioned in previous section, STT switching approach is utilized for DW motion. Thus, to model the DW behavior

TABLE I
SIMULATION PARAMETERS OF DWNM AND MTJS

Parameter	Description	Value
	$DW_{Length} \times DW_{Width} \times DW_{Thickness}$	100 nm×10 nm×3 nm
Area	MTJ-1/MTJ-2 Surface	100nm×65nm×π/4
	Reference MTJ Surface	100nm×45nm×π/4
t_{ox}	Thickness of oxide barrier	0.85 nm
α	Gilbert Damping factor	0.01
t_{free}	Thickness of free layer	1.3 nm
μ_B	Bohr Magneton	9.27e-24 $J \cdot T^{-1}$
P	Polarization (DWNM, MTJ)	0.75, 0.5
M_s	Saturation magnetization	8e5 $A \cdot m^{-1}$
I_{C0}	Threshold Current Density	e10—e12 $A \cdot m^{-2}$
R_{AP}, R_P	MTJ-1/MTJ-2 Resistance	2.5 KΩ, 1.25 KΩ
R_P	Reference MTJ Resistance	1.8 KΩ
TMR	TMR ratio	100%
H_k	Out of Plane Anisotropy Field	1600~1800 Oe
K_u	Uniaxial Anisotropy	400e3 J/m^3

Landau-Lifshitz-Gilbert (LLG) must be modified to describe the proper function of the CIDW switching, as indicated in the equations below [22-23]:

$$\frac{\partial \vec{m}}{\partial t} = -\gamma(\vec{m} \times \overrightarrow{H_{eff}}) + \alpha\left(\vec{m} \times \frac{d\vec{m}}{dt}\right) - u(\vec{j}.\nabla)\vec{m} + \quad \beta u\vec{m} \times (\vec{j}.\nabla)\vec{m}, \quad where\ \overrightarrow{H_{eff}} = -\frac{\delta_w}{\mu_0 M_s \delta_m} \tag{1}$$

$$u = \frac{\mu_B JP}{eM_s} \tag{2}$$

where μ_B is the Bohr Magneton, γ is the gyromagnetic ratio, μ_0 is the free space permeability, α is the adiabatic damping coefficient, β is the non-adiabatic spin transfer term, J is the current density, P is the spin polarization, M_s is the saturation magnetization, e is the electron charge, and u is the DW velocity. Equation (3) is the result of solving LLG equation by converting Magnetization vector, $\vec{m}$, and current flow vector, $\vec{j}$, from Cartesian to spherical coordinates [24]:

$$(1+\alpha^2)\vec{\emptyset} = -\frac{\mu_0}{2}\alpha\gamma(H_k \sin 2\emptyset - \pi H_T) + \gamma\left(\mu_0 H_Z - \frac{VX}{M_s d}\right) + \frac{\beta - \alpha}{W}u \tag{3}$$

where $\emptyset$ is the polarization angle, X is the wall position, $V$is the pinning potential, $W$is the domain wall width, and H_k, H_T, and H_Z are anisotropy field, transverse field and longitudinal field, respectively. Herein, DWNM behavior is simulated using a mixed simulation framework, i.e. device simulation and circuit level simulation. First, in device simulation, the OOMMF micromagnetics simulator [25] is leveraged to verify the functionality of our DMNW model, and then a Verilog-A compact model is used to simulate an MTJ cell behavior based on the results extracted from OOMMF. In the first simulation phase, device specifications are calibrated with experimentally measured data reported in [26]. The scatter-plot of data points closely following the linear analytical model shown in Fig. 4 indicates that the model is properly calibrated in terms of domain wall velocity versus input current density. Finally, in the circuit-level simulation, the calibrated model is utilized in SPICE circuit simulation tool to validate the designed circuit functionality using experimental parameters listed in Table I.

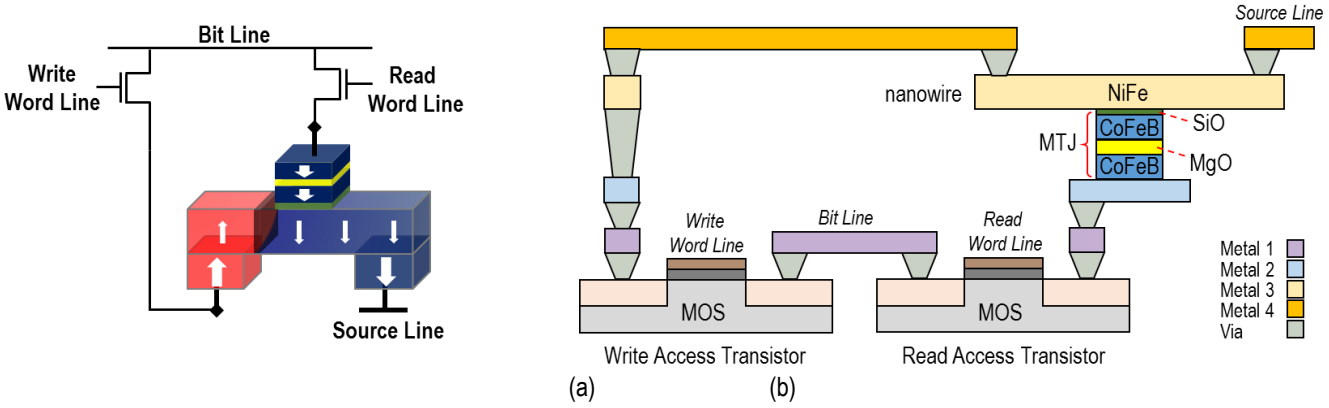

Fig. 3. DWNM (a) cell design, and (b) cross sectional view.

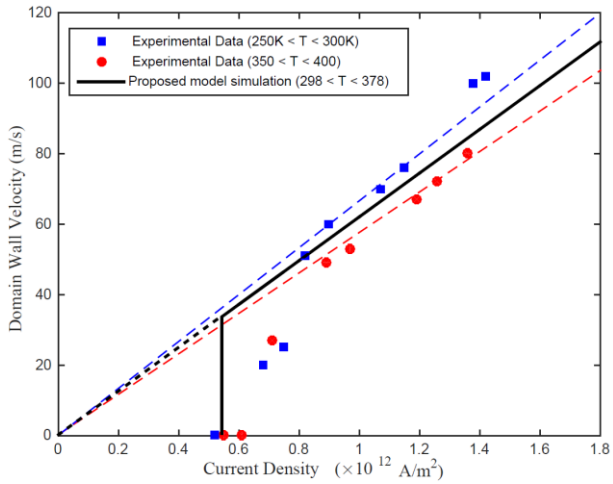

Fig. 4. Domain Wall velocity versus input current density. Red and blue dashed lines express the linear fit to experimental data in different operating temperatures [26].

III. Current Mode Domain-Wall Based Full Adder

In this Section, an innovative 1-bit DWNM based Full-Adder (DWNM-FA) design is proposed using Majority Gate (MG) paradigms which is completely compatible with the current mode behavior of the DWNM.

A. Functionality Analysis

Functionalities of three and five input majority gates are shown in (4). It expresses the output for a MG with *n* inputs, where *n* is always an odd number. The MG outputs "1" if and only if more than $\frac{n-1}{2}$ of the inputs are "1", and vice versa.

$$\begin{aligned} M3 &= Majority\,(A,B,C) = AB + AC + BC \\ M5 &= Majority\,(A,B,C,D,E) \\ &= ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \end{aligned} \tag{4}$$

In addition, a 1-bit full adder Boolean expression is as below:

$$\begin{aligned} C_{OUT} &= A.B + A.C + B.C = M3 \\ SUM &= A.B.C + \bar{A}.\bar{B}.C + \bar{A}.B.\bar{C} + A.\bar{B}.\bar{C} \end{aligned} \tag{5}$$

re-writing (5) according to (4) describes that a 1-bit FA could be implemented using a 3-input MG and a 5-input MG as shown in (6). The terms shown in boldface are inserted to allow expression in M5 function. Thus, while conventional FAs use XOR gates to create the SUM signal, we recognize here the advantage of this alternate formulation which becomes quite amenable to a CIDW realization.

$$\begin{aligned} SUM &= A.B.C + (A+B+C).(\overline{AB}.\overline{AC}.\overline{BC}) \\ &= ABC + (A+B+C)\overline{M3} \\ &= ABC + (A+B+C)\overline{M3} + \mathbf{M3}\overline{\mathbf{M3}} \\ &= ABC + (A+B+C)\overline{M3} + (AB+AC+BC)\overline{M3} \\ &= ABC + (A+B+C)\overline{M3}.\overline{\mathbf{M3}} + (AB+AC+BC)\overline{M3} \quad + (\mathbf{AB}+\mathbf{AC}+\mathbf{BC})\overline{\mathbf{M3}} \\ &= Majority(A,B,C,\overline{M3},\overline{M3}) = M5\,(A,B,C,\overline{C_{OUT}},\overline{C_{OUT}}) \end{aligned} \tag{6}$$

B. Circuit Design

Figure 5 shows the 1-bit DWNM-FA circuit consists of two DWNMs, two Sense Amplifiers (SAs), a CMOS inverter, and a Voltage Controlled Current Source (VCCS) [27]. Functionality of the circuit could be described as follows:

1) The inputs of the proposed circuit are bidirectional currents. Each of the three input currents are injected into the left terminal of M3, while its right terminal is connected to ground (GND), as shown in Fig. 5. The sum of the currents flowing into the left terminal node, according to the conservation of current, results in a left-to-right or right-to-left current flow through the nanowire, which consequently moves the DW to the right or left inside the nanowire-1, respectively, which functions as a three-input MG.

2) Magnetization orientation of the MTJ-1 free layer is changed according to the nanowire-1 magnetic orientation determined by the position of the DW. Herein, pre-charge SAs are leveraged to sense the *P* or *AP* states of the MTJs [28-30]. SA sensing process has two phases called *pre-charge* and *discharge*. First, in the pre-charge phase, both SA branches are charged to V_{DD}. Then, the branches are isolated from V_{DD} and connected to GND in order to start the discharge phase. Each branch will discharge at a different speed based on its resistance. The side with lower resistance discharges faster and eventually outputs a "0" logic level, and vice versa. The reference MTJ resistance is designed in a manner such that its value in parallel configuration is between low resistance *(R_P)* and high resistance *(R_{AP})* of the MTJ cells, i.e. MTJ-1/MTJ-2, to properly sense its state. Reference MTJ cell and MTJ-1/MTJ-2 cell dimensions are listed in Table I. Figure 5 indicates that SA-1 outputs the state of nanowire-1, i.e. C_{OUT}.

3) C_{OUT} voltage is first inverted and then converted to current by means of a VCCS [27] to be employed along with the primary three inputs of the circuit as inputs of the 5-input MG, which is built by nanowire-2 as depicted in Fig. 5.

4) SA-2 outputs the state of the nanowire-2 which is the output of the FA circuit, at the terminal labeled *SUM*.

In the proposed circuit, we assumed logic “1” is equal to +800µA and logic “0” is -800µA. This assumption is compatible with the required current mode operation, since the sum of the input currents produces a bidirectional induced current which drives the DW to the left or right side of the nanowire based on the current direction. It also significantly reduces the routing

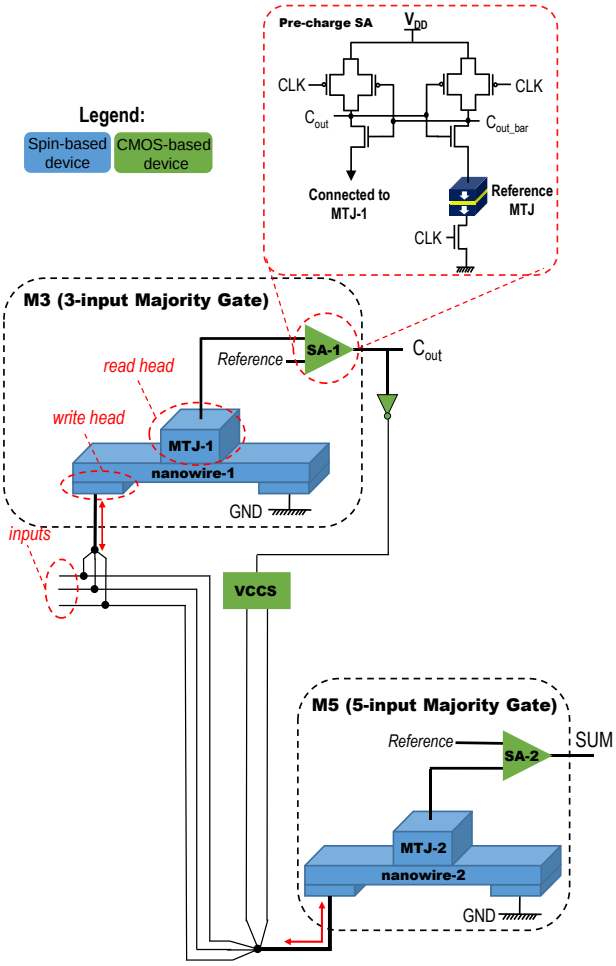

Fig. 5. Schematic of DWNM based Full-Adder Circuit. The main structure is comprised two DWNMs and two SAs, which operate as the functional building blocks and the decision-making elements, respectively.

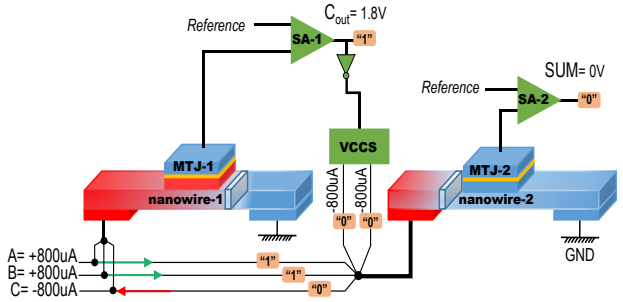

Fig. 6. Example of the proposed DW based Full-Adder function for ABC= “110” input. The sum of the input current moves the DW in nanowire-1 which denotes Cout=“1”. Meanwhile, the majority of the applied currents into the nanowire-2 cannot unpin to move its DW because it does not exceed the threshold value, so SUM=“0”.

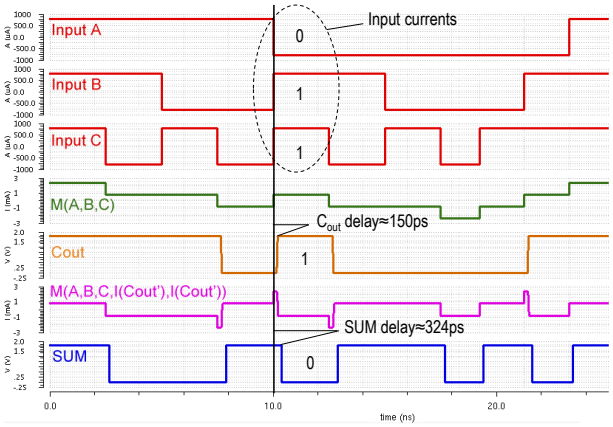

Fig. 7. Simulation results of 1-bit DWNM based FA. Logic 0/1 levels of inputs (A, B, and C) correspond to applied currents of -800µA and +800µA whereas bits 0 and 1 for outputs, Cout and SUM, correspond to voltage of 0V and 1.8V. For instance, input current pulses ABC=011 nucleate the DW in nanowire-1, Cout=1, and cannot unpin the DW in nanowire-2, SUM=0.

complexity and peripheral circuits realizing the logic level corresponding to the position of the DW inside the nanowire. Figure 6 elaborates the functionality of the proposed DWNM-FA via an example for *A*= "1", *B*= "1", and *C*= "0" inputs.

IV. Results and Analysis

A. DWNM-FA Functionality

In order to verify the functionality of our proposed circuit, SPICE circuit simulator with parameters mentioned in Table I is utilized. The simulation includes the threshold current density which is required to unpin DW from its fixed position near the antiferromagnetic contacts. However, the stochastic behavior of the DWM device which is affected by the thermal fluctuations and edge roughness are not embraced. The 1-bit DWNM-FA simulation results along with the input and output waveforms are shown in Fig. 7. All transitions matched the desired behavior while considering the propagation delays.

B. DWNM-FA Delay Analysis

Delay of the proposed Full-Adder circuit, t_{Cout} and t_{SUM}, is calculated using (7):

$$\begin{aligned} t_{Cout} &= t_{nanowire1} + t_{SA1} \\ t_{SUM} &= t_{Cout} + t_{inv-vccs} + t_{nanowire2} + t_{SA2} \end{aligned} \tag{7}$$

where $t_{nonowire1}$, $t_{nonowire2}$, t_{SA1}, and t_{SA2} are the nanowire-1, nanowire-2, SA-1, and SA-2 delays, respectively, and $t_{inv-vccs}$ is the delay of the inverter and VCCS together. Herein, $t_{nonowire1}$ and $t_{nonowire2}$ values are calculated using (8) and parameters mentioned in Table I as given by:

$$t_{nanowire} = DW_{Length}/u \tag{8}$$

where u is the DW velocity which could be calculated using (2), and DW_{Length} is the length of the nanowire which is equal to 100nm in our design.

Nanowire delay is different for each set of inputs, due to the difference in input current. Table II provides the values for the nanowire-1 and nanowire-2 delays for each set of inputs. As listed in the Table, the average delay of nanowire-1 is roughly 85.8ps which is five sixth of a nanowire switching delay with single input current. Using a similar approach for calculating the delay of the nanowire-2 results in an average delay of 103ps which is equal to the delay of a single input nanowire. Moreover, $t_{inv-vccs}$, t_{SA1}, and t_{SA2} are extracted using SPICE simulation in the 90nm technology library available, and are equal to 23ps, 47ps, and 47ps, respectively.

Substituting (8) according to (2) implies that the nanowire delay has inverse relation with the input current, as described in (9), where I is the input current.

$$\begin{aligned} t_{nanowire} &= \frac{DW_{Length} \times eM_s}{\mu_B JP} \\ &= \frac{DW_{Length} \times eM_s \times DW_{Width} \times DW_{Thickness}}{\mu_B PI} \end{aligned} \tag{9}$$

Equations 10 and 11 indicate that the FA circuit average delay, as calculated by (7) and (9) using the values obtained through SPICE simulation. The relation between the average delays of a DWNM-FA circuit and input current is depicted in Fig. 8.

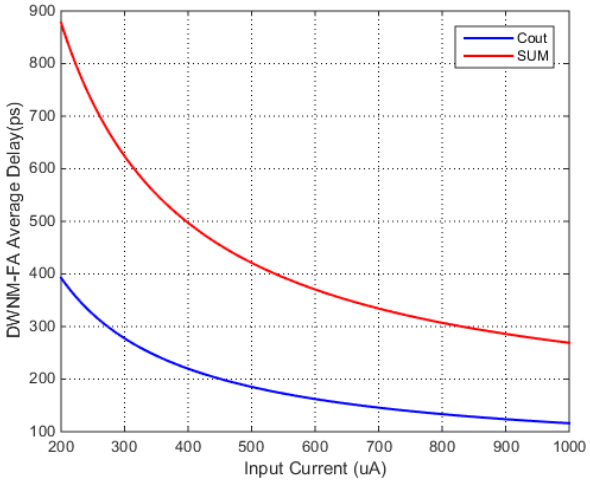

Fig. 8. Dependence of DWNM-FA Average Delay on Input Current are depicted for circuit outputs C_{out} and SUM.

TABLE II
NANOWIRE-1(FOR C_{OUT}) AND NANOWIRE-2 (FOR SUM) SWITCHING DELAYS.

$A\ (\mu A)$	$B\ (\mu A)$	$C\ (\mu A)$	$\sum inputs$	$C_{out}\ (V)$	$I(\overline{C_{out}})\ (\mu A)$	nanowire-1 delay (ps)	$\sum inputs + 2 \times I(\overline{C_{out}})$	$SUM\ (V)$	nanowire-2 delay (ps)
-800	-800	-800	-2.4 mA	0	+800	34.34	-800	0	103
-800	-800	+800	-800 μA	0	+800	103	+800	1.8	103
-800	+800	-800	-800 μA	0	+800	103	+800	1.8	103
-800	+800	+800	+800 μA	1.8	-800	103	-800	0	103
+800	-800	-800	-800 μA	0	+800	103	+800	1.8	103
+800	-800	+800	+800 μA	1.8	-800	103	-800	0	103
+800	+800	-800	+800 μA	1.8	-800	103	-800	0	103
+800	+800	+800	+2.4 mA	1.8	-800	34.34	+800	1.8	103
						Average ≈ 85.8			Average = 103

$$t_{Avg-Cout} = t_{Avg-\,nanowire1} + t_{SA1} = \left(\frac{5}{6}\right) t_{nanowire} + 47\ (ps) \tag{10}$$

$$t_{Avg-SUM} = t_{Avg-Cout} + t_{inv-vccs} + t_{nanowire2} + t_{SA2} = \left(\frac{11}{6}\right) t_{nanowire} + 117\ (ps) \tag{11}$$

FA operation speed could be directly controlled by the value of the input currents, which could result in a high speed arithmetic unit. However, this approach may not necessarily be power efficient.

C. DWNM-FA Power Analysis

As mentioned in previous sections, DWNM-FA circuit comprises two DWNMs, two SAs, a CMOS inverter, and a VCCS. Hence, average power consumption of the proposed circuit, $P_{DWNM\text{-}FA}$, could be extracted using (12).

$$P_{DWNM-FA} = P_{Avg-\,nanowire1} + P_{Avg-\,nanowire2} + 2 \times P_{SA} + P_{inv-vccs} \tag{12}$$

Herein, the demonstrated nanowire consumed power, $P_{nanowire}$, is expressed as below [31]:

$$P_{nanowire}(I,T) = R_0\left(1 + \theta(T - T_0)\right) \times I^2 \qquad where, R_0 = \frac{\rho \times DW_{Length}}{DW_{Width} \times DW_{Thicknes}} \tag{13}$$

where, T_0 is room temperature, i.e. 298 K, R_0 is the resistance at T_0, temperature coefficient θ is considered +3e-3 K^{-1} at T_0, and ρ is the nanowire resistivity, which is considered 100 Ω·nm.

In a manner similar to that used to obtain the results listed in Table II, the power consumption also varies based on different sets of inputs. Thus, a similar approach is employed for computing the average nanowire power consumption. At room temperature, the average power consumption obtained is $P_{avg\text{-}nanowire1} = 3P_{nanowire} = 640\ \mu W$ and $P_{avg\text{-}nanowire2} = P_{nanowire} = 213.33\ \mu W$. Furthermore, SA average power consumption, P_{SA}, and inverter and VCCS average power consumption, $P_{inv\text{-}vccs}$, are obtained respectively to be 13.6646 µW and 4.4277 µW by SPICE simulation in 90nm technology in the circuit delay time window. Finally, the relation between proposed DWNM-FA average power consumption, and input currents along with temperature is extracted using (12) in conjunction with the values gained by SPICE simulation. Figure 9 exhibits a quadratic and linear growth for power consumption relative to the input current and temperature, respectively.

Finally, the Power-Delay Product (PDP) of the proposed DWNM-FA according to different values for input current and temperature are extracted utilizing 1.8V nominal voltage (V_{DD}) and 1 GHz circuit clock (CLK) frequency, as shown in Fig. 10. Result illustrates a quadratic growth for PDP corresponding to the input current. As a result, based on the operating temperature of the proposed circuit and desired Power-Delay values, optimum input current could be extracted from Fig. 9 and Fig. 10. Both iso-power and temperature constrained operating points can be readily obtained by the above mentioned surface plots.

D. Results and Comparison with Previous Works

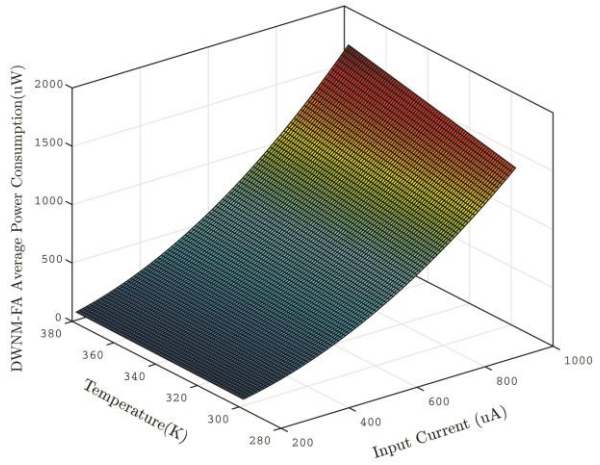

Fig. 9. Power Consumption of DWNM-FA versus temperature and applied current.

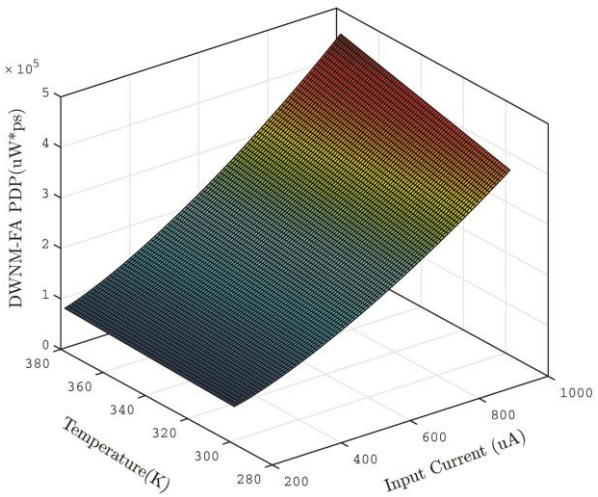

Fig. 10. PDP of DWNM-FA versus temperature and applied current.

Our designed tunable majority gate based FA can function in two different modes. *1) Low Power Mode (LPM)*: the lowest current magnitude is injected, e.g. 200µA, as the input current, resulting in a low power and low speed operation of the FA circuit. *2) High Speed Mode (HSM)*: the highest magnitude current is injected as an input, e.g. 1 mA, so that the HSM FA design functions rapidly but with high power consumption. Comparison results with previous CMOS and MTJ based FAs fabricated using 180 nm CMOS process are summarized in Table III. It shows that our design has a significant improvement in terms of area and complexity, i.e. device count. Moreover, MTJs are 2-terminal devices which share a common path for reading and writing operations that results in major reliability issues in MTJ-based designs [32-33]. Whereas the DWNM employed in our design is a 3-terminal device enabling separate read and write paths that significantly reduce the disturbances induced by using a common path.

TABLE III
COMPARISON OF 1-BIT FULL ADDERS

Parameter \ Design	CMOS [6]*	MTJ-based [6]	LPM (*herein*)	HSM (*herein*)
Delay	224 ps	219 ps	877 ps	269 ps
Dynamic Power (@1 GHz)	143 µW	33 µW	85 µW	1364 µW
Static Power	0.9 nW	0.0 nW	0.0 nW	0.0 nW
Area	333 μm^2	315 μm^2	160 μm^2	
Complexity	42 MOSs	34 MOSs + 4 MTJs	20 MOSs + 4 MTJs + 2 nanowires	

* Full Adders are fabricated using 180 nm CMOS process

V. CONCLUSION

In this paper, we developed a novel, compact, and highly-scalable current mode 1-bit DWNM-FA. The DWNM behavior modeled and its specifications were calibrated with the experimentally extracted data. The DWNM and MTJ characteristics simulated in Verilog-A based on precise physical equations which showed favorable tunability over typical operating range. Functionality of the proposed circuit was verified using SPICE circuit simulators; tightly integrated consideration of analytical formulations and simulation results facilitated deeper insights into DW interactions. Furthermore, the detailed analysis and calculations illustrated the power-based relationships of the DWNM-FA despite different induced input currents at various operating temperatures. Comparison results with previously proposed CMOS-based and MTJ-based FAs show benefits in terms of area and complexity. Future works includes leveraging the unique characteristics of the proposed circuit to design an ALU with high performance and scalability, and low power consumption and complexity.

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