Design Space Issues for Intrinsic Evolvable Hardware

James Hereford
Murray State University
Murray, KY 42071
James.Hereford@murraystate.edu

David Gwaltney
NASA-Marshall Space Flight Center
Huntsville, AL 35812
avid.A.Gwaltney@nasa.gov

Abstract

This paper discusses the problem of increased programming time for intrinsic evolvable hardware (EHW) as the complexity of the circuit grows. We develop equations for the size of the population, *n*, and the number of generations required for the population to converge, *ngen*, based on L, the length of the programming string. We show that the processing time of the computer becomes negligible for intrinsic EHW since the selection/crossover/mutation steps are only done once per generation, suggesting there is room for use of more complex evolutionary algorithms in intrinsic EHW. Finally, we review the state of the practice and discuss the notion of a system design approach for intrinsic EHW.

References:

[1] J. Lohn, G. Larchev, R. F. DeMara, "Evolutionary Fault Recovery in a Virtex FPGA Using a Representation that Incorporates Routing", International Parallel and Distributed Processing Symposium (IPDPS'03), April 22 - 26, 2003.