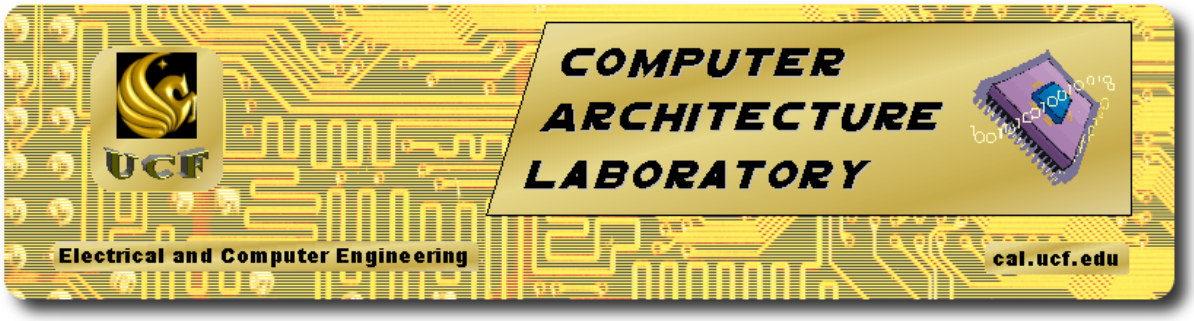

Reactive Rejuvenation of CMOS Logic Paths using Self-Activating Voltage Domains

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Reactive Rejuvenation of Voltage Domains for Anti-aging

Reactive Rejuvenation (RR):

- a *post-fabrication self-adapting* circuit-level approach to mitigate timing degradations.

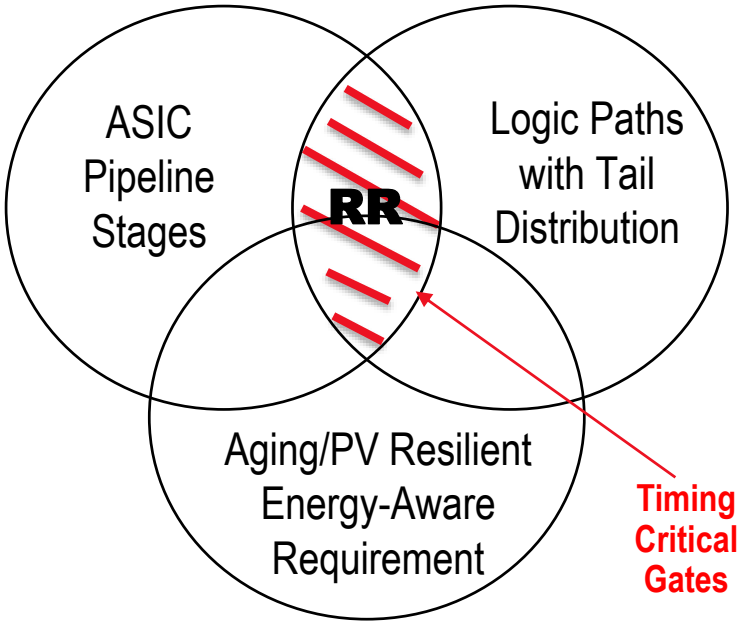
Research Objective:

- Mitigate *Transistor Aging* due to BTI and HCI thus reducing the energy wastage due to conservative selection of guardbands.

Targeting Aging-critical Elements:

- aging-critical logic portions of the circuit are targeted for protection → minimal overhead
- power-gating is effective in reducing BTI and HCI. Switching activity (p) effects the shift in V_{th}

$$\Delta V_{th}(t) \propto (pt)^n$$



Research Needs

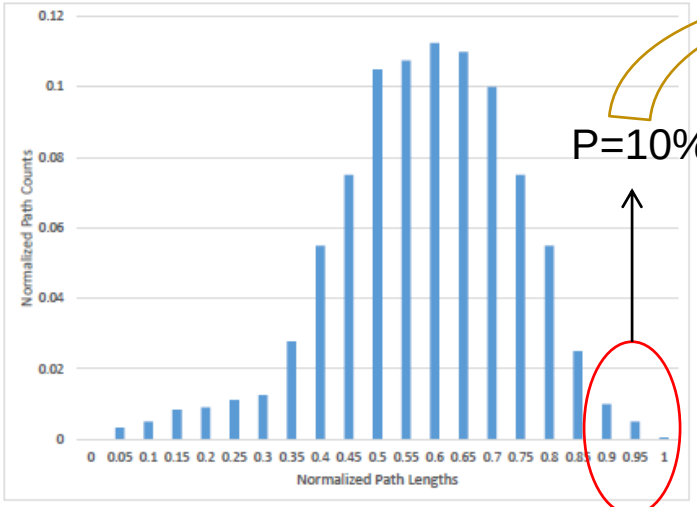
Need addressed	Approach	Benefit
Transistor Aging	Power-gating of critical elements	Reduced lifetime delay degradation through stress reduction
	In-situ timing assessment and autonomous control of Sleep Interval	Avoids the need for complicated modeling of aging degradation at design-time
Energy Consumption	Reduced voltage guardbands	Low energy requirement with narrower margins for longer periods
	De-emphasized role of voltage regulators	Circumvent conversion inefficiencies and switching losses
	Selective Redundancy	Power-gating lowers the leakage energy overheads

Related Works

Technique	Anti-Aging Strategy	Design Requirements/ Parameters	Adaptability Characteristics/ Degree	Overheads		
				Throughput	Power	Area
			Worst-case Design			
VM, FM	Static Margin	MD-RoD/ ΔV_{DD}, $\Delta F_{nominal}$	None	FM: High	VM: High (Dynamic & Leakage)	None
Gate-Sizing	Static Margin	MD-RoD; Extended Std. Lib.; Multi-obj. Opt./ $\Delta\beta_i, \forall$ gates i	None	None	Medium (Dynamic & Leakage)	Low (Gate-level)
Re-Synthesis	Static Margin	MD-RoD annotated Std. Lib.; Aging-aware Synthesis/ $\Delta\beta_i$, $\Delta V_{th,i} \forall$ gates i	None	None	Low-Medium (Dynamic & Leakage)	Low (Gate-level)
			Dynamic Operating Conditions			
DVFS	Dynamic Margin	Timing Sensors; Feedback Control/ $\Delta V_{DD}(t)$, $\Delta F(t)$, $\Delta V_{bb}(t)$	Yes/ Fully Autonomous	Low	Medium (Dynamic & Leakage)	Medium (On-chip VR & sensors)
SVS	Dynamic Margin	MD-RoD/ $\Delta V_{DD}(t + \Delta t_{step})$	Yes/ t_{step}	None	Medium (Dynamic & Leakage)	Medium (On-chip VR)
GNOMO	Static Margin + Power-Gating	MD-RoD/ $(V_{DD,g}, t_{idle})$	None	Medium (Workload Dependent)	Medium (Dynamic & Leakage)	None
			Adaptive Resource Management			
SD	Proactive Mngt. + Power-Gating	Modular Redundancy/ Sleep Interval	Yes / Sleep Interval	None	High (Leakage)	High (Module-level)
ITL schemes	Proactive Mngt. + Power-Gating	Exploit App. Redundancy/ Idle time	Yes / Task Scheduling	Medium (Workload Dependent)	None	None
Proposed herein						
RR	*Reactive Fine-Grain Mngt. + Power-Gating*	*Timing Sensors; Feedback Control; CPRT/ ERT%*	*Yes/ Fully Autonomous*	*None*	*Minimal (Leakage)*	*Low (Gate-level & sensors)*

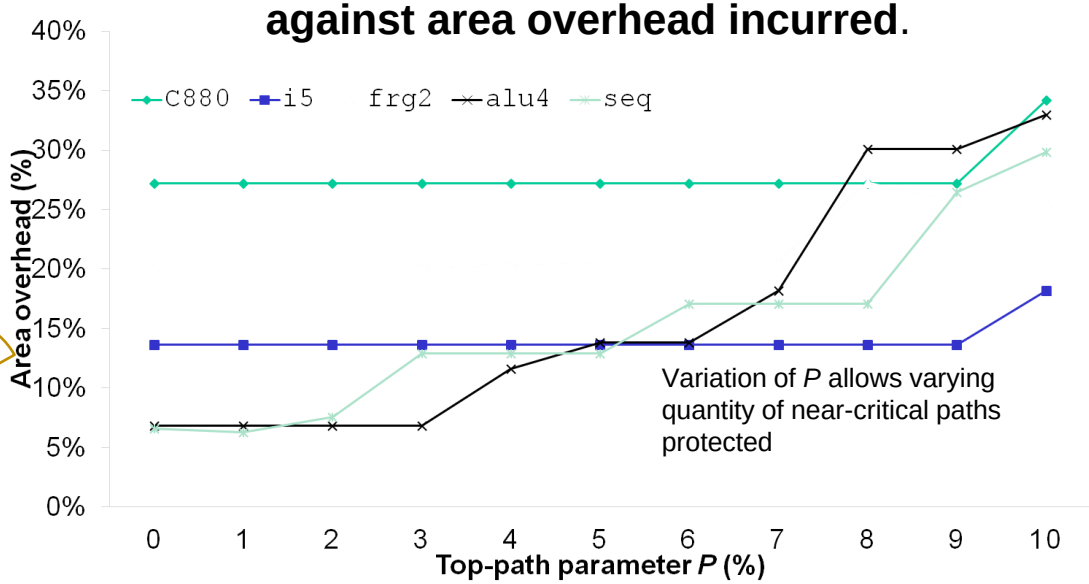
Aging-Sensitive Logic Domains

1) Path distribution of OpenSPARC ALU



[G. Hoang et al."Exploring circuit timing-aware language and compilation," *SIGPLAN Not.,* vol. 47, no. 4, pp. 345–356, Mar. 2011.]

2) Parameter *P* can be traded-off against area overhead incurred.

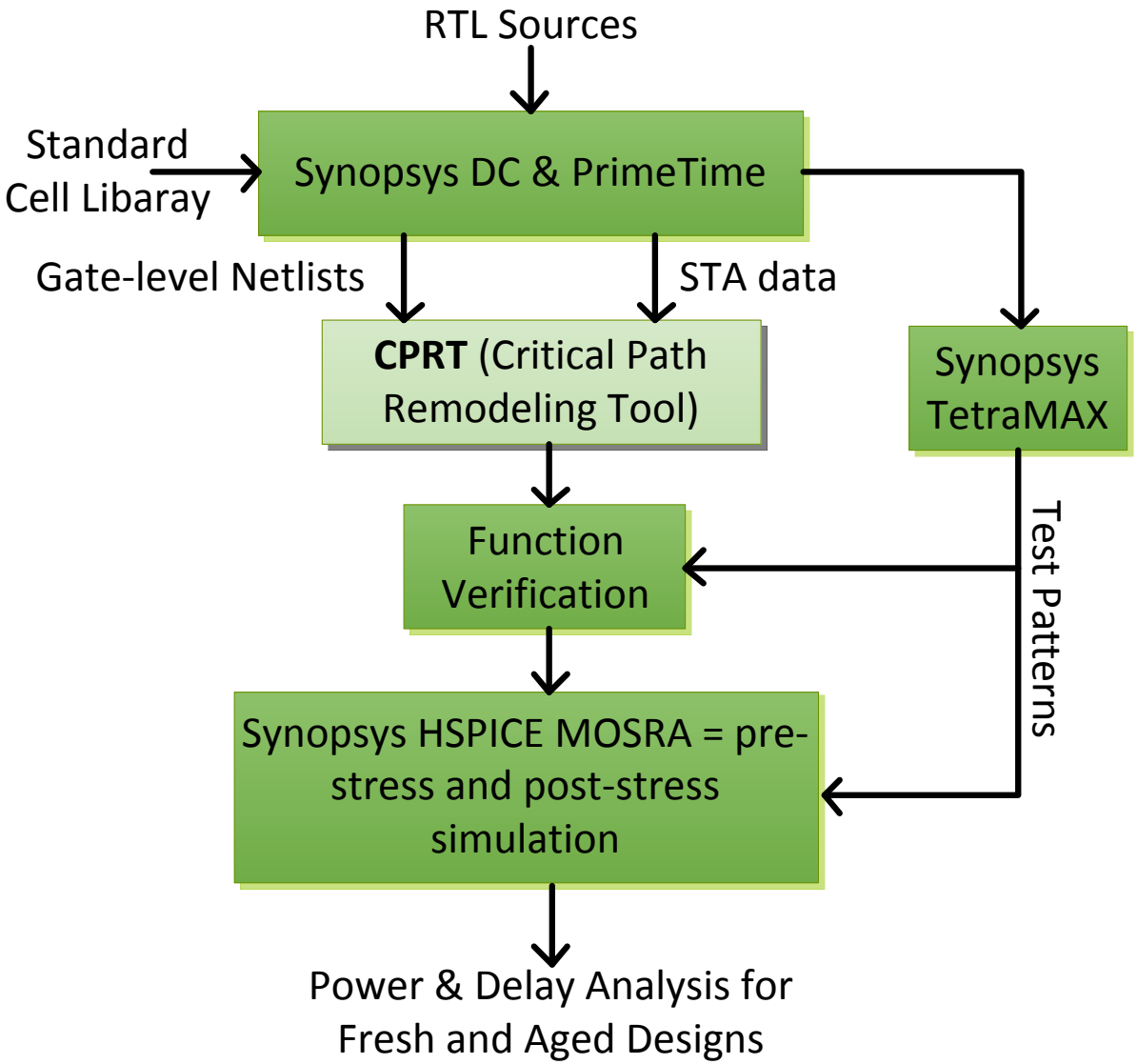


3) RR covers logic paths having delays:

$$[D_{critical}(t) * (100\% - P), D_{critical}(t)]$$

- P is top-path parameter
- based on near critical paths due to aging and/or PV effects
- *P=10%* used herein

Critical Path Remodeling Tool (CPRT)



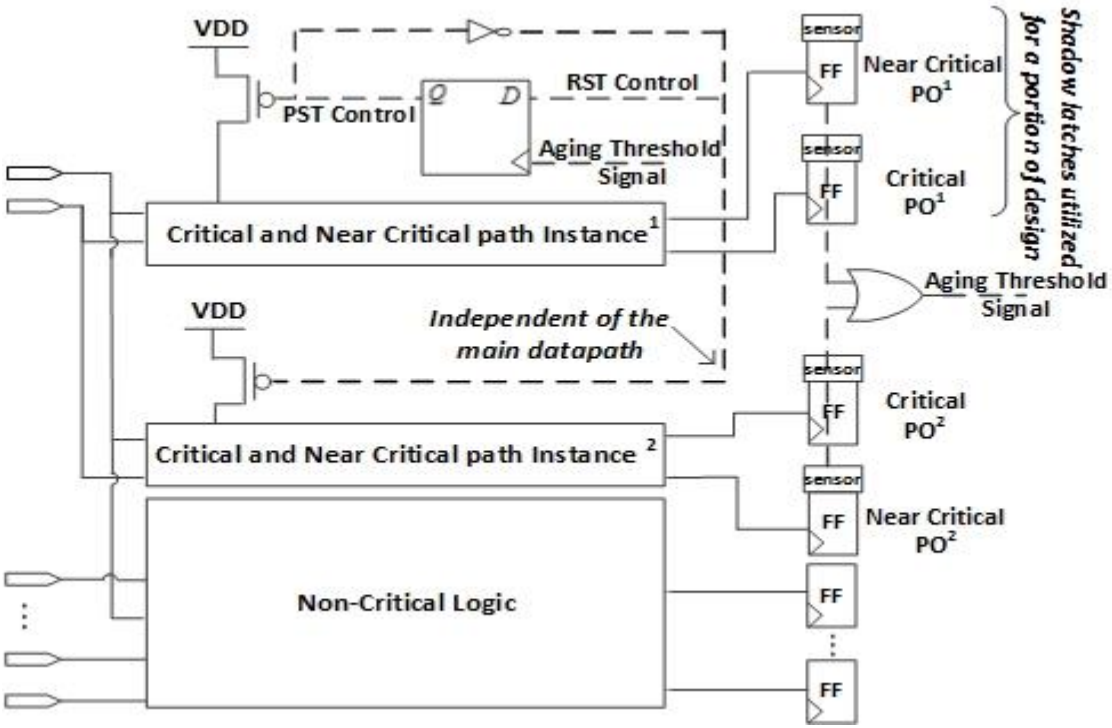
Autonomous Operation via RR

Need for circuit-level feedback:

- Determination of *sleep interval* at design-time is based on assumptions and may mismatch actual circuit aging.

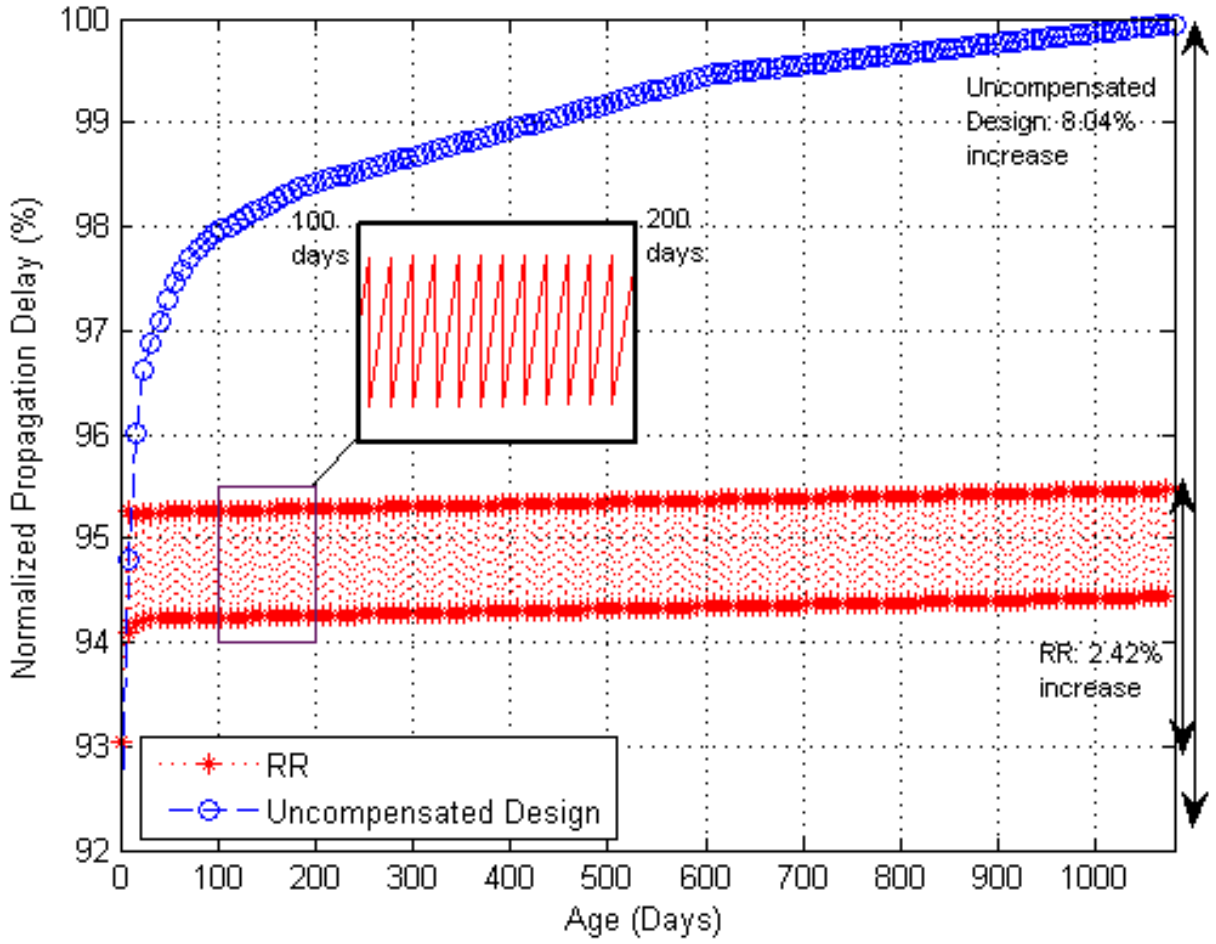
Reactive Rejuvenation (RR):

- Fully autonomous reliable operation with optimal switching interval and minimal design effort.



RR Reduction of Delay Degradation c880

- NanGate Library based on 45nm Predictive Technology Model is used
- Built-in models for BTI and HCI are utilized for HSPICE simulations



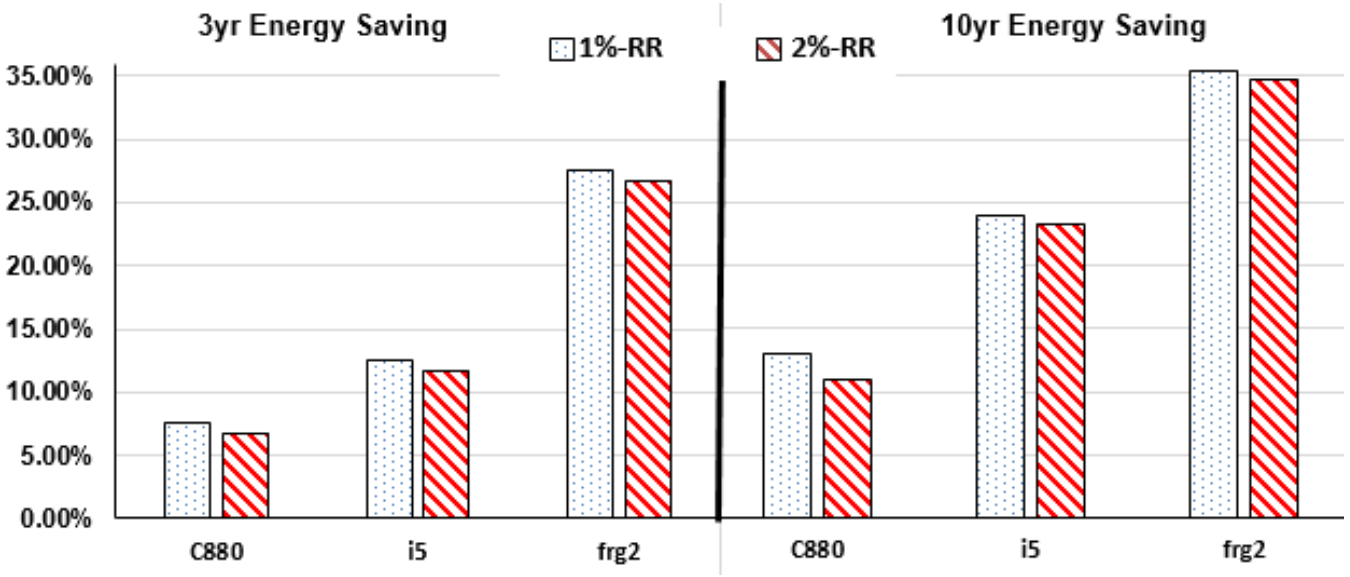
Implications of Tighter Timing Specifications

Elastic Recovery Threshold:

- at design-time, supply voltage is set such that delay of circuit is **ERT**% below desired timing specification. ERT=1% and 2% used.

Reduced guardbands:

- enables energy savings as high as 35.3% and 34.6% for frg2 with ERT of 1% and 2% respectively over 10 years.



Area Overhead w.r.t. Related Works

Case-study:

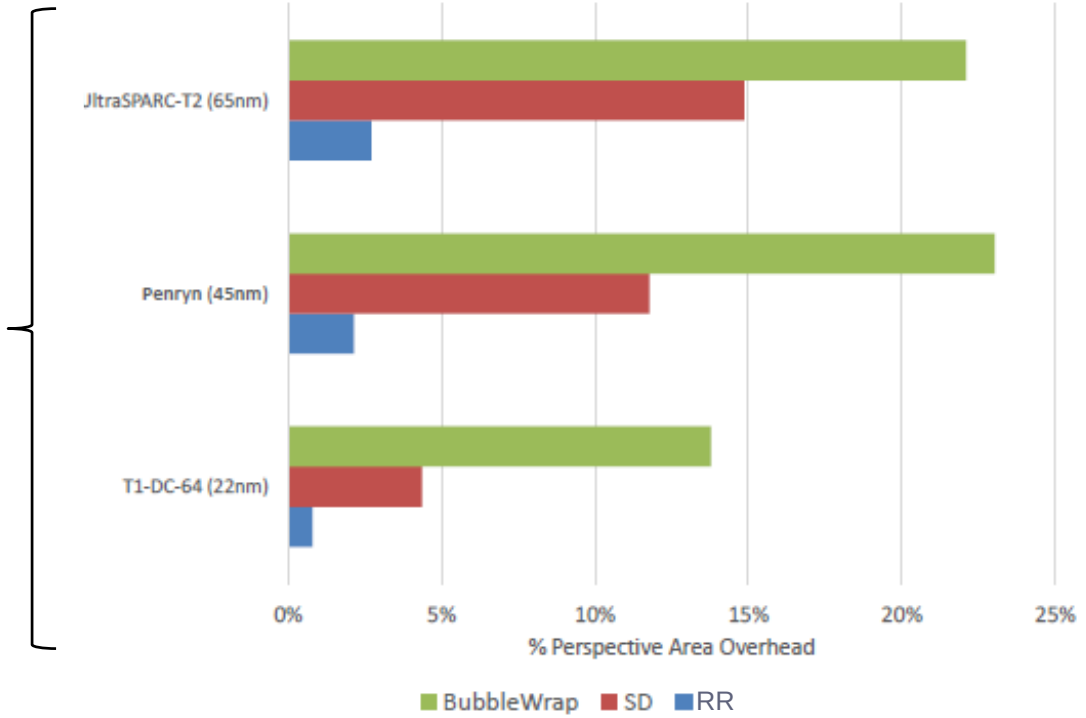
- 45nm-based Intel Penryn multicore processor.
- Core-area of 46.1%, Uncore-area composed of caches, NoC, etc.

Execution unit:

- 39%, of which 65.5% is occupied by arithmetic units

  → aging-critical portion = 11% of die

- **For BubbleWrap:** half of the cores are designated as *expandable*
- **For SD:** aging-sensitive logic is replicated
- Utilized ALU area overhead with *N=2, P=7%*



Conclusions

Summary of Approach

- RR provides an **adaptive** technique for anti-aging using a **spatial redundancy** and **power-gating** to enable BTI recovery
- **Accurate aging modeling → unnecessary**
  as circuit degradation is determined using operational conditions
- **Intrinsic runtime competition** among logic domains in the presence of process, voltage and temperature variations
- Favorable energy savings as high as 35.3% using RR are obtained due to reduction of operating voltage through **autonomous adaptation** of switching interval