Port prioritization scheme

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Abstract

An apparatus comprising a first compare circuit, a second compare circuit and a memory. The first compare circuit may be configured to present a first match signal in response to a first address and a second address. The second compare circuit may be configured to present a second match signal in response to the first match signal, a first write enable signal and a second write enable signal. The memory may also be configured to present the first and second write enable signals. In one example, the memory may be configured to store and retrieve data with zero waiting cycles in response to the second match signal.

References

[1] Alves et al., "Built-In Self-Test for Multi-port RAMs", 1991, IEEE, p. 248-251.

[2] S. E. Crawford, and R. F. DeMara, Cache coherence in a multiport memory environment. *In Massively Parallel Computing Systems*, 1994., Proceedings of the First International Conference on, pp. 632-642. IEEE, 1994.