Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching

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Abstract

Magnetic tunnel junction (MTJ) based devices have been studied extensively as a promising candidate to implement hybrid energy-efficient computing circuits due to their non-volatility, high integration density and CMOS compatibility. In this paper, MTJs are leveraged to develop a novel full adder (FA) based on 3- and 5- input majority gates (MGs). Spin Hall Effect (SHE) is utilized for changing the MTJ states resulting in low-energy switching behavior. SHE-MTJ devices are modeled in Verilog-A using precise physical equations. SPICE circuit simulator is used to validate the functionality of 1-bit SHE-based FA. The simulation results show 76% and 32% improvement over previous voltage-mode MTJ-based FA in terms of energy consumption and device count, respectively. The concatanatability of our proposed 1-bit SHE-FA is investigated through developing a 4-bit SHE-FA. Finally, delay and power consumption of an n-bit SHE-based adder has been formulated to provide a basis for developing an energy efficient SHE-based *n*-bit arithmetic logic unit (ALU).

Index Terms

full adder, magnetic tunnel junction (MTJ), spin-Hall Effect (SHE), spin-transfer torque (STT).

I. Introduction

SCALING MOS technology increases leakage power which can compromise a significant part of the total power consumption in systems-on-chip designs [1]. The MOS scaling challenges has resulted in considerable research on emerging technologies. Spintronic devices such as magnetic tunnel junctions (MTJs) are one of the promising alternatives for MOS due to their non-volatility, near-zero standby power, high integration density, and radiation-hardness features [2-3]. Moreover, MTJ can be vertically integrated at the back-end process of CMOS fabrication. Thus, in a hybrid MTJ/MOS design, the distance between logic elements and memory building blocks can be reduced, resulting in lower standby power and area overhead. Hence, spin-based devices have been extensively studied in both memory [4-5] and logic units [6-7] in recent years. In most of the previous developed spin-based building blocks, spin-transfer torque (STT) [8] switching approach is exploited. Although STT offers several advantages in read operation, it suffers from high switching power and delay. Recently, spin-Hall effect (SHE)-based switching approach [9] is introduced to address the mentioned STT-related concerns. A three-terminal SHE-based MTJ (SHE-MTJ) offers improved reliability, higher switching speed and lower write energy operation compared with a conventional two-terminal STT-based MTJ (STT-MTJ) [10-11]. In this work, we look to exploiting the mentioned advantages of the SHE-MTJ devices to develop a low-power and non-volatile 1-bit full adder (FA).

Binary addition is one of the most fundamental operations in arithmetic logic units (ALUs), therefore FA plays a significant role in an ALU structure. In this paper, we have designed a non-volatile FA using SHE-MTJ devices. Our proposed FA is composed of 23 MOS transistors and three SHE-MTJs. Two of the SHE-MTJs function as majority gates (MGs), and the other one is utilized as a reference element to sense the output of the FA. The switching behavior and functionality of the proposed circuit is verified using SPICE circuit simulator. Detailed simulation results and calculations have been provided to evaluate the performance of the proposed FA.

The remainder of this paper is organized as follows. In Section II, review and precise model of a STT-MTJ and SHE-MTJ devices are provided along with the functionality of MG-based FA. Section III introduces the SHE-based FA circuit design. Simulation results and detailed analysis are summarized in Section IV including functional and timing analysis. Finally, Section V concludes the paper by highlighting the advantages and features of the proposed architecture.

II. Review of MTJ and FA

A. Magnetic Tunnel Junction (MTJ)

An MTJ is composed of a thin oxide barrier placed between two ferromagnetic layers, free layer (FL) and pinned layer (PL), as shown in Fig. 1(a). Due to the difference in coercivity, polarization state of FL can readily change, meanwhile PL magnetization is fixed. Hence, there are two stable configurations, parallel (P), i.e. low resistance state, and anti-parallel (AP), i.e. high resistance state. P and AP states denote “0” and “1” in binary information, respectively. STT is one of the most prevalent switching approaches for MTJs, due to its simplicity [8]. In STT switching approach, a bidirectional current passes through an MTJ according to which it can be configured into P or AP state. Although STT offers the aforementioned advantages, it suffers from some challenges such as high

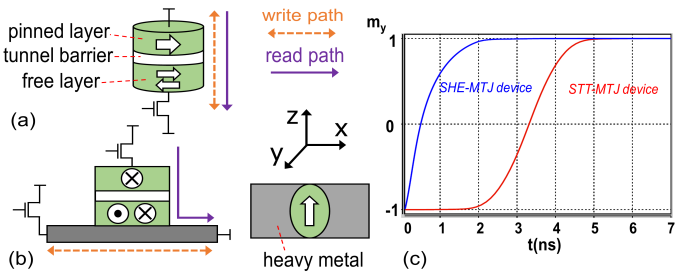

Fig. 1: (a) two-terminal In-plane MTJ structure [23], (b) three-terminal SHE-MTJ, vertical and top view (left and right, respectively), and (c) magnetization switching time for SHE- and STT- MTJs [14].

write current, and switching asymmetry [12]. Moreover, STT-MTJ is a two-terminal device with a shared write and read path. Consequently, undesirable switching may occur during the read operation, and stored data can be flipped accidentally. Recently, 3-terminal MTJ (SHE-MTJ) has been researched as a potential alternative offering some benefits such as decoupled read and write paths, as well as energy-efficient and high-speed write [6].

A SHE-MTJ structure includes an MTJ that its FL is directly connected to a heavy metal (HM). The HMs can be made of β-tantalum (β-Ta) [9], β-tungsten (β-W) [10] or Pt [11]. In this paper, we have utilized the tungsten characteristics to model our device, due to its high positive spin Hall angle [13]. The magnetization direction of the FL can be oriented according to the direction of an applied charge current that flows through HM. If a charge current is injected to HM in +x (or -x) direction, a spin current will be generated in +y (or -y) direction, which exerts STT on FL and results in P to AP (or AP to P) switching. Figure 1(b) shows a SHE-MTJ structure with separated read and write paths.

Spin Hall injection efficiency (SHIE) value, which is the ratio of the produced spin current to the applied charge current is expressed by equation 1 [13]. In this paper, SHIE value is always greater than unity, which can be extracted using Equation (1) and the parameters mentioned in Table I. While, the spin injection efficiency of a conventional STT-MTJ is normally less than one, which results in an increased switching energy for STT-MTJ devices.

$$SHIE = \frac{I_{sz}}{I_{cx}} = \frac{\pi . MTJ_{width}}{4HM_{thick}} \theta_{SHE}[1 - sec(\frac{HM_{thick}}{\lambda_{sf}})] \tag{1}$$

where MTJ_{width} is the width of the MTJ, HM_{thick} is the thickness of the HM, λ_{sf} is the spin flip length in HM, and θ_{SHE} is the SHE angle. This equation is valid for SHE-MTJ devices in which length of the MTJ equals the width of the HM. The critical spin current for switching the free layer magnetization orientation is expressed by Equation (2) [13]:

$$I_{S,critical} = 2q\alpha M_S V_{MTJ}(H_k + 2\pi M_s)\overline{h} \tag{2}$$

where V_{MTJ} is the MTJ free layer volume. Thus, SHE-MTJ critical charge current can be calculated using Equations (1) and (2). To exhibit the transient response of the SHE-MTJ and STT-MTJ devices, we have utilized a model developed by Camsari et al. in [14]. Figure 1(c) shows the transient switching behavior of STT-MTJ and SHE-MTJ devices, in which the applied write current equals 150 μA. The SHE-MTJ switching delay is approximately 2ns, which is smaller than that of the STT-MTJ, $\approx$ 5ns.

B. Full Adder (FA) Functionality

Full adders are one of the most important elements in any arithmetic unit. The logic functions of a full adder can be expressed by C_{out}=AB+AC+BC, and SUM=A$\oplus$B$\oplus$C. Equation 3 expresses the functionality of a 1-bit FA based on 3- and 5-input Majority Gates (MGs). In [15-16], the reliability of FAs are analyzed by leveraging probabilistic transfer matrix (PTM) method, which shows that a FA design based on 3- and 5-input MGs has the lowest probability of failure for both C_{out} and SUM outputs that realizes a high-reliability design.

$$\begin{aligned} C_{OUT} &= AB + AC + BC = M3(A, B, C) \\ SUM &= ABC + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} = \\ & ABC + (A + B + C)\overline{M3} = M5(A, B, C, \overline{C_{OUT}}, \overline{C_{OUT}}) \end{aligned} \tag{3}$$

The computational mechanism for current-induced spin-based devices is accumulation-mode, which enables realization of MG. Hence, herein, 1-bit MG-based using SHE-MTJs developed. In this paper, Verilog-AMS is utilized to model the behavior of SHE-MTJ devices. Then, the model is leveraged in SPICE circuit simulator to validate the functionality of the designed circuits using experimental parameters listed in Table I. The transient switching behavior of SHE-MTJ devices are extracted using the model developed by Camsari et al. in [14] that utilizes a simplified Landau-Lifshitz-Gilbert (LLG) solver.

III. Proposed SHE-MTJ based FA

Figure 2 depicts the schematic of our proposed FA, which consists of three SHE-MTJs and 23 MOS transistors. The structure of the proposed SHE-based FA includes two main parts as described below.

TABLE I: Simulation Parameters of SHE-based FA.

Parameter	Description	Value
SHE-R	HM Volume (L×W×T)	120×60×3 nm^3
	MTJ Area (L×W)	60×30×π/4 nm^2
SHE-1	HM Volume (L×W×T)	100×60×3 nm^3
	MTJ Area (L×W)	60×30×π/4 nm^2
SHE-2	HM Volume (L×W×T)	150×80×3 nm^3
	MTJ Area (L×W)	80×40×π/4 nm^2
θ_{SHE}	Spin Hall Angle	0.3
ρ_{HM}	Resistivity	200 $\mu\Omega.cm$
ϕ	Potential Barrier Height	0.4 V
t_{ox}	Thickness of oxide barrier	1.2 nm
α	Gilbert Damping factor	0.007
M_s	Saturation magnetization	7.8e5 A.m^{-1}

The SHE-MTJs are designed in specific dimension to match with circuit requirements for providing optimal sensing performance with one reference (SHE-R).

A. Write/Reset circuit

For SHE-MTJ write operation, a charge current should be applied to the HM to produce a spin current greater than the critical switching spin current of the MTJ. In our SHE-based FA design, three PMOS transistors are leveraged to produce the input charge current according to the three inputs of the circuit, A, B, and C_{in}. The magnitude of the driven current for SHE-1 is determined based on the conservation of current on the N_1 node shown in Fig. 2. The dimensions of the SHE-1 is designed in a manner such that its switching critical current is higher than a charge current produced by one of the input PMOS transistor (MP_4, MP_5, and MP_6). In order for the C_{out} to become "1", the SHE-1 state should change to anti-parallel. Hence, at least two of the three input transistors are required to be ON to switch the SHE-1 state. Therefore, the three PMOS transistors and SHE-1 device together function as a 3-input MG. To perform the SHE-1 write operation, RES1, WR1, and SHE1 signals should be "0", "1" and "1", respectively. For reset operation, two NMOS transistors (MN_8 and MN_{10}) are assigned to reset the SHE-1 state and prepare it for next operation. Herein, reset operation means writing on SHE-MTJs in the -x direction to change their configuration to P state.

To implement the 5-input MG required for producing the SUM output, $\overline{C_{out}}$ is obtained through a sense amplifier, and MN_5 transistor is used to produce a current based on the obtained $\overline{C_{out}}$. The size of the MN_5 transistor is designed in a manner such that it generates a current amplitude approximately twice as large as the currents produced by input PMOS transistors (MP_4, MP_5, and MP_6). Therefore, it can be assumed that there are five input

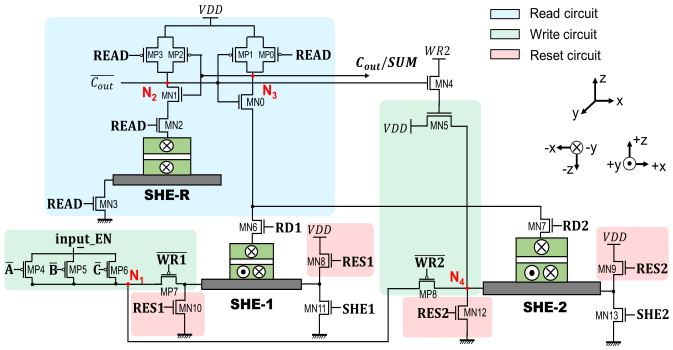

Fig. 2: Circuit-view of SHE-based FA design. SHE-1 functions as a 3-input MG, while SHE-2 performs 5-input MG function.

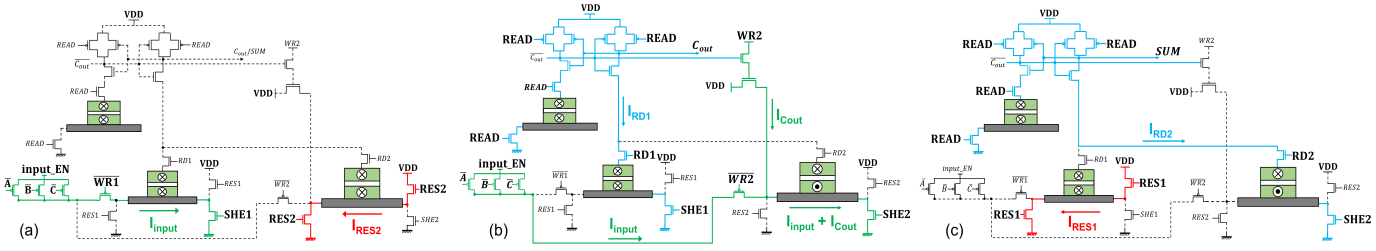

Fig. 3: SHE-based functionality for input ABC= "010" (a) Write and reset operations for SHE-1 and SHE-2 occurred, respectively, Iinput= 94 μA < $I_{C\text{-}SHE1}$; hence, FL of SHE-1 remains in P state, then (b) read and write operation for SHE-1 and SHE-2 perform simultaneously, in which injected current through SHE-2 is 146 μA > $I_{C\text{-}SHE2}$, so FL of SHE-2 changes to AP state, and finally (c) SHE-1 is reset along with reading SHE-2 state.

currents injected to SHE-2. The magnitude of the current applied to the HM of the SHE-2 is determined based on the conservation of the aforementioned currents in N_1 node. Dimensions of the SHE-2 is designed in a way that at least three out of the five inputs should be applied to HM to produce a current amplitude greater than the critical current of SHE-2. Thus, SHE-2 functions as a 5-input MG. SHE-1 read operation and SHE-2 write operation should be performed simultaneously. Therefore, all of the RD1, SHE1, WR2, and SHE-2 signals should be "1" during this operation. The reset mechanism for SHE-2 is similar to that of the SHE-1. However, it can be improved by performing the reset operation only when C_{out} equals "1". Thus, unnecessary reset operations will be removed, which can decrease the energy and delay overhead caused by the reset scheme. The dimensions of the SHE-MTJs used herein are listed in Table I.

B. Read Circuit

The main component of reading scheme is a pre-charge sense amplifiers (PCSAs) [17], which operates in two phases: *pre-charge* and *discharge*. In pre-charge phase, READ signal is "1" and N_2 and N_3 nodes are charged to V_{DD}. In discharge phase, READ="0" and SHE1 or SHE2 signals equal "1". Due to the difference between the resistances of the SA's branches, each branch will discharge at a different speed. The branch with higher resistance discharge more slowly and finally outputs V_{DD} that denotes "1", and vice versa. To perform proper sensing operation, the reference SHE-MTJ device (SHE-R) is designed in a way that its resistance value in parallel configuration is between low resistances (R_Ps) and high resistances (R_{AP}s) of the SHE-1 and SHE-2 cells. Table II elaborates the required signaling for performing the write, read, and reset operations.

IV. Simulation Results

To verify the functionality of proposed SHE-based FA design, SPICE circuit simulator and SHE-MTJ model with parameters mentioned in Table I are utilized. Figure 3 shows the functionality of our proposed SHE-based FA, in which the applied inputs are ABC="010". Write, read, and reset operations are indicated by green, blue, and red colored shading, respectively. There are three phases for one complete operation cycle of SHE-FA. In phase I, shown in Fig. 3.(a), write and reset transistors for SHE-1 and SHE-2 are enabled, respectively. The produced input charge current according to ABC="010" equals 94 μA, which is smaller than SHE-1 critical current, i.e. $I_{C\text{-}SHE1}$=108 μA. Thus, the FL magnetization direction of SHE-1 remains in P state. Simultaneously, the SHE-2 reset transistors generate a 164 μA current amplitude in -x direction, which can reset SHE-2 to P state in 2.07ns.

Figure 3.(b) depicts the second phase of SHE-FA operation including reading SHE-1 and writing SHE-2 devices at the same time. As mentioned above, since the SHE-1 input current for ABC="010" is not sufficient to switch its states, C_{out} and $\overline{C_{out}}$ equal "0" and "1", respectively. Therefore, MN_4 and MN_5 transistors are ON, and $I_{\overline{C_{out}}}$ will be generated. Input currents and $I_{\overline{C_{out}}}$ are accumulated in N_4 node, and produce the SHE-2 write current. In this example, the magnitude of the injected current equals 146 μA, which is greater than SHE-2 critical current, i.e. $I_{C\text{-}SHE2}$=139 μA. Thus, the state of the SHE-2 device changes to AP configuration.

In the third phase, the reset and read operations are performed for SHE-1 and SHE-2, respectively. Due to the difference between the resistances of the SHE-1 and SHE-2 HMs, the produced reset current for SHE-1 is different

TABLE II: Required signaling for 1-bit SHE-based FA.

Operation	Device	Signaling
WRITE	SHE-1	READ= "0", WR1= SHE1= "1"
	SHE-2	WR2= SHE2= SHE1= RD1= READ= "1"
READ*	SHE-1	RD1= SHE1= READ = "1"
	SHE-2	RD2= SHE1= READ= "1"
	SHE-R	READ= "1"
RESET	SHE-1	RES1= "1"
	SHE-2	RES2= "1"

($*$) When READ is set("1"), node N_2 in Fig. 2 is connected to the ground via SHE-R, which is in parallel configuration.

$R_{SHE\text{-}1\ (P)}$, $R_{SHE\text{-}2\ (P)} < R_{SHE\text{-}R\ (P)} < R_{SHE\text{-}1\ (AP)}$, $R_{SHE\text{-}2\ (AP)}$

TABLE III: SHE-based FA Performances for all Input Combinations.

Standard functions			I_{SHE1}	Power (μW)		Delay		C_{out}	I_{SHE2}	Power (μW)		Delay		SUM
A	B	C	(μA)	write	read	write	delay		(μA)	write	read	write	read	
0	0	0	0	0	14.72	N/A	41 ps	0	112	137	14.72	N/A	41 ps	0
0	0	1	94	113	14.72	N/A	41 ps	0	146	178	12.4	2.7 ns	30 ps	1
0	1	0	94	113	14.72	N/A	41 ps	0	146	178	12.4	2.7 ns	30 ps	1
0	1	1	136	162	12.4	2.25 ns	30 ps	1	135	163	14.72	N/A	41 ps	0
1	0	0	94	113	14.72	N/A	41 ps	0	146	178	12.4	2.7 ns	30 ps	1
1	0	1	136	162	12.4	2.25 ns	30 ps	1	135	163	14.72	N/A	41 ps	0
1	1	0	136	162	12.4	2.25 ns	30 ps	1	135	163	14.72	N/A	41 ps	0
1	1	1	158	188	12.4	1.89 ns	30 ps	1	157	189	12.4	2.45 ns	30 ps	1

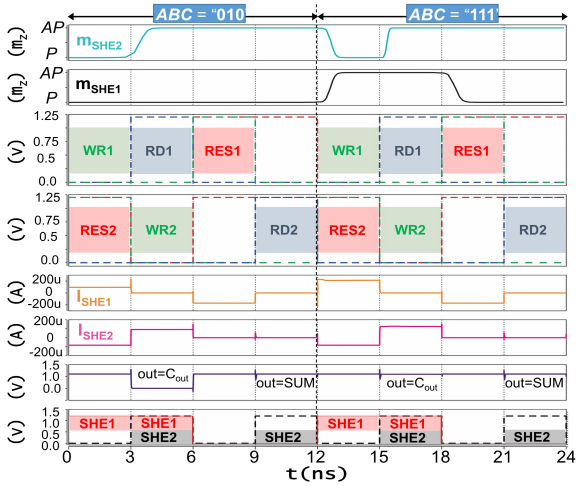

Fig. 4: Simulation results of 1-bit SHE-based FA for two input sequences, "010" and "111".

from that of the SHE-2. SHE-1 reset current equals 170 μA, which result in a 1.73 ns delay for SHE-1 reset operation. In this phase, SHE1 and SHE2 signals are equal to "0" and "1", respectively. Thus during the read operation, PCSA senses the state of the SHE-2 device that is the SUM output. As mentioned above, SHE-2 was configured to AP state in the second phase, therefore the output of the PCSA equals "1". Simulation results including timing diagram and SHE-MTJs' magnetization directions are depicted in Fig. 4, which validates the functionality of our proposed FA for two sets of inputs, ABC= "001" and ABC= "111". Propagation delays, produced charge currents, and power consumption for all possible input combinations are listed in Table III. Table IV provides comparison between our 1-bit SHE-based FA and previous CMOS-based [18] and MTJ-based [18] 1-bit FAs in terms of delay, area, power consumption, and complexity. The current-mode FAs that are proposed in [7-19] are excluded from our comparison.

To investigate the effect of V_{DD} scaling on the performance of the SHE-based FA, we have simulated our design at super-threshold, near-threshold, and sub-threshold regions. However, as it can be seen in Fig. 5, for V_{DD} values lower than 0.5 V, transistors' width should be significantly enlarged to produce the write current required for switching. For instance, for V_{DD}= 0.5V, the width of transistors should be 8 times larger than the transistors utilized in V_{DD}= 1V. It is worth noting that MTJ switching could not be achieved in sub-threshold region, since the produced write currents were significantly smaller than required switching critical current.

Herein, we have examined the functionality of an *n*-bit SHE-FA to verify the concatenatability of our SHE-based FA. Figure 6 shows the schematic and timing diagram for a 4-bit SHE-based FA. To obtain the SUM output for each adder block, C_{out} of their previous block is required to be applied as one of the three input signals. Hence, each C_{out} bit in level *n* is utilized to obtain, (1) SUM output in level *n*, and (2) C_{out} bit in level *n+1*. Therefore, the C_{out} in each level should remain unchanged for a sufficient duration to ensure the correct operation of an *n*-bit SHE-FA. This can be achieved by SHE-MTJ devices without any additional energy consumption, due to their non-volatility feature. The timing limitations are considered in the timing diagram shown in Fig. 6. To decrease the propagation delay of an *n*-bit SHE-FA, the independent operations are designed to be performed simultaneously. Namely, C_{out} write operation for the second adder block is independent of the SUM write operation of the first block, thus both are operated in the second time step.

Power consumption of an *n*-bit SHE-FA relies on the number of write, read, and reset operations that are required to be executed for a complete addition cycle. For instance, there are 8 SHE-MTJs in a 4-bit SHE-FA, thus eight write and reset operations should be performed in a complete addition operation. Moreover, as shown in Fig. 6, eleven

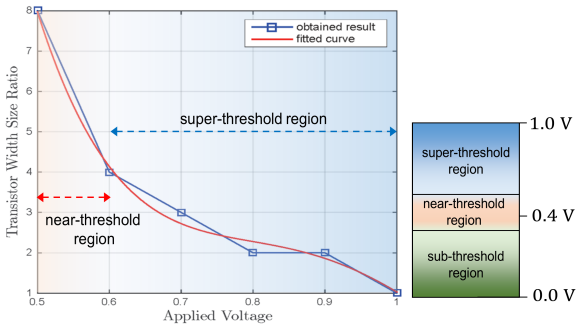

Fig. 5: (left) Transistor width needed for various supply voltages, (right) three threshold regions applicable to the transistors used herein. (V_{DD}= 1V, V_{th}= 0.4V).

TABLE IV: Comparison of logic-in-memory 1-bit full adder circuits.

Parameter	CMOS [18]	MTJ- based [18]	developed herein
Delay*	2.2 ns	10.2 ns	7 ns
Dynamic Power†	2 mW	2.1 mW	0.71 mW
Static Power	0.9 nW	0	0
Area	333 μm^2	315 μm^2	180 μm^2
Device Count	42 MOSs	34 MOSs + 4 MTJs	23 MOSs + 3 SHEs

($*$) Total delay including write and read operations.

($\dagger$) Dynamic power depends on the number of current paths from

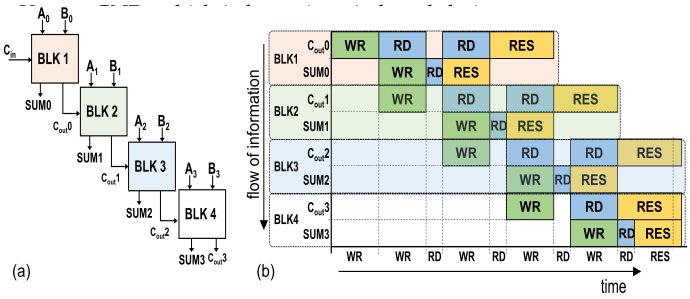

Fig. 6: Schematic of 4-bit SHE-based FA and its timing diagram.

read operations are performed in a complete cycle; eight operations to output the SUM and C_{out} values and three operations for switching SHE-2 states. In general, the total propagation delay and power consumption of our proposed n-bit SHE-based FA can be calculated using below equations:

$$D_{n-FA} = DWR_{SHE-1} + N \times (DWR_{SHE-2}) + N \times (D_{SA}) + DRES_{SHE-2} \tag{4}$$

$$P_{n-FA} = 2N \times (PWR_{SHE-2}) + 2N \times (PRES_{SHE-1}) + (3N-1) \times (PRD_{SHE-1}) \tag{5}$$

where, N is number of bits, DWR_{SHE-1} and DWR_{SHE-2} are write operation delays of SHE-1 and SHE-2, respectively. D_{SA} is PCSA delay, and $DRES_{SHE-2}$ is reset operation delay of SHE-2. PWR_{SHE-2}, $PRES_{SHE-1}$, and PRD_{SHE-1} are the power consumption of SHE-2 write, SHE-1 reset, and SHE-1 read operations, which are the worst case values for each quantity.

V. Conclusion

In this brief, we have leveraged SHE-MTJ devices to develop a novel non-volatile 1-bit FA. Behavior of the SHE-MTJ are modeled and simulated in Verilog-AMS, and calibrated with the previous experimental results. The SHE-based FA was examined using SPICE circuit simulator, which indicated 76% and 32% improvements in terms of energy consumption and area over the previous spin-based FA, respectively. Due to the scalability and voltage-based operation of our proposed 1-bit SHE-FA, it can be readily concatenated to constitute an n-bit SHE-based adder or an n-bit SHE-based ALU with significantly low area and energy consumption as depicted by the pipeline analysis.

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