

SoCrates - A Scalable Multiprocessor System On Chip

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Abstract

This document is the result of a Master Thesis in Computer Engineering, describing the analysis, specification and implementation of the first prototype of Socrates, a configurable, scalable and predictable platform for System-on-chip Multiprocessor system for real-time applications. The design time of System-on-a-Chip (SoC) is today rapidly increasing due to high complexity and lack of efficient tools for development and verification. By combining all the functions into one chip the system becomes smaller, faster, and less power consuming but increasing the complexity. To decrease the time-to-market SoCs are entirely or partially build with IP-components. Thanks to SoC, a whole new domain of products, like small hand held devices, has emerged. The concept has been around a few years now, but there are still challenges that needs to be resolved. There is a lack of standards for enabling fast mix and match of cores from different vendors. Further needs are new design methods, tools, and verification techniques. SoC solutions needs special kind of CPUs that consumes less power, is cheaper, smaller, but still has high-performance requirements. To fulfill all these demands, they are getting more and more complex as the number of transistors are rapidly growing which has led to the emerging of multiprocessors systems-on-a-chip. Our initial question is to investigate if it is possible to build these complex multiprocessors systems on a single FPGA and if these solutions can lead to shorter time-to-market. The consumer demands for cheaper and smaller products makes FPGA solutions interesting. Our approach is to have multiple processing nodes containing processing unit, memory and a network interface all together connected on a shared bus. A central in-house developed hardware real-time unit handles scheduling and synchronization. We have designed and implemented a MSoC that fits on a single FPGA in only 40 days, which has to our supervisors knowledge not been accomplished before. Our experience is that a tightly coupled group can produce fast results since information, new ideas and bug reports propagates immediately.

References

- [1] David E.Culler, Pal Singh, Jaswinder and Anoop Gupta. *Parallel Computer Architecture, A Hardware/software approach*, Morgan Kaufmann Inc, San Fransisco California, 1999, ISBN 1-55860-343-3.
- [2] Sven Eklund *avancerad datorarkitektur*, Studentlitteratur, Lund, 1994, ISBN 91-44-47671-X.
- [3] global sources. *System-on-a-chip sets new rules in the industry*
global sources MArS 10, 1999.
<http://www.globalsources.com/MAGAZINE/EC/9905/SOCREP.HTM>
- [4] Bill Cordan, Palmchip Corporation *An effecient bus architecture for system-on-chip design* Custom INtegrated Circuits, 1999. Proceedings of the IEEE 1999 pp: 623-626

- [5] Sibabrata Ray, Hong Jiang. *A reconfigurable bus structure for multiprocessors with bandwidth reuse*, Journal of Systems Architecture 45, 1999
- [6] Hammond Lance, Olukotun Kunle. *Considerations in the Design of Hydra: A Multiprocessor-on-a-Chip Microarchitecture*, Stanford Technical Report CSL-TR-98-749, Stanford University, 1998.
- [7] Lars-Hugo Hemert *Digitala kretsar*, Studentlitteratur, Lund, 1996, ISBN 91-44-00099-5.
- [8] John L. Hennessy, David A. Patterson *Computer Architecture A Quantitative Approach, second edition*, Morgan Kaufmann Inc, San Fransisco California, 1996, ISBN 55860-329-8.
- [9] Vincent P. Heuring & Harry F. Jordan *Computer Systems Design and Architecture*, Addison Wwesley, California, 1997, ISBN 0-8053-4330-X.
- [10]Howard Sachs, Mark Birnbaum *VSIA Techical Challenges Custom Integrated Circuits*, 1999. Proceedings of the IEEE 1999 , 1999 , Page(s): 619 -622
- [11]Geert Rooseel, Sonics Inc. *Decouple core for proper integration* EETIMES Jan 3, [2000. www.eetimes.com/story/OEG2000010350048](http://www.eetimes.com/story/OEG2000010350048)
- [12]Jon Turino, SynTest Technologies, Inc. *emphDesign for Test and Time to Market - Friends or Foes Test Conference*, 1999. Proceedings. International, 1999 , Page(s): 1098 -1101
- [13]Lewis, Jeff. *Intellectual Property (IP) Components*, Artisian Components Inc. <http://www.ireste.fr/fdl/vcl/ip/ip.htm>
- [14]Olukotun Kunle, Bergman Jules, Kun-Yung Chang and Basem Nayfeh. *Rationale, Design and Performance of the Hydra Multiprocessor*, Stanford Technical Report CSL-TR-94-645, Stanford University, 1994
- [15]RealChip Custom communication Chips.
System-on-Chips,
<http://www.realchip.com/Systems-on-Chips/Systems-on-chips.html>
- [16]Rincon Ann Marie, Cherichetti Cory, Monzel James. A, Stauffer David, R, Trick Michael, T. IBM Microelectronics Corp.
Core Design and System-on-a-Chip Integration, IEEE Design & Test of Computers. Volume: 14 4 , Oct.-Dec. 1997, pp: 26-35
- [17]Rincon Ann Marie, Lee William. R and Slattery Michael.
IBM Microelectronics Corp.
The Changing Landscape of System-on-Chip Design, Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999, pp: 83-90
- [18]IBM Microelectronics Corp & Synopsys, Inc./Logic Modeling *Design Environment for System-OnA-Chip Products & solutions Success Stories*
http://www.synopsys.com/products/success/soc/soc_wp.html
- [19]Wilson, Ron. *Is SoC really different?*, EETIMES November 8, 1999.
<http://www.eetimes.com/story/OEG19991108S0009>
- [20]Wilson, Ron. *The rest of the SoC task*, EETIMES October 11, 1999.
<http://www.eetimes.com/story/OEG19991011S0006>
- [21]David Patterson. *Vulnerable Intel*, The New York Times, June 9, 1998, pp: 44-49

- [22]Manfred Schlett. *Trends in Embedded-Microprocessor Design*, Computer, August, 1998.
- [23]Wulf Wm. A and McKee Sally. A. *Hitting the Memory Wall: Implications of the Obvious*, Computer Science Report CS-94-48.
- [24]Prince Betty Memory strategies International, USA
Memory in the fast lane, IEEE Spectrum Feb 1994, Vol 31, Issue 2. PP: 38-41.
- [25]Golla C and Ghezzi S. *Flash Memory Architecture*, Microelectron Reliab.. Vol 38, No 2, 1998, pp: 179-184.
- [26]Abraham S.G, Sugumar R.A, Windheiser D, Rau B. R and Gupta R. *redictability of load/store instruction latencies* Microarchitecture, 1993, pp: 139-152.
- [27]Boland K and Dollas A, AT&T Global Information *Predicting and precluding problems with memory latency* IEEE Micro, Aug 1994, Vol 14, Issue 4, pp: 59-67.
- [28]Katayama Y, IBM Research, Tokyo, Japan *Trends In Semiconductor Memories* IEEE Micro, 1997, Vol 17, Issue 6, pp: 10-17.
- [29]Rao R. Tummala, Vijay K. Madiseti *System on Chip or System on Package ?* IEEE Design & Test of Computers Volume: 16 2 , April-June 1999 , Page(s): 48 -56
- [30]Mark Dorais, ROHM ELECTRONICS *Analyze ASIC Designs To Optimize Integration Levels* ELECTRONIC DESIGN ONLINE, August 1999
<http://devel.penton.com/ed/Pages/magpages/aug0999/digitech/0809dt3.htm>
- [31]Lage C, Hayden J.D and Subramanian C. Adv. Products Res. & Dev. Lab., Motorola Inc., Austin, TX, *Advanced SRAM technology-the race between 4T and 6T cells* Electron Devices Meeting, 1996., International Dec 1996, pp: 271-274.
- [32]Takai Y, Nagase M, Kitamura M, Koshikawa Y, Yoshida N, Kobayashi Y, Obara T, Fukuzo Y and Watanabe H. *250 Mbyte/s Synchronous DRAM Using a 3-Stage-Pipelined Architecture* IEEE Journal of Solid-State Circuits. April 1994, Vol 29, Issue 4, pp: 426-431.
- [33]Henry Chang, Larry Cooke, Merrill Hunt, Grant Martin, Andrew McNelly, Lee Todd. *Surviving the SOC Revolution, A Guide to Platform-Based Design*, Kluwer Academic Publishers, 1999, ISBN 0-7923-8679-5.
- [34]National Semiconductor, Geode Products
Geode SC1400 (Information Appliance-on-a-Chip)
www.national.com/appinfo/solutions/0,2062,243,00.html
- [35] International Competence Cluster for System-on-a-Chip to be created in Sweden
<http://www.isa.se/default.cfm?page=/regionalinfo/index.htm>
- [36] Embedded Systems and the Year 2000 Problem
Mark A. Frautschi
Draft of 10 September 1999, Shakespeare and Tao Consulting
- [37] The Pittsburgh Digital Greenhouse
<http://www.digitalgreenhouse.com/>
- [38] www.arm.com
- [39] AMBA specification (REV 2.0) ARM Limited, 13 may [1999. www.arm.com](http://www.arm.com)

- [40] www.palmchip.com
- [41] S. E. Crawford, and R. F. DeMara. Cache coherence in a multiport memory environment. *Massively Parallel Computing Systems, Proceedings. 1994. pp: 632-642.*
- [42] O'Krafka, B.W & Newton, A.R. *An empirical evaluation of two memory-efficient directory methods* Computer Architecture, 1990. Proceedings. 1990. pp: 138-147.
- [43] Farkas, K.I, Jouppi, N.P & Chow, P. *How useful are non-blocking loads, stream buffers and speculative execution in multiple issue processors?* High-Performance Computer Architecture, Proceedings. 1995. pp: 78-89.
- [44] Sez nec, A. *DASC cache* High-Performance Computer Architecture, Proceedings. 1995. pp: 134-143.
- [45] Jouppi, N.P. *Improving direct-mapped cache performance by the addition of a small fully-associative cache and prefetch buffers* Computer Architecture, Proceedings. 1990. pp: 364-373.
- [46] Jouppi, N.P. *Cache Write Policies and Performance* Computer Architecture, Proceedings. 1993. pp: 191-201.
- [47] Agarwal, A & Pudar, S.D. *Column-associative Caches: A Technique For Reducing The Miss Rate* Computer Architecture, Proceedings, 1993. pp: 179-190.
- [48] Pendse, R & Bhagavathula, R. *Performance of LRU block replacement algorithm with pre-fetching* Circuits and Systems, Proceedings. 1998. pp: 86-89.
- [49] Colagiovanni, L. & Shaout, A. *Cache memory replacement policy for a uniprocessor system* Electronics Letters, 14 April 1990. Vol. 26 Issue: 8. pp: 509-510.
- [50] So, K & Rechtschaffen, R.N. *Cache operations by MRU change* IEEE Transactions on Computers June 1988. Vol. 37 Issue: 6. pp: 700-709.
- [51] Stiliadis, D & Varma, A. *Selective victim caching: a method to improve the performance of direct-mapped caches* IEEE Transactions on Computers, May 1997, Vol. 46, Issue: 5 pp: 603-610.
- [52] , S & Kessler, R.E. *Evaluating stream buffers as a secondary cache replacement* Computer Architecture, Proceedings 1994. Proceedings, pp: 24-33.
- [53] Wong, W.A & Baer, J-L. *Modified LRU policies for improving second-level cache* High-Performance Computer Architecture, 2000. HPCA-6. pp 49-60.
- [54] *Core Connect Bus Architecture* International Business Machines Corporation, 1999
www.chips.ibm.com
- [55] *Microprocessor system buses: A case study* Ehud Finkelstein, Shlomo Weiss Journal of Systems architecture 45 (1999) pp: 1151-1168