Compact Spintronic Muller C-Element with Near-Zero Standby Energy

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***Abstract*—The complementary roles of asynchronous architecture with nonvolatile spintronic devices are explored herein to realize a novel asynchronous logic element. By redesigning the Muller C-Element to take advantage of spintronic device non-volatility and area-efficiency, benefits such as reduced asynchronous handshaking area overhead, are achieved in addition to instant on/off capabilities for reduced static-power dissipation through power-gating. We propose a novel 8 transistor and 1 spintronic device Muller C-Element design which is 20% faster and uses 68% of the power of previous non-volatile Muller C-Element designs. This spintronic Muller C-Element is demonstrated within a 4-phase dual-rail asynchronous pipeline resulting in 48% fewer transistors in comparison with the previous designs. Additionally, bundled-data protocol overhead is shown to be reduced by using the spintronic Muller C-Element proposed herein. Detailed analysis of the effects of driving transistor width and the Tunneling Magnetoresistance Ratio on device performance characteristics is included.**

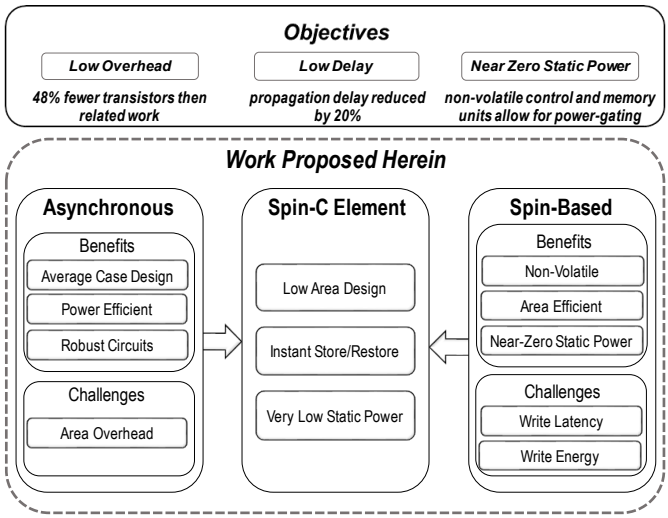


Figure 1: Objectives and approaches of the proposed work.

I. INTRODUCTION

As technology advances towards CMOS scaling limits, new and innovative strategies using emerging devices to explore intriguing energy versus performance tradeoffs at both circuit and architecture levels. Asynchronous architectures are characterized as requiring no clock tree, high power efficiency, circuit elasticity, and robustness [1-3]. By utilizing local clock generation control circuits instead of the global synchronization clock found in synchronous pipelines. Local clock generation in lieu of global synchronization provides robust, elastic, and high performance circuits with on-demand power consumption by design [1]. Systems with similar levels of robustness, performance, and power efficiency are difficult, if even possible, to realize using synchronous design [1]. This is due to synchronous designs being limited by the worst case logic delays register setup and hold times, process variation, and aging-based circuit degradation [1]. Additionally, propagation delays, multiple clock domains, and the exponentially increasing circuit complexity of today's microprocessors all contribute to increasingly complex clock trees and the associated area and energy overheads relative to the circuits they are controlling in synchronous pipelines [4]. Heat, power, security, and electromagnetic radiation issues also arise from the large power spikes following the clock edge, which is avoided with asynchronous design [3]. However large area overheads are required in order to implement the local-clock generation circuitry [1-3]. Such challenges have limited asynchronous architectures to a niche but growing range of applications such as cryptography, energy autonomous systems, and sensors [3]. The work proposed herein aims to leverage the properties of emerging spintronic devices to address the challenges of asynchronous architectures in a mutually-beneficial way as illustrated in Figure 1. We will utilize these approaches to bridge circuit-level properties of non-volatile devices with architectural level properties of asynchronous pipelines.

The following research contributions are provided:

1) a novel, compact spintronic-based Muller C-element design for reducing asynchronous control area overhead,
2) reducing power-gating store and restore delay and circuit overheads by operating in an intrinsically non-volatile manner, and

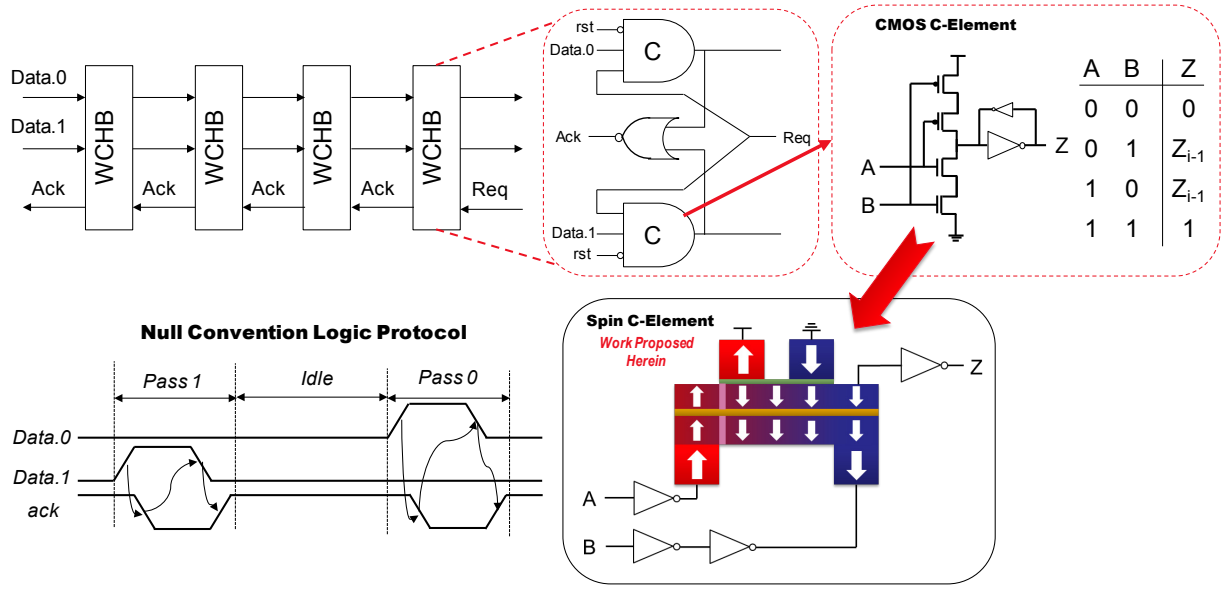


Figure 2: Null Convention Logic, Weak Conditioned Half Buffer, Muller C-Element gate, CMOS implementation, and proposed implementation.

3) realization of a delay-element-free asynchronous Bundled Data pipeline.

The remainder of this article is organized as follows; Section II briefly describes asynchronous architectures and spintronic devices in order to provide background information on the devices and circuits utilized herein, Section III describes related works, Section IV introduces two functionally-equivalent, but distinct spintronic Muller C-Element designs and evaluates their power and performance characteristics, Section V implements the spintronic Muller C-Element into common asynchronous pipelines and details the results, Section VI provides a discussion of the challenges and prospects for this work, and Section VII concludes the paper.

II. Background Information

In this section, two asynchronous pipeline designs which are in prevalent use and their benefits are described in addition to identifying the fundamental properties of spintronic devices and characteristics of the particular device utilized herein.

A. Muller C-Element for Asynchronous Pipeline Control

Asynchronous design is an established field with a large variety of protocols available, and is out of the scope of this paper to describe them in detail completely. Thus, we will introduce two protocols used herein. The 4-phase dual-rail quasi-delay-insensitive Null Convention Logic (NCL) pipeline as depicted in Figure 2 is based on dual-rail logic, which uses 2 wires, noted as *Data.0* and *Data.1*, to transfer every bit of data [1]. If *Data.0* is asserted logic high, then a logic 0 is transferred. If *Data.1* is asserted logic high, then a 1 is transferred. If both *Data.0* and *Data.1* are asserted logic low, then a NULL value is transferred, and it is not allowed for both *Data.0* and *Data.1* to be asserted logic high at the same time. The basic register element for our particular NCL implementation is called the Weak-Conditioned Half Buffer (WCHB) and is shown in Figure 2. The WCHB works by correlating the request (*req*) signal of the next stage with the input dual-rail data of the previous stage to determine

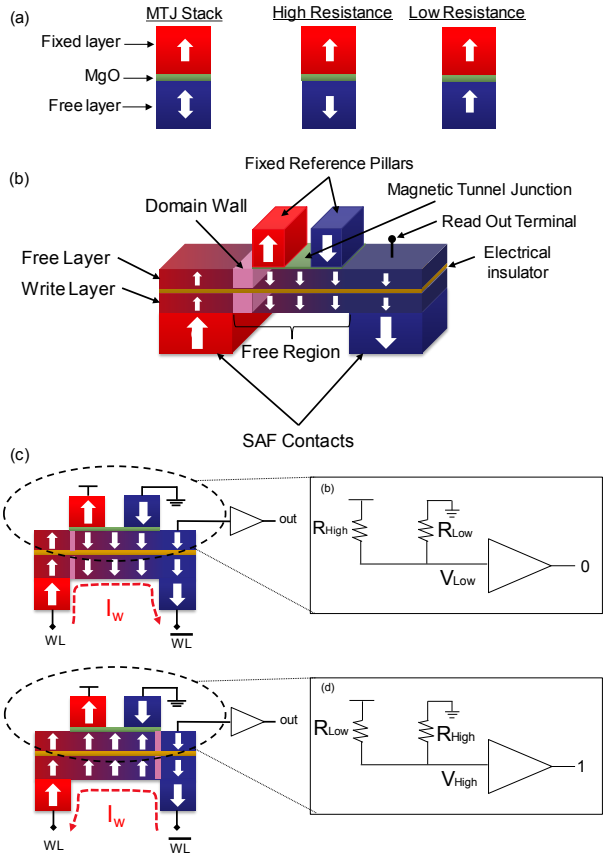


Figure 3: Domain Wall Coupled STT Device. a) MTJ stack parallel and anti-parallel states, b) DWCSTT device structure, and c) voltage-divider-based state-sensing scheme.

if it can record the previous stage's data. When a data signal is asserted high, the WCHB resets the *ack* signal, indicating that it is not ready to accept data, other than a NULL value. Once a NULL value is received, the *ack* signal is set and indicates that it is ready to accept new data. With this inter-stage handshaking, data flows through the pipeline in a coordinated accurate-by-design method without a need for global synchronization.

The asynchronous Bundled-Data protocol lacks the dual-rail logic of NCL architectures, which alleviates the overhead needed for two wires per bit, but negates the intrinsic completion detection of NCL designs [1]. By contrast, Bundled-Data is implemented with standard pipelining of combinational logic and local clock generation by inserting delay elements equivalent to the delay of the combinational logic between clock generating circuits as shown in Figure 8.

Regardless of the protocol, the key element for implementing the inter-stage handshaking that many asynchronous pipelines depend on is the *Muller C-Element* [5]. As depicted by Figure 2, the Muller C-Element asserts a logic 1 when both inputs are logic 1 and asserts a logic 0 when both inputs are logic 0; if the inputs are different, then its output does not change. The key principle of this operation is that an output change indicates that both of the inputs are identical to the output at that transition. One particular low-area CMOS implementation of the Muller C-Element is shown in Figure 2 and utilizes a weak-inverter based SRAM cell to store the output data until a (0,0) or (1,1) condition is reached [6]. The volatile state of this design leads to increased static power dissipation and power-gating overheads by requiring additional store and restore circuitry and delays if power-gating is desired. The work proposed herein utilizes the non-volatile memory properties of a particular spintronic device for implementing a compact Muller-C element with instant store/restore functionality for reduced asynchronous pipeline area and power-gating requirements.

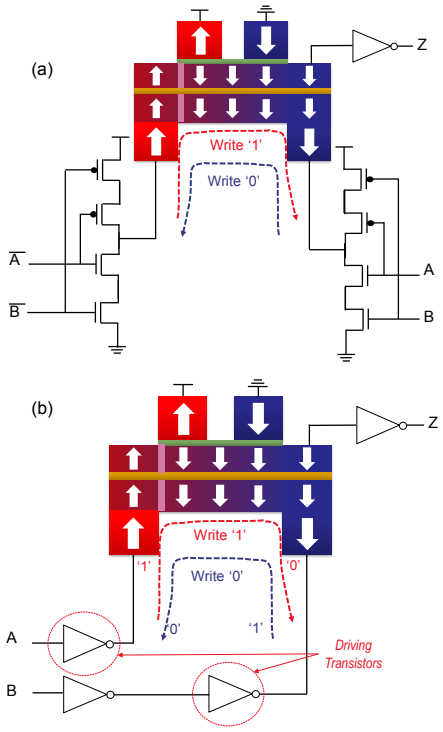


Figure 4: Two Spintronic Muller C-Element designs.

B. Spintronic Fundamentals

Spintronic devices offer high-speed non-volatile memory with good scaling, area, and power characteristics [7]. The fundamental principle by which spintronic devices operate is the manipulation of the magnetization orientation of a nanomagnet between two stable states. Sensing the current state of the nanomagnet magnetization is done by using the tunneling magnetoresistance effect of a Magnetic Tunnel Junction (MTJ) [8-9]. A simple abstracted view of an MTJ is shown in Figure 3a. A thin oxide layer (typically MgO) is sandwiched between two ferromagnetic layers. The top layer is "fixed" and will be unable to change its magnetic orientation after fabrication. Also, the bottom layer is "free" and can be manipulated using current, magnetic field, or electric field, depending on the device structure. If the magnetic orientation of the free layer is parallel to the fixed layer, then the MTJ will have a lower resistance (R_{Low}) than if the free layer is anti-parallel to the fixed layer (R_{High}), as shown in Figure 3a. A critical parameter of the MTJ is the *Tunneling Magnetoresistance Ratio (TMR)*, which is the relative resistance change between R_{Low} and R_{High} defined as TMR = $[(R_{High} - R_{Low})/R_{Low}] * 100\%$.

$$\frac{\partial \vec{m}}{\partial t} = -\gamma(\vec{m} \times \overrightarrow{H_{eff}}) + \alpha\left(\vec{m} \times \frac{d\vec{m}}{dt}\right) - u(\vec{j}.\nabla)\vec{m} + \beta u\vec{m} \times (\vec{j}.\nabla)\vec{m} \quad (1)$$

$$\overrightarrow{H_{eff}} = -\frac{\delta_w}{\mu_0 M_s \delta_m} \qquad u = \frac{\mu_B JP}{eM_s} \quad (2)$$

The particular spintronic device used herein is the *Domain Wall Couple Spin-Torque-Transfer* (DWCSTT) device introduced in [10] and shown in Figure 3b. This device uses two electrically isolated, but magnetically coupled domain wall strips to isolate the read and write mechanisms of the device. The device state is sensed through the two anti-parallel fixed reference pillars, which have MTJs with the underlying domain-wall-based free layer. The domain wall only has two stable states as shown on the left side of Figure 3c, and therefore one fixed reference pillar will always be R_{High} and the other will be R_{Low}, and they will alternate depending upon the location of the domain wall. If the TMR of the MTJs is large enough (~100%), then we can use the two MTJs

of the DWCSTT device as a voltage divider to output a V_{low} or a V_{high}, which can switch a CMOS inverter as shown in Figure 3c. The write operation of the device is performed by passing a current through the lower domain wall ferromagnetic layer, denoted as the write layer, which is first spin-polarized through the *Synthetic Anti-Ferromagnetic* contacts, and then exerts a *Spin-Transfer-Torque* (STT) on the write layer, which can move the domain wall according to the Landau-Lifshitz-Gilbert equation below [11]:
where μ_B is the Bohr Magneton, γ is the gyromagnetic ratio, μ_0 is the free space permeability, α is the adiabatic damping coefficient, β is the non-adiabatic spin transfer term, J is the current density, P is the spin polarization, M_s is the saturation magnetization, e is the electron charge, and u is the domain wall velocity. Since the upper domain wall ferromagnetic layer, denoted as the free layer, has strong dipolar coupling with the write layer, its magnetization will rotate in conjunction with the write layer as it undergoes STT. The velocity of the domain wall is linearly related to the current density applied to the write layer, and experimental results show that domain wall velocities up to 125 m/s is achievable with current densities near 1.8e8 A/cm^2 [12]. Using standard 16nm PTR CMOS models [13] with a supply voltage of 0.7V, we are able to achieve respectable write speeds by simply applying logic "1" or "0" (*vdd* or *gnd*) to the device inputs. By varying the driving transistor widths we are able to adjust the speed and power draw of the device.

III. Related Work

Several previously developed CMOS and spintronic Muller C-Element designs and their associated results are listed in Table 1 [1-2,14]. Yancey et al. provided a comprehensive comparison between current CMOS-based Muller C-Element designs as well as a proposed Differential Null Convention Logic design [14]. Zianbetov et al. developed a hybrid CMOS-MTJ Muller C-Element with body biasing and a silicon-on-insulator design [1]. Their design typically operates in an ordinary CMOS-only fashion for high speed, with a propagation delay of just 32 ps, and can then backup the state data to non-volatile MTJ cells prior to powering the circuit down for power-gating. The metrics listed in Table 1 compare only the backup delay and power instead of the standard CMOS-only high-speed operation in order to compare the NV operation of the design with the intrinsically NV operation of the design proposed herein. NV operation can increase radiation-induced soft error immunity. For instance, Onizawai et al. proposed their design to address Single Event Upsets using the resilience of MTJs [2]. Their design lacks the CMOS-only high speed operation of Zianbetov et al. as their focus was to improve reliability, and as such, needed to write to the non-volatile cells every operation.

Table 1: Related Research in Muller C-Element Design

C-Element	Volatile/Non-Volatile	Transistor Count	Delay	Total Power
Static [13]	Volatile	12	104 ps	-
Semi-Static [13]	Volatile	8	139 ps	-
DNCL [13]	Volatile	8	71 ps	-
Zianbetov et al.	Non-Volatile	17	1 ns	50 uW
Onizawai et al.	Non-Volatile	38	1.05 ns	263.8 uW
Proposed Herein	Non-Volatile	8	801 ps	34.04 uW

IV. Proposed Spintronic Muller C-Element Designs

When developing the spintronic Muller C-Element, two functionally-correct designs were obtained. The first design developed is shown in Figure 4a and operates by only allowing one p-MOS branch and one n-MOS branch to be "on" when *A* and *B* are either (0,0) or (1,1), and all CMOS branches to be in a high-impedance state when *A* and *B* are (1,0) and (0,1). This causes current to pass through the write terminals of the DWCSTT device only when the output transitions according the Muller C-element functionality shown in Figure 2. It also restricts current flow through the write terminals when output transitions do not occur.

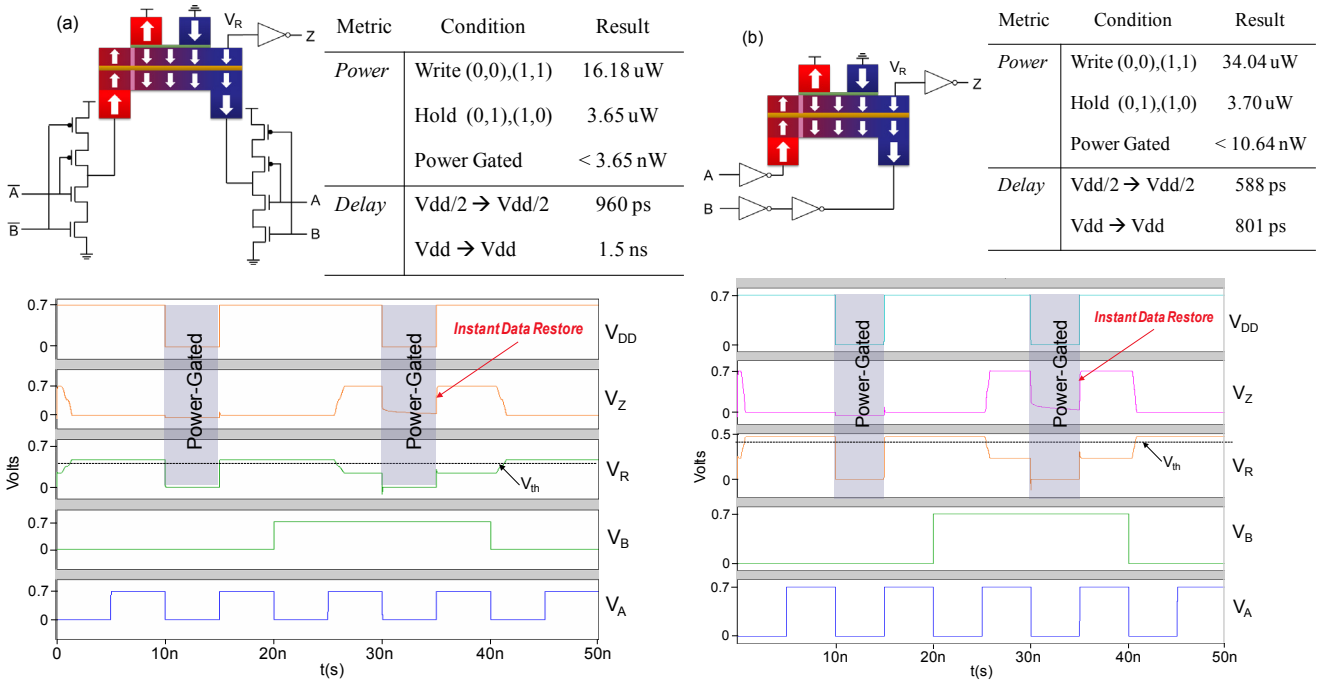
The second design iteration of the spintronic Muller C-Element is shown in Figure 4b. This design operates by using the pMOS or nMOS branches of the inverters driving *A* and *B* to connect the write terminals of the DWCSTT device to either V_{DD} or *GND*. If A and B are (0,0) or (1,1), then a potential difference occurs between the write terminals of the DWCSTT device, which generates a current through the device to change its state. If *A* and *B* are either (0,1) or (1,0), then both write terminals will be either *GND* or V_{DD}, thus eliminating any potential difference necessary to generate current flow.

Table 2: DWCSTT Device Parameters Used Herein

Parameter	Value
Domain Wall Length	32 nm
MTJ Length (each)	12 nm
Device Width	10 nm
Write Path Resistivity	$200\ \Omega nm$
MTJ Parallel Resistance-Area Product	$5 * 10^7\ \Omega nm^2$
Tunneling Magnetoresistance Ratio	100%

A. Simulation and Results

The two design iterations of the spintronic Muller C-Element were implemented with 16nm PTR transistor models [12] in HSPICE. The DWCSTT device was simulated by altering the Verilog-A model of [15] to have opposite fixed reference pillars as well as a *Read Out Terminal* according to the DWCSTT device operation. To elaborate, the original model used in [15] is a compact model encapsulating a first-order approximation of STT-



Metric	Condition	Result
Power	Write (0,0),(1,1)	16.18 uW
	Hold (0,1),(1,0)	3.65 uW
	Power Gated	< 3.65 nW
Delay	Vdd/2 → Vdd/2	960 ps
	Vdd → Vdd	1.5 ns

Metric	Condition	Result
Power	Write (0,0),(1,1)	34.04 uW
	Hold (0,1),(1,0)	3.70 uW
	Power Gated	< 10.64 nW
Delay	Vdd/2 → Vdd/2	588 ps
	Vdd → Vdd	801 ps

Figure 5: Spintronic C-Element designs, functional verification, and performance metrics.

driven domain wall motion empirically-fitted to experimental results [12]. It utilizes separated read and write paths and two MTJ pillars with parallel fixed layers utilizing the read path as the free layer. The DWCSTT device is very similar to this design, the only difference being that the two MTJ pillars have anti-parallel fixed layers, and an additional terminal is provided at the read layer, which is connected to one side of both MTJs. Thus, straightforward minor alterations to the model of [15] are required to realize the DWCSTT functionality without altering the underlying STT-driven domain wall motion model. Namely, it is necessary to modify one MTJ resistance to be configured oppositely of the other with respect to the free layer orientation. Meanwhile, a terminal is connected between the two MTJs. The DWCSTT device parameters utilized herein are listed in Table 2.

The circuits simulated with their corresponding functional verification waveforms and power and delay metrics are shown in Figure 5. For both circuits, V_{DD} is 0.7V, nMOS width is 3F, pMOS width is 6F (where F is the minimum feature size), the TMR is 100%, and the value of R_{Low} used herein is $40k\Omega$. Having a large R_{Low}, which is correlated with the thickness of the oxide layer in the MTJ, minimizes the reading current used in the voltage-divider sensing scheme. Both circuits were also power-gated by turning off V_{DD} for 5 ns when the output is both a logical 0 and logical 1. In both instan ces, when V_{DD} is restored, the correct logical value is restored, demonstrating the simple instant-on/off nature of the circuits. Additionally, V_R, which is the voltage read at the *Read Out Terminal,* is shown to switch above and below V_{Th}, which is the threshold voltage for a 16nm CMOS inverter using PTR models.

Although the first design iteration in Figure 5a showed much lower power consumption than the second design in Figure 5b, the nearly double rail-to-rail swing delay causes the total energy consumption to be similar between the two designs. Since both designs use a comparable amount of energy, however, the second design is nearly twice as fast and reduces the transistor count, it offers several advantages.

In Figure 6, we analyze the relationship between TMR and write power, energy, and delay in order to extrapolate how the spintronic Muller C-Element will benefit with improved MTJ manufacturing techniques, which can improve TMR. For instance, room temperature TMR has been experimentally reported to be as high as 604% [16], with theoretical limits approaching 34,000% [17]. Additionally, in Figure 6, we analyze how the widths of driving transistors, which determine the magnitude of the current through the DWCSTT, affects the performance characteristics of the Muller C-Element. As the TMR is increased, improvements in all performance characteristics are observed due to the greater difference between V_{low} and V_{high} achieved when increasing the TMR. As the driving transistor width is increased, which increases the driving current, write power is increased significantly, delay is decreased significantly until w=3, and then steadily decreases, and write energy is increased.

V. Asynchronous Pipeline Simulations and Results

In this Section, two different asynchronous protocols are implemented and discussed. First a simple 4-bit dual-rail NCL pipeline is implemented with the spintronic Muller C-Element demonstrating functional correctness as well as instant on/off power-gating

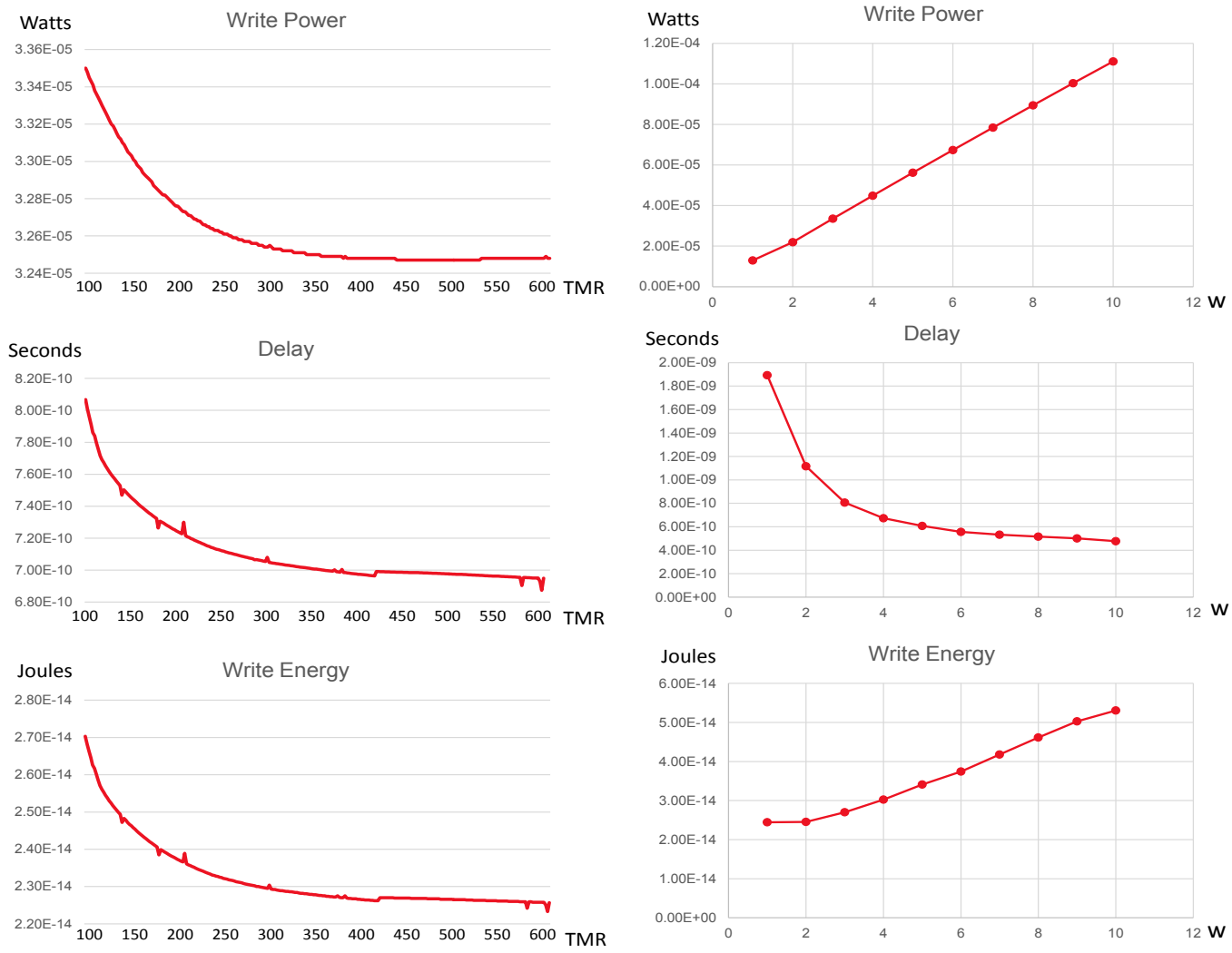


Figure 6: Left side – relation of performance characteristics to TMR. Right side – relation of performance characteristics to driving transistor width (nMOS width = Fw and pMOS with = $2Fw$ where F is the minimum feature size).

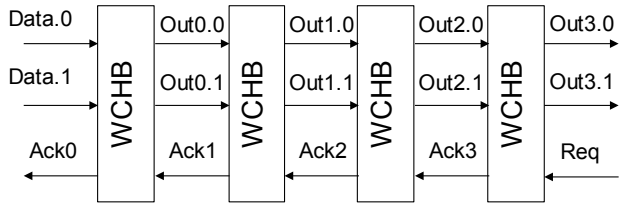
potential. Next, a pipelined 4-bit Ripple Carry Adder is implemented in a Bundled Data fashion to illustrate how the delay of the Spintronic Muller C-Element compared to typical CMOS gate delays can be utilized to reduce circuitry overhead of the local clock generating circuits.

A. Null Convention Logic

In order to demonstrate the functionality and results of the developed Muller C-Element, the asynchronous NCL pipeline shown in Figure 7 is simulated in HSPICE. It consists of a simple FIFO pipeline using WCHBs as the intermediate storage and control. Each WCHB uses two Muller C-Elements with reset control and a two-input NOR gate as shown in Figure 2. The total transistor count for each WCHB is 24, which is 52% fewer transistors than in [1]. The included waveform demonstrates the pipeline handshaking protocol shown in Figure 2, which deterministically ensures correct propagation of data, typically called tokens, between the stages. Since V_{Req} is held low for a period, tokens are only allowed to propagate to the 3rd stage until V_{Req} goes high. Until this happens each stage holds onto its previous token, even after power-gating the entire circuit for 5 ns, demonstrating the NV functionality of the pipeline.

B. Bundled Data

Typical CMOS-only implementations of Bundled Data pipelines require delay elements equating to the delay of the combinational logic to be inserted between the local clock generating Muller C-Elements as shown in Figure 8. By simulating the clocking circuitry using Spintronic Muller C-Elements without any combinational logic, it is determined that the propagation delay between pipeline stages is about 605ps. Additionally, the propagation delay of a two-input NAND gate was found to be about 9ps. By extrapolation, it can be said that up to 67 CMOS gate delays can fit within the delay margin of the Spintronic Muller C-Element, and therefore, it



Metric	Condition	Result
Power	Average	120.83 uW
	Peak	202.95 uW
	Power Gated	39.38 nW
Delay	Token Passing	641 ps

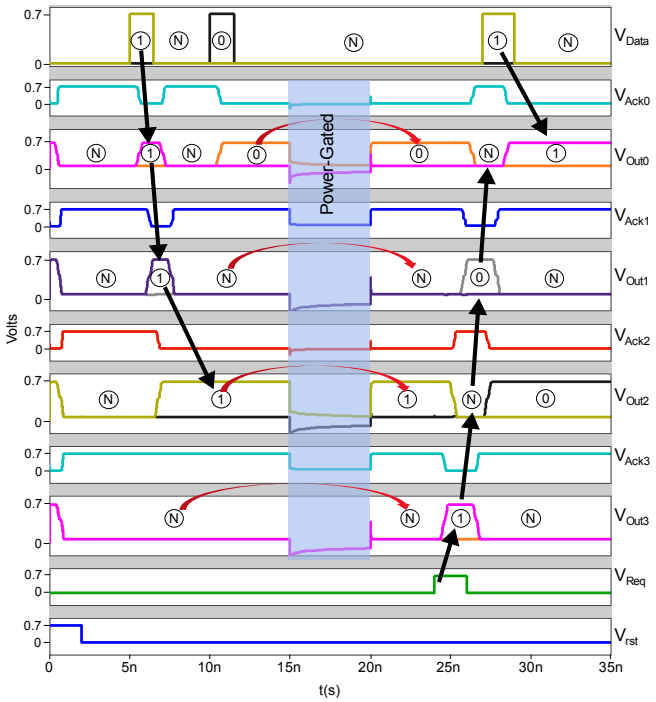


Figure 7: Asynchronous 4-phase dual-rail FIFO pipeline design, performance characteristics, and functional verification showing instant on/off after power gating.

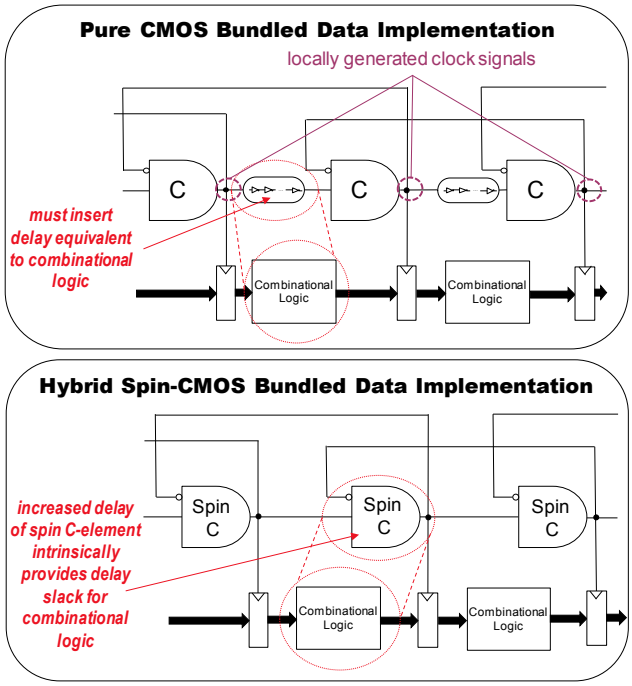


Figure 8: Comparison between pure CMOS and hybrid spin-CMOS bundled data implementations

is not obligatory to insert delay elements between Muller C-Elements, as illustrated in Figure 8. This concept was then simulated with a four-stage pipelined 4-bit ripple carry adder, and it was found to be functionally correct and the had additional delay slack to accommodate larger combinational circuits between pipeline stages. The stage delay for an input pattern of all zeros for both operands was 605 ps, which corresponds to the minimum delay since no carry logic is required. The maximum stage delay for an input pattern of all ones for both operands was about 2.4 ns, which corresponds to the maximum delay since each adder will compute a carry that must be propagated.

VI. Discussion

The approach developed and demonstrated herein provides a novel look at the utilization of non-volatile devices to alleviate the area demands imposed by asynchronous architectures relative to their synchronous counterparts. Energy-sparing benefits are also conferred via instant store and restore features which leverage non-volatility. Even though the DWCSTT device proposed in [10] has yet to be experimentally verified, devices utilizing a similar structure with coupled read and write domain-wall have been fabricated and validated [12]. Additionally, the techniques developed herein could be elaborated further with alternative non-volatile spintronic devices, such as Spin Hall Effect-enhanced switching MTJs. Nonetheless, various non-volatile devices compatible with back-end-of-line fabrication processes can facilitate novel means of mitigating significant area-overheads associated with asynchronous architectures, while providing novel features such as instant store and restore to realize more effective power-gating schemes as demonstrated herein.

VII. Conclusion

Non-volatile spintronic device-based Muller C-Element designs have beneficial characteristics relating to asynchronous architectures. The designs proposed through the course of this paper realizes a compact non-volatile Muller C-Element that's capable of instant on/off functionality with higher speed and lower power compared to previous non-volatile Muller C-Element designs. Additionally, analysis of driving-transistor widths and TMR effects on performance characteristics are detailed. The best performing design was simulated using HSPICE within a four-phase NCL pipeline and demonstrated instant store/restore power-

gating functionality. Furthermore, Bundled Data protocols have been shown to have reduced overheads when using the Spintronic Muller C-Element proposed herein.

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