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# Energy-Efficient and Process Variation-Resilient Write Circuit Schemes for Spin Hall Effect MRAM

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**Abstract**—In this paper, various energy-efficient write schemes are proposed for switching operation of spin Hall Effect (SHE)-based magnetic tunnel junctions (MTJs). A transmission gate (TG)-based write scheme is proposed which provides a symmetric and energy-efficient switching behavior. We have modeled SHE-MTJ using precise physics equations, and then leveraged the model in SPICE circuit simulator to verify the functionality of our designs. Simulation results show the TG-based write scheme advantages in terms of device count and switching energy. In particular, it can operate at 12% higher clock frequency while realizing at least 13% reduction in energy consumption compared to the most energy-efficient write circuits. We have analyzed the performance of the implemented write circuits in presence of process variation in the transistors' threshold voltage and SHE-MTJ dimensions. Results show that the proposed TG-based design is the second most process variation-resilient write circuit scheme for SHE-MTJs among the implemented designs. Finally, we have proposed the 1TG-1T-1R SHE-based magnetic random access memory (MRAM) bit cell based on the TG-based write circuit. Comparisons with several of the most energy-efficient and variation-resilient SHE-MRAM cells indicate that 1TG-1T-1R delivers reduced energy consumption with 43.9% and 10.7% energy-delay product (EDP) improvement, while incurring low area overhead.

**Index Terms**—Magnetic random access memory (MRAM), magnetic tunnel junction (MTJ), spin-based memory cell, spin Hall Effect (SHE) MRAM, write energy, process variation.

## I. INTRODUCTION

RECENTLY, magnetic tunnel junctions (MTJs) have attracted considerable attentions as an alternative for CMOS in both logic and memory [1-3]. MTJ consists of two ferromagnetic (FM) layers, called *Fixed Layer* and *Free Layer*, separated by a thin oxide barrier [4]. The fixed layer is magnetically pinned and utilized as a reference layer, while the free layer magnetic orientation can be modified using various switching approaches. There are two different magnetization configurations for FM layers, *parallel* (P) and *antiparallel* (AP) according to which MTJ resistance is low or high, respectively.

In [5], spin transfer torque (STT) switching technique is proposed for changing the MTJ states. Despite the advantages, the main challenge of STT switching approach is its high dynamic energy consumption. Reducing the energy consumption of the STT-MTJ write operation has been widely researched in recent years [6, 7]. Recently, spin hall effect-based MTJ (SHE-MTJ) is introduced as an alternative for STT-MTJ, which provides separate paths for read and write operations, while expending significantly less switching energy [8-11]. In this paper we concentrate on different write mechanisms for SHE-MTJ devices. In particular, first we implement and analyze five different write circuits. Then, we investigate their performance in presence of process variation.

## II. FUNDAMENTALS AND MODELING OF SHE-MTJ

In [12], the physical equations which describe the three-terminal SHE-MTJ device behavior are provided. Fig. 1 shows the SHE-MTJ, in which the MTJ free layer is directly connected to a heavy metal (HM). The MTJ logic state is determined by the direction of the charge current applied to the write terminals. Ratio of the injected spin current to the applied charge current, spin Hall injection efficiency (SHIE), is defined as below:

$$SHIE = \frac{I_{sz}}{I_{cx}} = \frac{\pi MTJ_{width} MTJ_{length}}{4 HM_{thick} HM_{width}} \theta_{SHE} \left[ 1 - \operatorname{sech}\left(\frac{HM_{thick}}{\lambda_{sf}}\right) \right] \quad (1)$$

where  $\lambda_{sf}$  is the spin flip length in HM, and  $\theta_{SHE}$  is the SHE angle [12]. The critical spin current required for switching the free layer magnetization orientation is expressed by (2), where  $V_{MTJ}$  is the MTJ free layer volume [13]. Thus, SHE-MTJ critical charge current can be calculated using (1) and (2).

$$I_{S,critical} = 2q\alpha M_S V_{MTJ} (H_k + 2\pi M_S) / \hbar \quad (2)$$

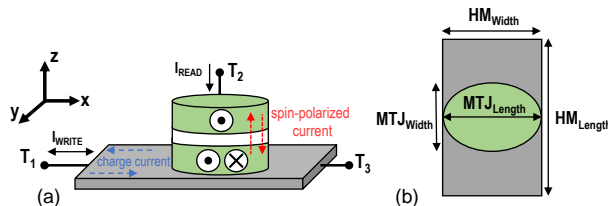


Fig. 1. (a) SHE-MTJ structure. Current along  $+x$  induces a spin injection current  $+z$  direction, producing the spin torque for aligning the magnetic direction of the free layer in  $+y$   $-y$  directions. (b) SHE-MTJ top view.

Equation (3) demonstrates the relation between SHE-MTJ switching time and the voltage applied to the HM terminals with the critical voltage  $v_c$ , which is given by (4).

$$\tau_{SHE} = \frac{\tau_0 \ln(\pi/2\theta_0)}{\left(\frac{v}{v_c}\right) - 1}, \quad \tau_0 = \frac{M_S \cdot HM_{Volume} \cdot q}{I_C \cdot P \cdot \mu_B} \quad (3)$$

$$v_c = 8\rho I_C \left\{ \theta_{SHE} \left[ 1 - \operatorname{sech}\left(\frac{HM_{thick}}{\lambda_{sf}}\right) \right] \pi HM_{length} \right\}^{-1} \quad (4)$$

where  $I_C$  is the critical charge current for spin-torque induced switching. In order to model the SHE-MTJ the HM resistance is also required, which is expressed by below equation, where  $\rho_{HM}$  is the electrical resistivity of HM, i.e.  $\beta$ -tungsten [14].

$$R_{HM} = (\rho_{HM} \cdot HM_{length}) / (HM_{width} \times HM_{thick}) \quad (5)$$

In this paper, we have utilized the approach proposed in [15] to model the behavior of SHE-MTJ device, in which a Verilog-AMS model is developed using the aforementioned equations. Then, the model is leveraged in SPICE circuit simulator to validate the functionality of the designed circuits using experimental parameters listed in Table I.

Fig. 2 shows the conventional 2T-1R SHE-MRAM cell [16, 17] in which one read transistor and one write transistor are utilized to connect the cell's bit line to MTJ and HM, respectively. The three terminal design of the SHE device facilitates the separate current flow paths to isolate its read operations and write operations. This reduces breakdown degradation vulnerability of the MTJ tunneling oxide barrier, since current flow through the oxide is avoided during the higher magnitude current which occurs during write operations.

### III. DESIGN AND ANALYSIS OF SHE-MTJ WRITE CIRCUITS

In this section, various write circuits are investigated for switching the states of SHE-MTJ devices. A comprehensive comparison of the different write circuits developed and examined in this paper is provided in Table II. The implemented write circuits are either proposed herein or inspired by previously proposed write circuits that are modified in this work to be capable of: (1) operating with an input clock signal, (2) producing a bidirectional current to enable switching the SHE-MTJ states from  $P$  to  $AP$  and vice versa. All the write circuits are simulated by SPICE circuit simulator in 90nm library using 1.2V nominal voltage. Herein, to provide a fair comparison, the minimum technology feature size is used for the gate channel width of the transistors. Critical charge current,  $I_C$ , for the SHE-MTJ is equal to  $108\mu A$ , which is obtained using (1) and (2).

#### A. Current Mirror Circuit Approaches

Herein, we have designed two different current mirror circuits based on the designs introduced in [18] and [19], which are shown in Fig. 3(a) and 3(b), respectively. Simulation results listed in Table II show that current mirror designs have asymmetric switching behavior, i.e. the produced current amplitude for switching from  $P$  to  $AP$  states is different from the current amplitude generated for  $AP$  to  $P$  switching. Therefore, in the current mirror-based designs the worst case condition must be considered for clocking scheme to ensure correct switching. Moreover, the implemented current mirror-based write circuits, CM-1 and CM-2, cannot

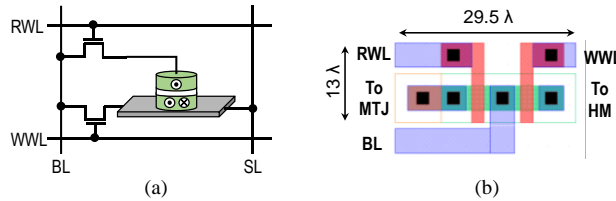


Fig. 2. (a) Conventional 2T-1R bitcell. (b) 2T-1R bitcell layout view.

TABLE I: PARAMETERS OF SHE-MTJ.

Parameter	Description	Value
$HM_{Volume}$	$HM_{Length} \times HM_{Width} \times HM_{Thickness}$	100 nm $\times$ 60 nm $\times$ 3 nm
$MTJ_{Area}$	$MTJ_{Length} \times MTJ_{Width} \times \pi/4$	60nm $\times$ 30nm $\times$ $\pi/4$
$\alpha$	Gilbert Damping factor	0.007
$P$	Spin Polarization	0.52
$M_S$	Saturation magnetization	7.8e5 A $\cdot$ m <sup>-1</sup>
$H_k$	Anisotropy Field	80 Oe
$\theta_{SHE}$	Spin Hall Angle	0.3
$\mu_B$	Bohr Magneton	9.27e-24 J $\cdot$ T <sup>-1</sup>
$\rho_{HM}$	HM Resistivity	200 $\mu\Omega$ .cm
$q$	Electric charge	1.602e-19 C
$\lambda_{sf}$	Spin Flip Length	1.5nm
$\hbar$	Reduced Planck's Constant	6.626e-34/2 $\pi$ J.s

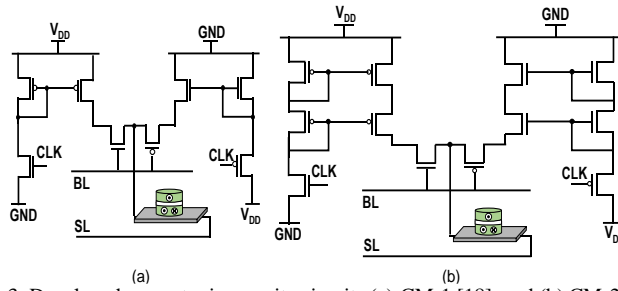


Fig. 3. Developed current mirror write circuits (a) CM-1 [18], and (b) CM-2 [19].

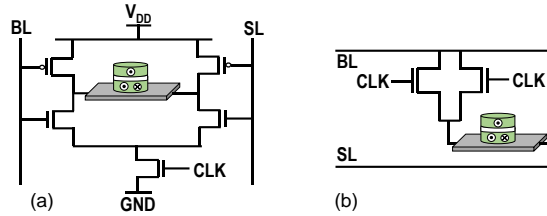


Fig. 4. Energy-aware write circuits inspired by the designs proposed by Ben-Romdhane et al. in [18], b) Gupta et al. in [21].

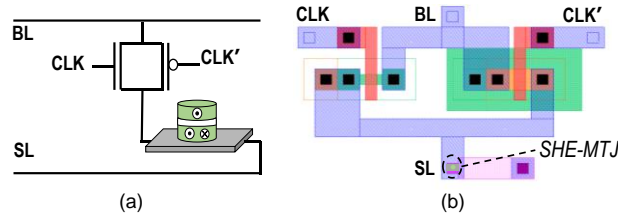


Fig. 5. (a) Transmission gate-based write circuit. (b) TG-based write circuit layout view.

produce the required critical current to ensure switching, i.e.  $108\mu\text{A}$ . Two solutions for the mentioned drawbacks are enlarging the channel width of the transistors and adding a reference current source to the circuit structure. Both of the mentioned approaches can result in a significant increase in the switching power consumption. Thus, these solutions are more appropriate for larger designs such as cache line drivers [20].

### B. Previous Energy-Aware Write Circuits

Fig. 4(a) shows a SHE-MTJ write circuit implementation inspired by the switching circuit proposed in [18] for Racetrack memory, which is equipped with a clocking mechanism herein. Advantages of the proposed circuit are its fully symmetric behavior, in addition to the fewer number of transistors utilized in its structure. However, as listed in Table I, the produced current amplitude is  $54.08\mu\text{A}$ , which is smaller than the critical current. Thus, this write scheme with transistors having minimum feature size cannot ensure the SHE-MTJ switching.

As listed in Table II, the conventional 2T-1R SHE-MRAM layout with a single write transistor produces  $I_{P-AP}=90.41\mu\text{A}$  and  $I_{AP-P}=79.43\mu\text{A}$  using the minimum transistor geometries that are possible by 90nm MOSFET technology. Since the produced write currents are smaller than SHE-MTJ critical current, we have leveraged another NMOS transistor to increase the write current, as inspired by the 2T-1R layout proposed by Gupta et al. in [21] for STT-MRAM. Fig. 4(b) depicts a write circuit that utilizes two NMOS transistors which are electrically connected in parallel configuration, both of which are ON during the write operation leading to a high switching current. The drawback of this write circuit is its highly asymmetric behavior. As it is listed in Table II, the produced current amplitude for switching from  $P$  to  $AP$  ( $I_{P-AP}=177.8\mu\text{A}$ ) is different from the current amplitude generated while switching from  $AP$  to  $P$  state ( $I_{AP-P}=139.9\mu\text{A}$ ). Consequently, the clocking schemes should be always considered for the worst case scenario to ensure the complete switching, which increases the average energy consumption.

### C. TG-based Write Circuit

In this paper, we propose utilizing transmission gates (TGs) in the SHE-MTJ write circuit, as shown in Fig. 5(a). The asymmetry between the write circuits is caused primarily by the different drive strengths of the PMOS and NMOS transistors. TGs are characterized by near-optimal full-swing switching behavior, since both of the NMOS and PMOS transistors are ON during the write operation, and contributing to the drive strength. We have leveraged this feature of TGs within the write circuit, incurring a symmetric switching operation without increasing the design complexities of matching PMOS and NMOS drive strengths. Results provided in Table II shows that TG-based write circuit provides a symmetric switching with a high amplitude current that ensures

TABLE II: SWITCHING CHARACTERISTICS IN ABSENCE OF CLOCKING LIMITATIONS. (SHE-MTJ CRITICAL CURRENT=108 $\mu$ A).

Features	2T-1R	Current Mirror		Ben-Romdhane	Gupta et al.	TG-based
	[16, 17]	CM-1 [18]	CM-2 [19]	et al. [18]	[21]	Write Circuit
<i>P</i> Current ( $\mu$ A)	90.41	49.57	12.92	54.08	177.8	157.2
to <i>AP</i> Delay (ns)	NA*	NA*	NA*	NA*	1.65	1.9
<i>AP</i> Power ( $\mu$ W)	108.5	120.3	15.49	64.9	213.38	188.68
<i>AP</i> Current ( $\mu$ A)	79.43	55.58	40.47	54.08	139.9	157.1
to <i>P</i> Delay (ns)	NA*	NA*	NA*	NA*	2.18	1.9
<i>P</i> Power ( $\mu$ W)	95.31	135.2	48.56	64.9	167.89	188.56
Symmetric	NO	NO	NO	YES	NO	YES

\* Produced current amplitude is smaller than critical current, thus SHE-MTJ state transduction cannot be ensured.

TABLE III: WRITE CHARACTERISTICS WITH CLOCKING REQUIREMENTS.

Features	Gupta et al. [21]	1TG-1R
Maximum CLK Frequency	220 MHz	250 MHz
Switching Energy (fJ)	P to AP AP to P	484.95 381.57
Average Energy Improvement	—	13%

a high speed switching. Fig. 5(b) shows the TG-based write circuit layout view. Although, TG-based designs necessitate the availability of both CLK and inverse CLK' signals, it is reasonable to assume access to both signal conditions within typical integrated circuits.

Table III provides a comparison between the TG-based write circuit and the write schemes inspired by the Gupta et al. [21] 2T-1R layout, both of which can produce a bidirectional current with an amplitude greater than the SHE-MTJ critical current. Assuming the typical 50% duty cycle, the maximum operating clock frequency based on which each of the circuits can ensure complete switching of the MTJ states are listed in Table II. 1TG-1R write circuit can operate at 12% higher clock frequency, while realizing at least 13% average energy reduction compared to 2T-1R write circuit.

#### IV. PROCESS VARIATION ANALYSIS

In this section, the effect of process variation (PV) on the proposed SHE-MTJ write circuits are investigated. The results shown in Section III are obtained by using the transistors with minimum feature size enabled by the 90nm technology, while higher switching currents can be generated by enlarging the write circuit transistors' size at the expense of higher power consumption. Since, the focus of this section is on the PV effects, we have sufficiently enlarged the transistors' width of the developed write circuits to generate the required current amplitude ensuring the complete switching. Figures 6(a) and 6(b) show the produced write current versus the transistors' size for *AP* to *P*, and *P* to *AP* switching, respectively. Moreover, Tables IV lists the write delay and power consumption as a function of transistor size, both of which are important metrics for the investigated write schemes.

Herein, we have modeled two types of process variation which have the most impact on the produced write current; (1)  $\sigma HM$ : variations in the HM dimensions, and (2)  $\sigma V_{th}$ : fluctuations in the threshold voltages ( $V_{th}$ ) of the transistors. Figures 7(a), 7(b), and 7(c) show the produced write current fluctuation versus  $\sigma HM$  for a given  $\sigma V_{th}$ . As it can be seen in Fig. 6(a), although the Gupta et al. [21] write circuit is the second most energy efficient design introduced herein, it is significantly susceptible to the variations in the HM dimensions. As it is shown in Fig. 7(c), for  $\sigma V_{th}=5\%$  the highest write current variation is associated with the current mirror write circuit CM-2, while its produced write current varies insignificantly for different  $\sigma HM$  values. Thus, it can be inferred that the high write current variation of the CM-2 write circuit is mainly induced by the  $V_{th}$  variations of MOS transistors, making CM-2 the most susceptible write circuit design to  $\sigma V_{th}$ .

To examine the impact of the  $V_{th}$  variations on implemented write circuits, the write current amplitude fluctuations for

TABLE IV: PERFORMANCE OF THE WRITE SCHEMES AS A FUNCTION OF TRANSISTOR SIZE.

Designs	Width/90nm Ratio							
	MOS=1 $\times$		MOS=2 $\times$		MOS=3 $\times$		MOS=4 $\times$	
	Power ( $\mu$ w)	Delay (ns)	Power ( $\mu$ w)	Delay (ns)	Power ( $\mu$ w)	Delay (ns)	Power ( $\mu$ w)	Delay (ns)
<i>P</i> CM-1 [18]	120.3	NA*	181.47	NA*	238.2	2.04	288.85	1.53
<i>P</i> CM-2 $\Psi$ [19]	15.49	NA*	48.05	NA*	65.05	NA*	82.02	NA*
to Ben-Romdhane et al. [18]	64.9	NA*	134.54	2.89	200.84	1.78	264.7	1.3
<i>AP</i> Gupta et al. [21]	213.38	1.65	430.24	0.76	627.2	0.51	796.28	0.4
<b>TG-based Write Circuit</b>	<b>188.68</b>	<b>1.9</b>	<b>342.86</b>	<b>0.98</b>	<b>463.3</b>	<b>0.71</b>	<b>562.17</b>	<b>0.57</b>
CM-1 [18]	55.58	NA*	201.4	2.9	262.58	1.84	316.6	1.39
<i>AP</i> CM-2 [19]	40.47	NA*	98.17	NA*	146.3	2.57	192.9	1.85
to Ben-Romdhane et al. [18]	64.9	NA*	134.54	2.89	200.84	1.78	264.7	1.3
<i>P</i> Gupta et al. [21]	167.89	2.18	280.1	1.22	353.5	0.95	405.94	0.81
<b>TG-based Write Circuit</b>	<b>188.56</b>	<b>1.9</b>	<b>334.77</b>	<b>1</b>	<b>442.56</b>	<b>0.74</b>	<b>525.6</b>	<b>0.62</b>

\* Produced current amplitude is smaller than critical current, thus SHE-MTJ state transduction cannot be ensured.

$\Psi$  The size of the transistors within CM2 write schemes should be enlarged 10-fold to produce a current amplitude greater than critical current (139.6 $\mu$ A>108 $\mu$ A) resulting in 183.3 $\mu$ W write power and 2.19ns write delay

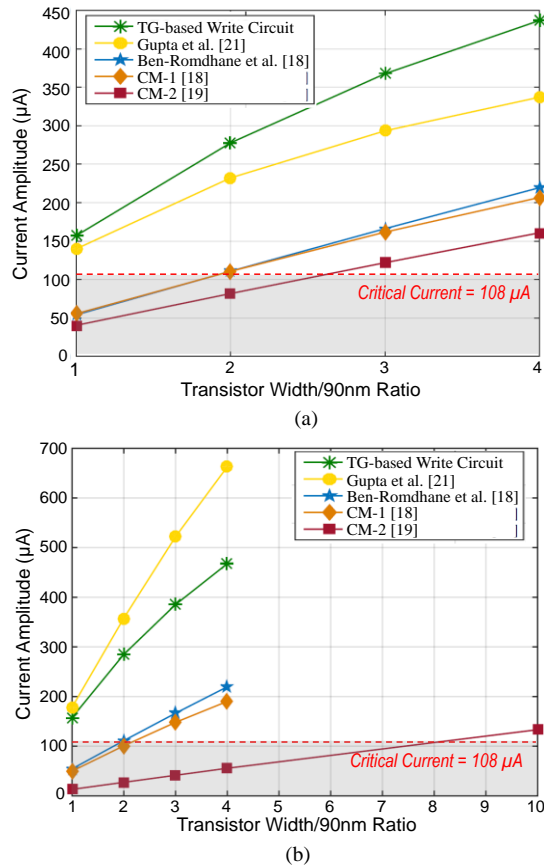


Fig. 6. Produced switching current versus the size of the transistors' width for (a) AP to P switching, and (b) P to AP switching.

various  $\sigma V_{th}$  values are measured for a given  $\sigma HM$ , as shown in Fig. 7(d-g). The significant increase in the produced write current variations for the current mirror circuits, CM-1 and CM-2, show their higher susceptibility to the  $V_{th}$  variations, which is mainly caused by the larger number of transistors utilized in their design. Moreover, the Ben-Romdhane et al. [18] and proposed TG-based write circuits are shown to be the most resilient designs to the  $V_{th}$  fluctuations. Fig. 7(g) shows the write current variation for the worst case scenario investigated herein, i.e.  $\sigma HM=20\%$  and  $\sigma V_{th}=5\%$ . The proposed TG-based write circuit shows 4.33% worst-case variation in the produced write current, making it the second most variation-resilient SHE-MTJ write circuit design after the Ben-Romdhane et al. [18] write circuit with 2.31% worst-case variation.

Thus far, we have considered two types of variations that have substantial impact on the production of write current, while the

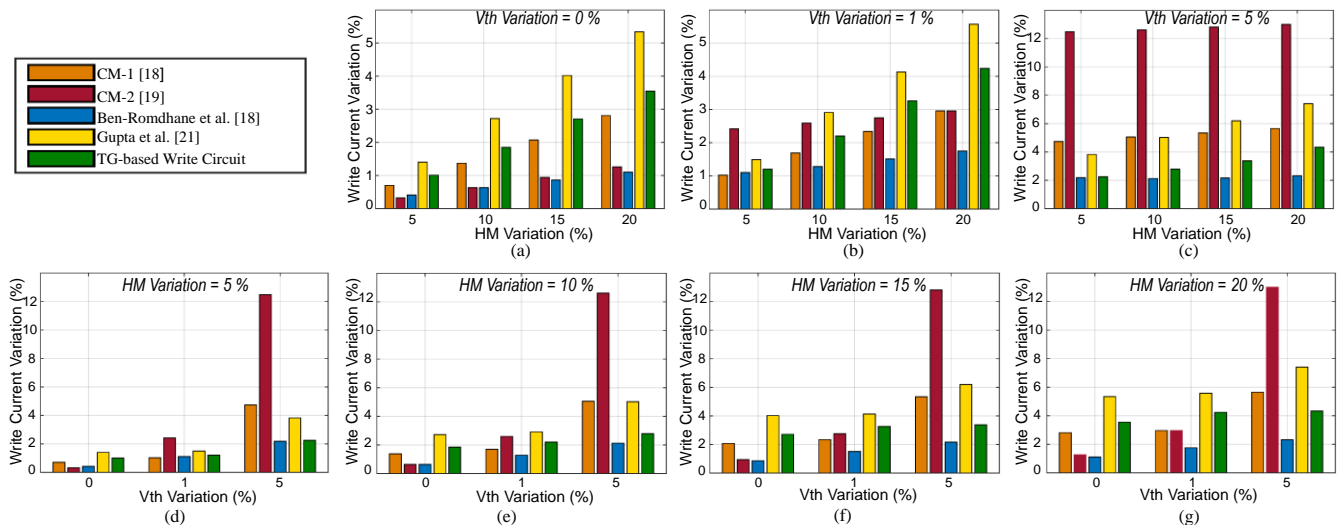


Fig. 7. Write current variations: (a) versus  $\sigma HM$  for  $\sigma V_{th}=0\%$ , (b) versus  $\sigma HM$  for  $\sigma V_{th}=1\%$ , (c) versus  $\sigma HM$  for  $\sigma V_{th}=5\%$ , (d) versus  $\sigma V_{th}$  for  $\sigma HM=5\%$ , (e) versus  $\sigma V_{th}$  for  $\sigma HM=10\%$ , (f) versus  $\sigma V_{th}$  for  $\sigma HM=15\%$ , (g) versus  $\sigma V_{th}$  for  $\sigma HM=20\%$ .

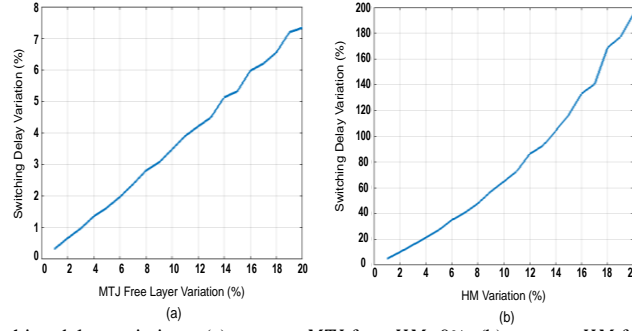


Fig. 8. Switching delay variations: (a) versus  $\sigma_{MTJ}$  for  $\sigma_{HM}=0\%$ , (b) versus  $\sigma_{HM}$  for  $\sigma_{MTJ}=0\%$

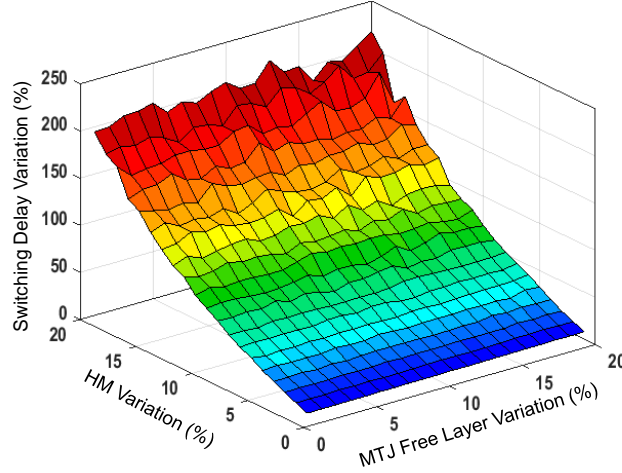


Fig. 9: Switching delay variations versus  $\sigma_{MTJ}$  and  $\sigma_{HM}$ .

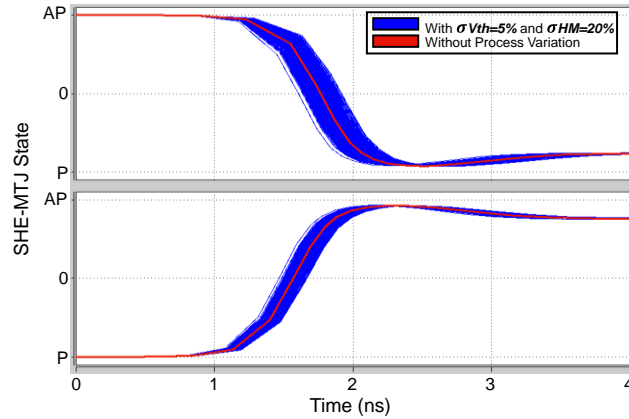


Fig. 10. Monte-Carlo simulation of TG-based write circuit for switching SHE-MTJ device (top) from AP to P, and (bottom) from P to AP.

variations in MTJ free layer ( $\sigma_{MTJ}$ ) can also influence the switching performance. Variations in the MTJ free layer do not affect the produced write current and only impact the switching delay regardless of the write circuit utilized. Based on these effects, herein we investigate the effect of  $\sigma_{MTJ}$  on switching delay using the proposed TG-based write circuit without loss of generality. MTJ free layer variation affects the spin injection efficiency and critical spin current according to (1) and (2), respectively, which can alter the switching delay. Fig. 8 (a) shows that the switching delay and  $\sigma_{MTJ}$  are linearly proportional with a mild slope, while  $\sigma_{HM}$  is fixed to zero. Moreover, HM variation also has significant effect on critical switching current, as well as the produced write current. Fig. 8(b) depicts the fluctuations in switching delay versus  $\sigma_{HM}$  without any variations in the MTJ free layer. Finally, Fig. 9 depicts the switching delay variations for various  $\sigma_{MTJ}$  and  $\sigma_{HM}$  values ranging from 0% to 20%. As it can be seen in the figure, switching delay can be approximately doubled for the worst case scenario considered herein, i.e.  $\sigma_{MTJ}=20\%$  and  $\sigma_{HM}=20\%$ .

To assess the transient behavior of SHE-MTJ switching in presence of process variations in  $HM$  size and  $V_{th}$ , a Monte-Carlo simulation is utilized in SPICE along with the SHE-MTJ model developed by Camsari et al. in [22]. Figure 7 shows the Monte-

TABLE V: WRITE CHARACTERISTICS FOR VARIOUS SHE-MRAM BIT CELLS.

Features		7T-1R	3T-1R	1TG-1T-1R
$P$	Current ( $\mu\text{A}$ )	166.2	358.16	<b>284.3</b>
$t_0$	Delay (ns)	1.78	0.76	<b>0.98</b>
$AP$	Power ( $\mu\text{W}$ )	199.7	430.04	<b>359.85</b>
$AP$	Current ( $\mu\text{A}$ )	166.2	241.18	<b>271.9</b>
$t_0$	Delay (ns)	1.78	1.17	<b>1.03</b>
$P$	Power ( $\mu\text{W}$ )	199.7	289.66	<b>344.94</b>
Maximum CLK Frequency (MHz)		280	425	<b>485</b>
Average Energy (fJ)		356.6	423.2	<b>363</b>
Energy-Delay Product (EDP) (fJ $\times$ ns)		634.75	408.39	<b>364.81</b>
Average EDP Improvement		7T-1R	35.6%	<b>43.9%</b>
		3T-1R	—	<b>10.7%</b>
Normalized Area Compared to 2T-1R		10.1	1.25	<b>2.88</b>

Carlo simulation of 1TG-1R write circuit for switching SHE-MTJ device in presence of 5% and 20% process variation in transistors'  $V_{th}$  and HM dimensions, respectively. The results are obtained for 10,000 simulation points. The effect of the process variation on the write current amplitude and in consequence of which on switching delay is shown in Fig. 10.

## V. SPIN-HALL EFFECT MRAM BASED MEMORY

Up to this point, we have investigated various SHE-MTJ write schemes, which can be utilized for both logic and memory applications. The obtained results have provided a meaningful comparison between the introduced write circuits. However, additional attributes should be considered for leveraging the write circuits within a SHE-based magnetic random access memory (SHE-MRAM) bit cell. Therefore, in this section, we have focused on the bit cell circuit and layout design considerations, as well as the effect of Source Line (SL), Bit Line (BL), and Word Line (WL) drivers on the write performance. Herein, we have utilized a chain of four inverters to drive BL, SL, and WL, in which each successive inverter is twice as large as the previous one. We have only leveraged the three most energy-efficient and variation-resilient write circuits examined in Section III and IV. The current mirror circuits are excluded from the analyses, due to their high energy consumption and susceptibility to  $V_{th}$  variations. Table V provides a detailed comparison of various SHE-MRAM memory cells developed and examined in this paper, in which the effect of line drivers is included for a meaningful comparison. The normalized area consumption of the proposed SHE-MRAM cells compared to the conventional 2T-1R cell is also listed in the last row of Table V.

Fig. 11 shows a 7T-1R bitcell that is designed based on the write circuit introduced in Ben-Romdhane et al. [18] requiring two read transistors and 5 write transistors. As it is shown in Fig. 6, the size of the write transistors should be tripled in this design to produce a write current greater than switching critical current leading to a significant area overhead as shown in Table V. A 3T-1R SHE-MRAM bitcell structure is shown in Fig. 12, which is inspired by the write circuit proposed by Gupta et al. [21]. The schematic and layout of our proposed TG-based SHE-MRAM bitcell is shown in Fig. 13, which includes one TG for write and one transistor for read operation (1TG-1T-1R). To provide a comparable configuration, we have also tripled the size of the transistors

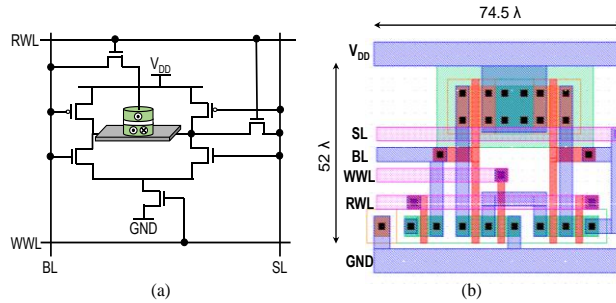


Fig. 11. (a) 7T-1R bitcell. (b) 7T-1R bitcell layout view.

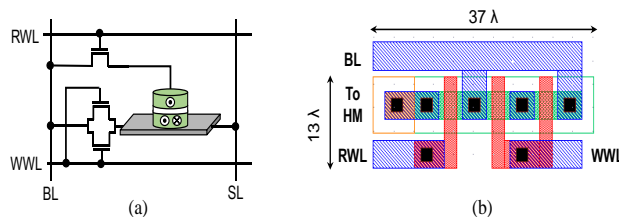


Fig. 12. (a) 3T-1R bitcell. (b) 3T-1R bitcell layout view.



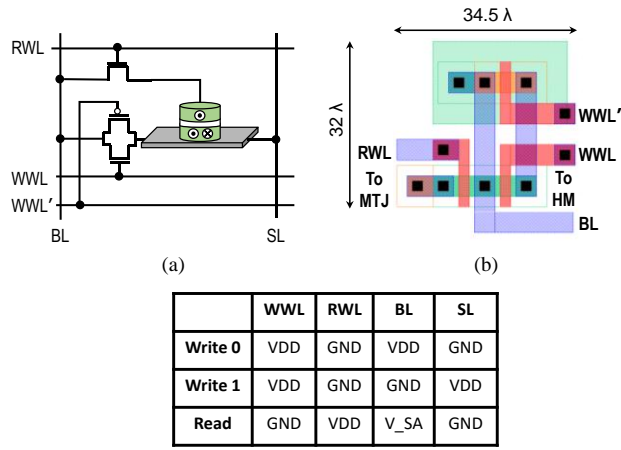


Fig. 13. (a) 1TG-1T-1R bitcell. (b) 1TG-1T-1R bitcell layout view. (c) Required signaling for 1TG-1T-1R SHE-MRAM cell.

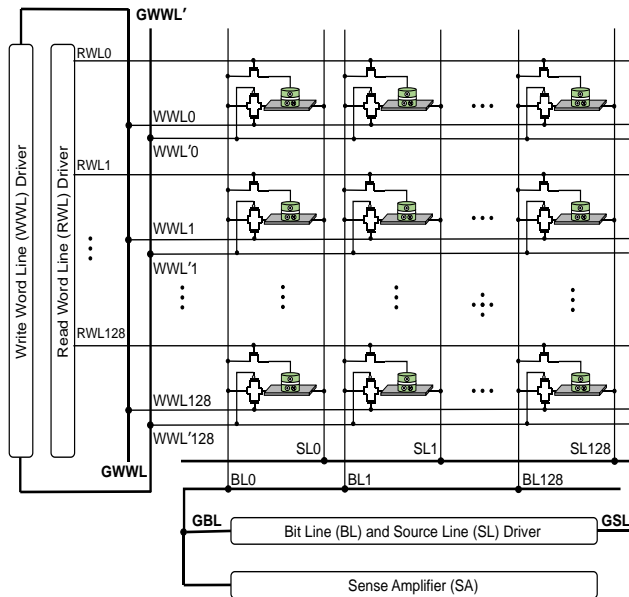


Fig. 14. 128x128 memory array constructed by the 1TG-1T-1R structure.

TABLE VI: QUALITATIVE COMPARISON BETWEEN SHE-MRAM BITCELLS.

Parameter	7T-1R	3T-1R	1TG-1T-1R
Energy Efficiency	✓✓	✓	✓✓
Process Variation Resiliency	✓✓	-	✓✓
Area Efficiency	-	✓✓	✓

utilized in 3T-1R and 1TG-1T-1R structures to obtain the results listed in Table V. As it is shown in Fig. 11, the 7T-1R bitcell has a completed current path from VDD to GND via the transistors and the HM. Since the BL and the SL are electrically isolated from the current path, the strengths of the BL and SL drivers do not need to be considered for the write operation. While, the 3T-1R and proposed 1TG-1T-1R structures do not have a completed current path. Since the polarities of the BL and SL need to be changed, additional write drivers should be connected to the both BL and SL. Hence, as it is listed in Table V, the 7T-1R structure is one of the most energy efficient designs, although it incurs significant area overhead. Moreover, delivering VDD to each bitcell within the memory array could be challenging, which is ignored in our analysis. The qualitative comparison provided in Table VI elaborates that our proposed 1TG-1T-1R bit cell is one of the energy-efficient designs with improved energy-delay product (EDP) values, as listed in the tenth row of the Table V, while being the second most variation-resilient and area-efficient design after the 7T-1R and 3T-1R bit cell designs, respectively. Fig. 14 shows a 128x128 memory array that is constructed by the proposed 1TG-1T-1R structure.

## VI. CONCLUSION

In this paper, we developed a symmetric energy-efficient TG-based write scheme for SHE-based MTJ devices. A SHE-MTJ Verilog-A behavioral model was leveraged via SPICE circuit simulations to validate the functionality of the designed circuit using experimental parameters. Various write schemes were developed and equipped with clocking mechanism to produce the required bidirectional current for SHE-MTJ switching. Simulation results exhibit symmetric behavior of the proposed TG-based write circuit. Comparisons with various write schemes indicated that TG-based design excels in terms of switching delay and energy. In particular, the proposed TG-based write scheme was shown to be able to operate at 12% higher clock frequency, and achieved over 13% energy improvement compared to the next most energy-efficient design. We have investigated the functionality and performance of implemented write circuits in presence of process variation in the transistors' threshold voltage and SHE-MTJ dimensions. The obtained results showed that the proposed TG-based design is the second most process variation-resilient SHE-MTJ write circuit among the implemented designs, allowing appropriate energy versus PV tradeoffs. Finally, we have leveraged three of the most energy-efficient and PV-resilient write circuits within a memory bit cell, and investigated their energy and area tradeoffs. Obtained results exhibit that our proposed 1TG-1T-1R SHE-MRAM bit cell excels in term of energy-delay product (EDP), while incurring low area overhead.

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