Jemal Abawajy
Sabah Mohammed
Ronnie D. Caytiles
Yvette E. Gelogo(Eds.)

Advanced Signal Processing

International Conference, ASP 2012
March 30-31, 2012
Olympic Parktel, Seoul, Korea
Conference Proceedings



Abstract: Area-Efficient Fault-Handling for Survivable Signal-Processing Architectures

Naveed Imran[1], Jooheung Lee*[2], Youngju Kim[2], Mingjie Lin[1], and Ronald F. DeMara[1]
[1]*Department of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL, 32816 USA*
naveed@knights.ucf.edu, mingjie@eecs.ucf.edu, demara@mail.ucf.edu
[2]*Department of Electronic and Electrical Engineering, Hongik University, Korea*
joolee@hongik.ac.kr, yjkim1@hongik.ac.kr

Abstract

We propose an area-efficient dynamic fault-handling approach to achieve high survivability for DSP circuits. Its benefits include requiring only a uniplex instance of the datapath, which has been partitioned into N + 1 Processing Elements (PEs) where N is the number of PEs utilized for fault-free throughput. Fault detection, isolation, and recovery are performed using discrepancy information derived from the existing functional throughput by reconfiguring one of the N + 1 Partially Reconfigurable Regions (PRRs) to replicate each of the N modules in succession. This differs significantly from the conventional approaches that heavily rely on static temporal/spatial redundancy and sophisticated error prediction/estimation techniques. The principal space complexity metric is the additional physical resources utilized to support the underlying fault-handling mechanism where a single PRR can check the health of multiple distinct functional blocks, by leveraging the property of dynamic partial reconfiguration. We demonstrate this approach by implementing a video encoder's DCT block with a Xilinx Virtex-4 device and also numerically simulating a Canny Edge Detector. Results clearly demonstrate the recovery of functionality lost due to randomly injected simulated stuck-at faults using only throughput data values rather than additional test vectors. Using a modular PE design, the area overhead of providing fault-handling capability was 12.5% for the DCT Block and 10% for the Canny edge detector. Moreover, the module granularity can be varied to accommodate tradeoffs of fault detection latency versus fault isolation specificity, as desired by the DSP circuit designer.