Glitch Power Reduction for Low Power IC Design

N. Weng[1], J.S. Yuan[1], Scott C. Smith[1], R. Demara[1], D. Ferguson[2], and M. Hagedorn[2]
[1]Chip Design and Reliability Laboratory, University of Central Florida, Orlando, FL 32816
tel: (407)823-5719, fax: (407)823-5835, email: yuanj@mail.ucf.edu
[2]Theseus Logic, Inc., 3501 Quadrangle Blvd., Suite 100, Orlando, FL 32817

Abstract: **Glitch power of a NCL multiplier is studied. The hysteresis threshold gates eliminate spurious power glitches significantly. The supply voltage signal bounce of the NCL circuit is also reduced drastically compared to its Boolean counterpart.**

1   Introduction

Because of the rapid growth of portable electronics, high density integrated circuits with low energy consumption and low electromagnetic interference (EMI) at high speeds are needed. It is well known that dynamic power dissipation is directly related to the number of the signal transitions in the circuit. Functional signal transitions are desirable, where spurious transitions (or glitches), caused by unequal propagation delays of input signals to the gate, are not desirable. Glitches multiply as they propagate through a combinational logic block and could occupy 20 to 70 percent of signal transitions [1]. In Boolean design, gate sizing and gate registration are used to reduce glitches. However, these techniques are delay sensitive and cannot truly eliminate glitches due to unequal propagation delays of input signals resulting from layout parasitics in deep submicron CMOS technology.

In this paper, we propose the use of the NULL Convention Logic (NCL) threshold gates and NCL design paradigms to eliminate spurious signal transitions. A 4 bit by 4bit multiplier is designed for the evaluation of glitch power and signal bounce from supply voltage variation. The effect of voltage scaling on the clockless circuit is also evaluated.

2   NULL Convention Logic

NCL, patented by Theseus Logic, Inc., integrates control within the data path [2]. A combination of NCL threshold gates and NCL design paradigms ensures delay insensitivity. The design paradigms include monotonic data transitions, mutual exclusive assertion groups (MEAGs), completion of DATA, and completion of NULL. NCL is inherently robust and reliable against temperature, process, and voltage variations. This enables NCL circuits run faster

when the conditions are favorable, while the circuits will still be functionally correct under adverse conditions. On the other hand, clocked designs must be developed for the worst case condition, and generally operate at the worst case rate condition.

The fundamental building blocks of NCL are threshold M-of-N gates with hyteresis [3]. The operation of a threshold M-of-N gate is described as follows. For the positive threshold gate logic, if the initial output state is "0", the gate requires at least M inputs "1" before asserting "1" on its output. Once the output asserts "1", it will remain at the "1" state until all N inputs become "0" [4]. In NCL design, all glitches are eliminated because of monotonic data transitions and completion of DATA and NULL. In addition, NCL circuits operate with alternating wavefronts of DATA and NULL. The randomly distributed switching activities of clockless NCL circuits spread the power spectrum on the power bus, thus reducing noise spikes and EMI.

3 NCL Multiplier Design

Figure 1 shows a 4x4 multiplier designed using NCL. In Fig. 1 FA represents a full adder, HA represents a half adder, and COMP represents the completion circuitry. In addition, 8 bit, 12 bit, and 13 bit NCL registers are used in the pipelined multiplier to improve throughput.
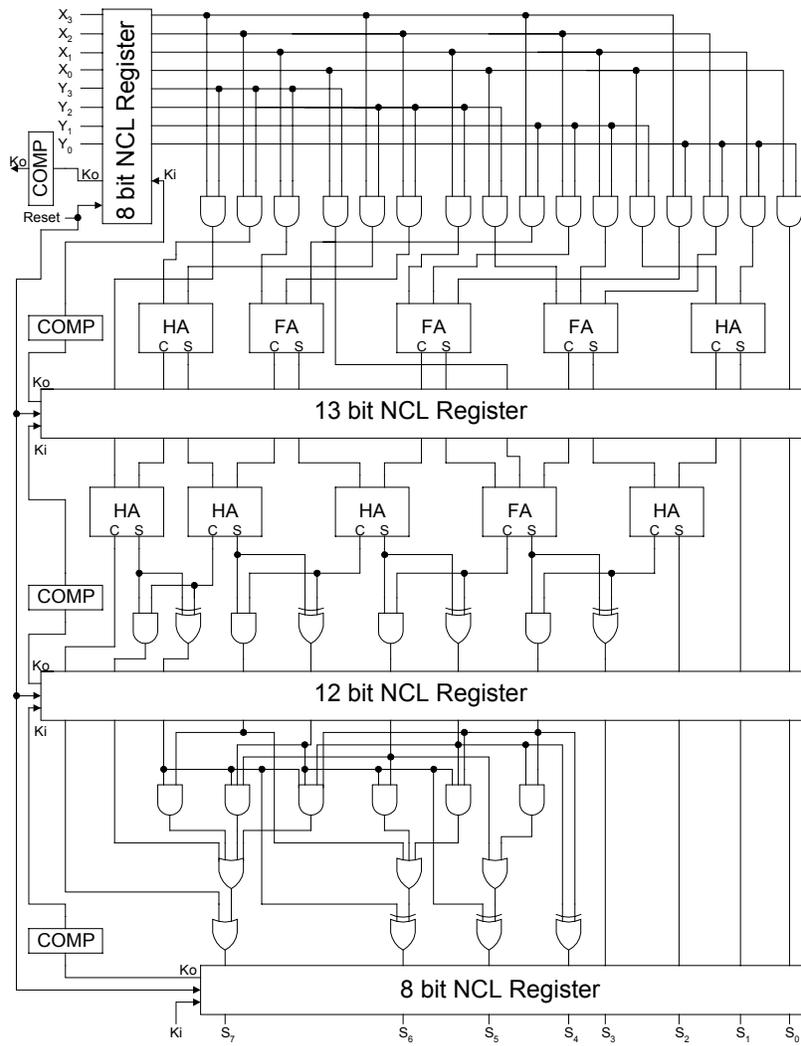
Fig. 1. 4x4 NCL multiplier

4   Power Evaluation Technique

To accurately determine the power dissipation of the NCL multiplier, the test bench circuit shown in Fig. 2 is adopted. An 8 bit timer (counter) is connected to the input of the multiplier. The output of the multiplier is connected to a detection circuit. The timer starts from 00000000, generating 256 possible DATA input combinations as well as the intermediate NULL inputs. Detecting circuit functions only when the output of the multiplier changes. It acknowledges
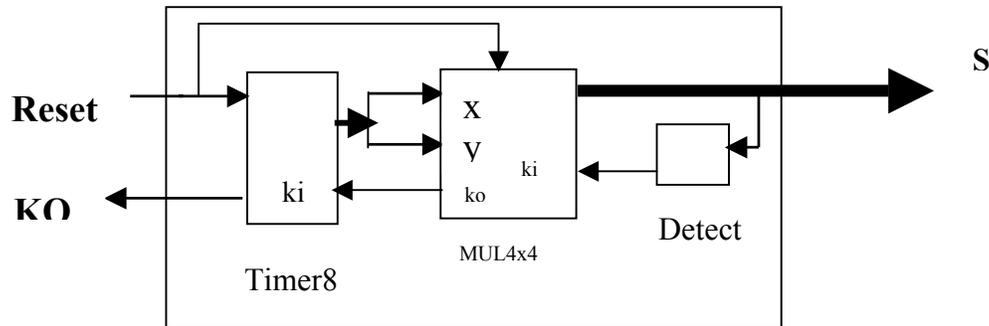
Fig. 2 Self-timed multiplier

complete DATA and NULL outputs and requests the next NULL and DATA output, respectively. The schematics of the timer is shown in Fig. 3 below.
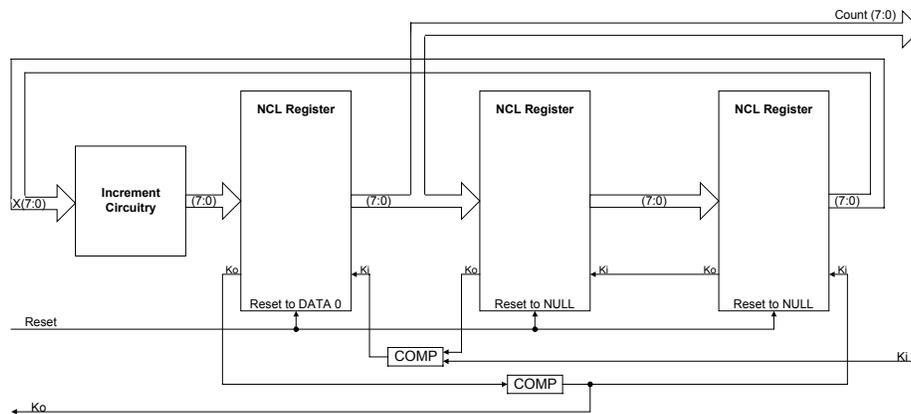
Fig. 3 NCL 8-bit timer using three stages register

5   Results and Discussions

The NCL multiplier is simulated in Cadence SPICE using the 0.18 μm CMOS technology models from TSMC. The simulated power current wavforms are shown in Fig. 4.
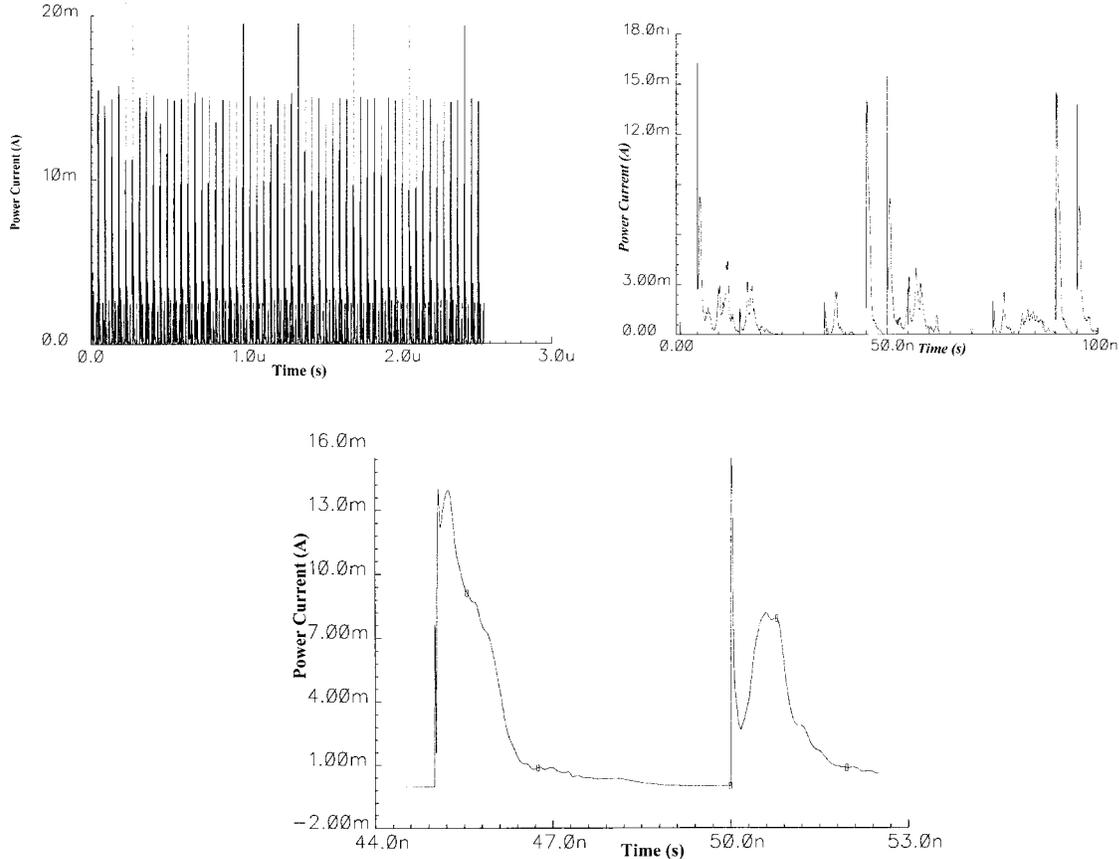

Fig. 4 Power current curves of the NCL multiplier

In Fig. 4 the upper left plot is the entire time window of 256 data patterns, the upper right plot focuses on the window of one NULL-DATA-NULL cycle, and the bottom plot shows the switching activities. The current waveforms in Fig. 4 are obtained from the supply voltage in Cadence simulation. The switching current consists of the short circuit current when both p and n-channel transistors are on and the capacitive current resulting from the charging and discharging of capacitances. The power is evaluated by integrating current and voltage over the 256 input combinations and then averaging the result.

The effect of signal bounce from V_{dd} on NCL design is evaluated. The power bus line is modeled by a simple lumped RLC network to produce voltage variation. As shown in Fig. 5, the internal V_{dd} to the multiplier dips in the initial transient and then goes back to normal. The response of the multiplier subject to V_{dd} variation is recorded in Figs. 6 and 7 for Boolean and NCL multipliers, respectively. In the NCL multiplier, threshold gates and NCL registers are used. In the Boolean multiplier, standard Boolean logic gates and equivalent registers are used.
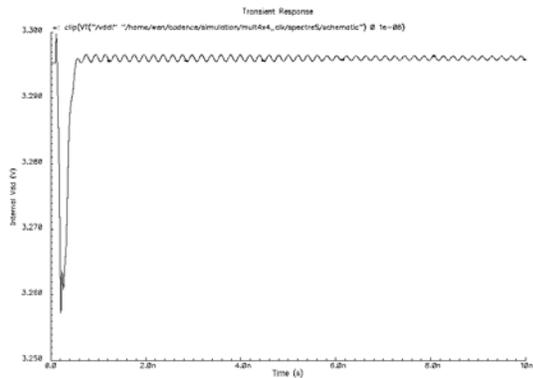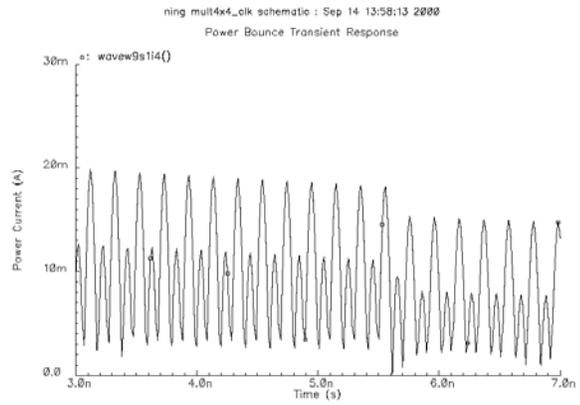
Fig. 5 V$_{dd}$ signal variation   Fig. 6 Power current curves of Boolean circuit
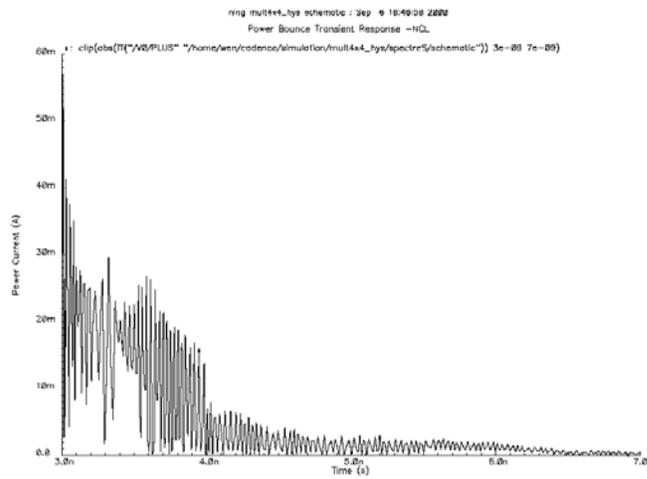

Fig. 7 Power current curves of NCL circuit

It is clear from Figs. 6 and 7 that the signal bounce due to V$_{dd}$ variation is significant for the Boolean circuit, while the NCL circuit has the ability to stop the power bus signal bounce over a very short period of time.

The adaptability of NCL circuits subject to voltage scaling is also evaluated. The following Table shows the current, energy per input pattern (or instruction), and performance of the NCL multiplier at $V_{dd} = 1.5, 2, 2.5, 3$, and 3.3 V.

Vdd [V]	1.5	2	2.5	3	3.3
Current [mA]	0.56	1.1	1.8	3	4.5
Energy/Instr [nJ]	0.19	0.32	0.51	0.87	1.31
Perf [MIPS]	4.6	6.7	8.7	10.4	11.4

In the above Table, current is the average value obtained from the supply voltage in Cadence simulation. Energy is calculated using the integration of current and voltage over a period of time. Performance is measured by the number of instructions times 10E6 dividing the time needed for the total number of instructions (or multiplications). In the 4x4 multiplier, the total number of instructions is 256.

Using more V_{dd} data points, smoother curves of current, energy/instruction, and performance are displayed in Fig. 8 below:
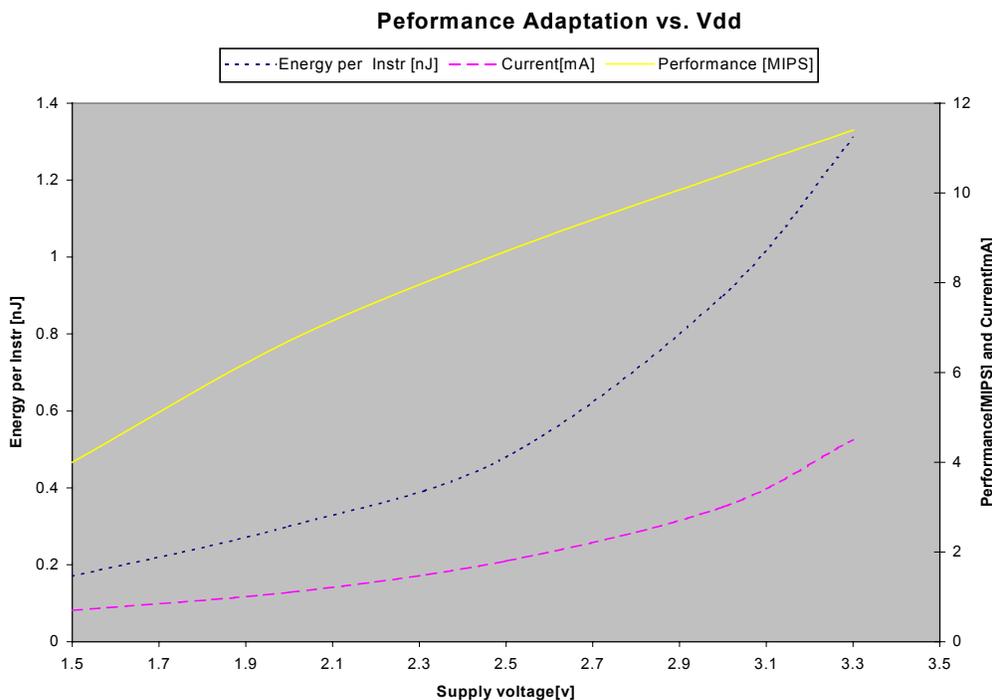

Fig. 8 Current, energy, and performance versus supply voltage

It is clear from Fig. 8 that the power current and energy per instruction increase quickly when the supply voltage increases. When the supply voltage decreases, the decrease of energy per instruction is much larger than the decrease of performance (MIPS). This implies a significant advantage for NCL design techniques for low voltage and low power applications.

6   Conclusion

The power glitches, signal bounce, and supply voltage scaling effects on the NCL multiplier are evaluated. The SPICE simulation results show that hyteresis threshold gates of NCL circuits and NCL design eliminate glitches due to signal propagation from input skews. The NCL design shows robustness in low voltage and low power applications. Randomly distributed switching activities of clockless NCL circuits generally spread signal spectrum on the power bus. This reduces power bus spikes and EMI. Further study will be conducted to demonstrate low EMI emission of NCL circuits by experiments.

References

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