

# Comparison of Four Different Designs of Sense Amplifiers on Energy Consumption for Dynamic Instruction Count

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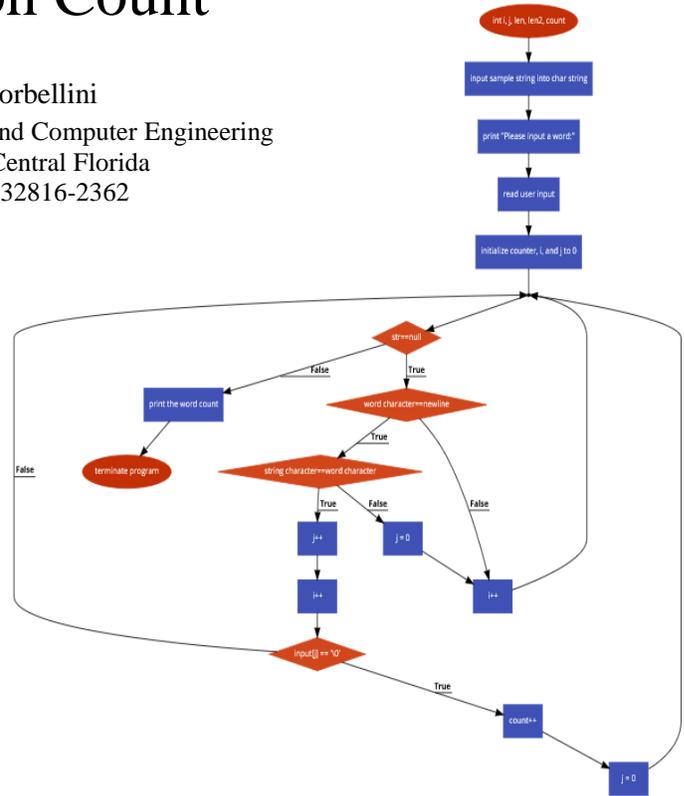
**Abstract**—The code’s goal was to read a sample sentence and see how many occurrences there were of a user inputted word in the string. This code was then used to compare the efficiency of energy consumption in four different designs of memory reading. The differences in these designs focused mainly around the design of the TGs, PVs, MTJs, and the SM in the circuit. The best energy consumption of the four designs was the EASA design with an energy consumption of only 74.5 nJ.

**Keywords**—Magnetic Tunnel Junction (MTJ), Sense Margin (SM), Transmission Gates (TGs), Process Variation (PV)

## I. PROJECT DESIGN

The code will take the string in the sample label and store it in t3. The program will print “Enter a word that you'd like to count:” for the user to write the word, and then the program will take an input from what ever the user writes. The program then loads the first bit from the string in t3 into another register. It also loads the first bit from the user input into a register, then creates two other registers, one for incrementing by 32 and one for decrementing by 32 so that it can upper case or lower case the letter just to be safe. Then it compares both and if one is equal to the bit in the sample string, then it jumps to the counter and increments it by one and back to the loop starting the next bit. After the null is hit in the string it will print the counter and terminate the program.

The code works based on which input u put in, it will load the first bit into a register and create 2 more registers based on that bit making sure it covers if the string is a capitol or lower case. It will compare the bits and if it is equal it will move on to the next bit in the input and compare it to the strings next bit. If they continue and the entire string of the input is equal to the sample, then it will add one to the counter. After it gets to the null in the sample string, it will print the counter which is equal to how many times the input string occurred in the sample string.



```

Run I/O
Enter a word that you'd like to count:and
and
5
-- program is finished running --

Enter a word that you'd like to count:AnD
AnD
5
-- program is finished running --

Run I/O
Enter a word that you'd like to count:it
it
4
-- program is finished running --
    
```

## II. MEMORY BIT-CELLS

For my program, I tried all four diverse designs that are possible for the memory read energy consumption options and compared all four of them. I calculated them all in Table II from the given Table I for the ALU instruction count given in MARS4.5 under the "Instruction Statistics" tab. The most important difference in all of these designs is the sense amplifier (SA). A sense amplifier is part of the read circuitry that is used when data is read from the memory. Its role is to sense the low power signals from a bitline that represents a data bit (1 or 0) stored in a memory cell and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly.

The first design is called the Energy Aware Sense Amplifier (EASA) which uses something called Transmission Gates (TGs) that are used to pick specific signals to block or pass to help reduce the energy that is leaked and Process Variation (PV). The more energy leaked, the more energy consumption from the system. Process variation causes measurable and predictable variance in the output performance of all circuits but particularly analog circuits due to mismatch. This design has the chance of read errors because of the extra TGs in the Magnetic Tunnel Junction (MTJ) that can cause more resistance in the circuit, which will affect the sense margin (SM) and PV.

The second design used is the Variation Immune Sense Amplifier (VISA). This design is very similar to the EASA, but the biggest difference between them is that the VISA design uses inverters. The inverters reduce leakage in some of the MTJ parts. Placing them in parallel is very advantageous because it will average the resistance of the larger and smaller numbers, increasing the SM.

The following design is known as the Pre-read and Write Sense Amplifier (PWSA). This design integrates both read and write into one circuit which allows for faster reading and writing. This setup will decrease the bit error rate, which is the consistency that a bit is incorrect in the transmission of data. This design uses 2 read steps, a pass/fail test, and a write step, which in turn increases the SM in the circuit.

The last design is the Body-Voltage Sensing Circuit (BVSC). Body-Voltage Sensing Circuit is the most intricate of the four designs because it is important what resistance load is used when trying to maximize the SM. If the resistance load is too high it could be fatal to the system and the speed can become limited. It is very important to find the right balance of this when you are constructing the circuit to get maximum efficiency from this design. If there is too large of a read margin this can affect the whole circuit.

## III. RESULTS AND DISCUSSION

Using the information given in Mars4.5 under the tools tab and Instruction Statistics, I calculated all of the energies used by each process. I ran the program using the word "and" for the input and the dynamic instruction count came out to 8474. I calculated the ALU, Jump, Branch, Memory, and Other energy. All of them are simple besides the Memory consumption, which will be the 50fj for the writing portion of it, but will have a different energy consumption based on which design is used.

The ALU, Jump, Branch, Memory write, and other energy consumptions are constant, so you can calculate the total energy for those processes and then add the memory read energy consumption for each of the four designs. These are the energy costs for each process:

- 1)  $ALU = 1 \text{ fJ}$
- 2)  $Branch = 3 \text{ fJ}$
- 3)  $Jump = 2 \text{ fJ}$
- 4)  $Memory = Read \text{ Energy} + Write \text{ Energy} (50\text{fJ})$
- 5)  $Other = 5 \text{ fJ}$

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [1-3].

Design	Energy Consumption For Each Bit-cell's Read Operation
EASA [1]	0.23 fJ
VISA [1]	1.86 fJ
PWSA [2]	36.0 fJ
BVSC [3]	195.5 fJ

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
EASA [1]	74.5nJ
VISA [1]	76.5nJ
PWSA [2]	119.5nJ
BVSC [3]	319.4nJ

## IV. CONCLUSION

This program was used as a testbench to compare the energy consumption of four different designs. The main factors in the energy consumptions for each circuit was the design of the TGs, PVs, MTJs, and the SM. EASA and VISA had very similar designs, but the inverters took up a little bit more energy in the circuit. The best design was the first one for the EASA. Its energy consumption in total was 74.5nJ which is 2nJ better than the VISA, and largely better than the rest.

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