Analysis of memory bit-cells when comparing design implementation

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***Abstract*— Different design implementations are used for select performance criteria. These designs can have a whole range of effects on a system and its output. Triple Modular Redundancy (TMR) is used to fulfil certain requirements in a system for initial overhead cost. TMR adds a high failure mitigation in a system and provides protection against Soft Errors, Single-Event Transient (SET), and Single-Event Upset (SEU). Though TMR is the most accurate at mitigating failures it consumes a lot of energy from the system. In this report we compared the energy consumption of each design from reference [2][3][4]. These tests have concluded that the Spin-transfer torque-RAM (STT-RAM) is the best, with the lowest energy consumption at 231,282 fj and a high rate of functionality.**

Keywords— Soft Error, Soft Error Rate (SER), Triple Modular Redundancy (TMR), Single-Event Transient (SET), Single-Event Upset (SEU), Magnetic tunnel junction (MTJ), Single event double node upsets (SEDU), Magnetic RAM (MRAM), Spin-transfer torque memory (SPRAM), *Spin-transfer torque-RAM (STT-RAM)*

I. PROJECT DESIGN

The Capstone project has a hardcoded string, or sample string, which the user will input a word to search for in the string. The word is exclusive and does not need to be repeated in the string to be counted. The program outputs how many occurrences there are of each word. It will count a string regardless of case, so an input of "KniGht" or "KnIGHt" will iterate if "knight" is present in the hardcoded string. The input string is taken and stored initially.

To begin comparisons, the first byte of the input and the sample string are both loaded into registers. When the value 10 is reached for the string, it indicates that the end of the string has been reached because there is a new line. Thus, the count for it can be incremented and the address will point back to the first byte and it will be checked for again. At each byte in the address, the value within it will be compared to several branch-equivalent statements ensuring that, regardless of case, matching values such as "A" and "a" will be counted as equivalent. This is done by adding 32 in case the sample value is capital and needs to be compared to lowercase, then subtracting 64 for another comparison in case the value is lowercase and needs to be compared to a capital. The address

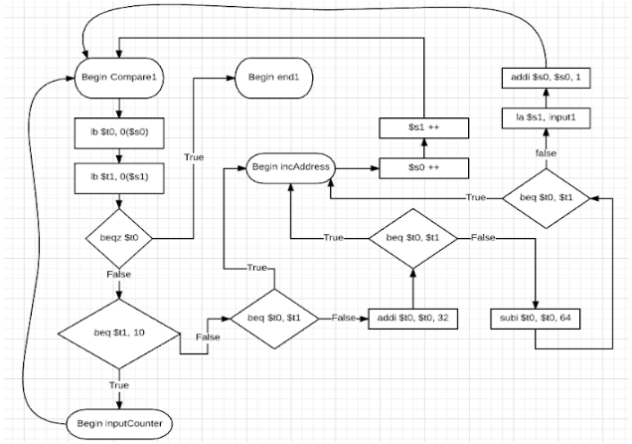

Fig.1: Flowchart of the assembly program.

```
Please input the word you want to search: KNIGHT
KNIGHT
: 6
-- program is finished running --

Please input the word you want to search: KnIGhT
KnIGhT
: 6
-- program is finished running --

Please input the word you want to search: knight
knight
: 6
-- program is finished running --
```

Fig.2: Sample outputs of the program.

always goes back to the first byte of the input string whenever the whole input word is not found before the new line value 10. After checking through the hardcoded string in the same way, the end of the code is reached when the sample string once again reaches the zero value. The amount of times each word is found is output as an integer.

This code can be tested by using various input strings with different case combinations. It should function regardless of case because it was designed to compare the values of the hardcoded string and input strings for all cases. This code can be tested with special characters as well. The code is designed to work with anything less than 10 characters. It will only find words present in the hardcoded string. This string will be tested using uppercase, mixed case, and lower case.

II. Memory Bit-Cells

To be able to reliably deal with the complexity of modern technology and its problems we must figure out different methods of protecting against faults. One method is Triple Modular Redundancy (TMR)(3MR), which is the process of triplicating circuity to input into a majority voter for a single output [1]. TMR is effective for fault masking on a system in multiple instance [1]. As well as the mitigation of soft errors, which affect the system critically [1]. TMR has high reliability in mitigating faults like Single-Event Transients (SET) and Single-Event Upsets (SEU) [3][4], but it has disadvantages that cause it to be inferior in some instances.

To use TMR you need a system able to withstand the cost. Though TMR is great for mitigating faults it comes with a more abundant consumptions rate. For instance, compared with FTNV-L, TMR has 2× reading/writing latency and 3× the energy consumption [2]. TMR requires a more overhead compared to other system in space, energy, and clock latency. The TMR circuits are more complex making it have more leakage caused by more components in the circuit. Another problem that could arise is an internal voting failure. While most voting failures are single failures, they cause little effect to the system. When there are two voting failures, it causes improper reporting and the output becomes corrupt [1]. This is critical in the system and can cause further disruptions.

The use of STT-RAM is promising for the future and how we process memory. Being able to surpass DRAM and its size capabilities means that technology will continue even at the nano scale [5]. The pictures in the report show a new model of the nano technology in which the transistors are made with overlapping metals [5].

The STT-RAM is a much-needed improvement on other forms of memory. Such improvements include high density, high speed, low-power, and non-volatile memory [6]. STT-RAM has issues with read and write failures. They optimized the read and write functions by using MTJ design to mitigate failures [6].

Just like in STT-RAM, spin-transfer torque memory (SPRAM) is another form of memory able process at high speeds with proficient function. This product is also using MTJ for mitigation and proficiency in read/write functions [7]. They use these MTJ for more reliable switching and less switch failures when reading/writing in programs [7].

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [2-4].

Design	Energy Consumption For Each Bit-cell's Read Operation
3MR, TMR [2]	1170 fJ
FTNV-L [2]	366 fJ
STT-RAM [3]	150 fJ
[4]	800 fJ

Table II: Total Energy consumption for the assembly program using designs provided in [2-4].

Design	Total Energy Consumption
3MR (TMR) [2]	1524642 fj
FTNV-L [2]	505170 fj
STT-RAM [3]	231282 fj
[4]	1055482 fj

III. Results and Discussion

In this section we have two tables. These tables show the compared energy of our Project-3-Dunn-Nathaniel.asm MARS 4.5 Capstone Project.

1) *ALU = 1 fJ*
2) *Branch = 3 fJ*
3) *Jump = 2 fJ*
4) *Memory = Read Energy (Refer to Table I) + Write Energy (20fJ)*
5) *Other = 5 fJ*

IV. Conclusion

From the data overserved, TMR has a large consumption of energy. This means that the system will need overhead to use TMR. TMR is one of the best ways to mitigate failures, but it is situational since it requires a large amount of area and energy. Technical topics learned in the report include Soft Errors, Triple Modular Redundancy, Single-Event Transients, Single-Event Upsets, Magnetic tunnel junction, and Spin-transfer torque-RAM. The best energy design is from reference [3] STT-RAM with a total energy consumption of 231282 fj.

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