Radiation-hardened MRAM-based LUT for non-volatile FPGA soft error mitigation with multi-node upset tolerance

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Abstract. In this paper, we have developed a radiation-hardened non-volatile lookup table (LUT) circuit utilizing spin Hall Effect (SHE)-magnetic random access memory (MRAM) devices. The design is motivated by modeling the effect of radiation particles striking hybrid CMOS/spin based circuits, and the resistive behavior of SHE-MRAM devices via established and precise physics equations. The models developed are leveraged in the SPICE circuit simulator to verify the functionality of the proposed design. The proposed hardening technique is based on using feedback transistors, as well as increasing the radiation capacity of the sensitive nodes. Simulation results show that our proposed LUT circuit can achieve multiple node upset (MNU) tolerance with more than 38% and 60% power-delay product improvement as well as 26% and 50% reduction in device count compared to the previous energy-efficient radiation-hardened LUT designs. Finally, we have performed a process variation analysis showing that the MNU immunity of our proposed circuit is realized at the cost of increased susceptibility to transistor and MRAM variations compared to an unprotected LUT design.

1. Introduction and previous work

Radiation-induced soft errors in nanometer-scale electronic circuits are of increasing concern in mission-critical space-based [1], high altitude [2], and terrestrial applications [3]. For instance, space missions which take place in a harsh environment in terms of cosmic radiation particles, temperature, and electromagnetic disturbances have grappled with radiation-induced upsets for many decades of continued device technology scaling [4]. As device dimensions are reduced, the critical charge required to induce a logic state upset causing a soft error has decreased, which is due to a number of compounding physical phenomena. These include the cumulative impact of aggressive voltage scaling which reduces the voltage headroom available to mask errors, and the continued miniaturization of deeply-scaled CMOS-based computing technology [5]. Applications which are especially susceptible due to factors of the mission criticality, the number and density of sensitive devices, and the environmental exposures they endure are autonomous systems utilizing high capacity fine-grained configurable components, such as Field Programming Gate Arrays (FPGAs) [6].

FPGAs are widely utilized in autonomous embedded systems due to their flexibility and accessibility. Being reconfigurable hardware fabrics, they can realize autonomous and adaptive computation with low component count, and thus frequently operate as mission-critical control elements [7]. Fortunately, FPGAs also enable uniquely-feasible solutions to process-voltage-temperature variations and can be effectively leveraged for fault recovery [6, 8]. This is mainly achieved through utilizing spare resources during the reconfiguration process, which provides run-time adaptability. However, spare fabric and registered outputs can increase device area and power consumption, as well as decrease performance compared to the application-specific integrated circuits (ASICs). Look-Up Tables (LUTs) are primary building blocks in FPGAs, which are utilized to implement Boolean logic functions. In particular, to implement an N-input Boolean function, a LUT circuit requires 2^N memory cells to store the logic function configuration data. Currently, most of the commercial FPGAs such as Altera and Xilinx products use static random access memory (SRAM) cells as storage elements within their LUT structure.

SRAM-based FPGAs, like all CMOS-based fabrics, are susceptible to radiation-induced transient soft faults such as single event upsets (SEUs), which primarily affect SRAM-based storage cells [9]. Thus, research into the design of suitable placements with improved soft error immunity and energy profiles is

urgently sought using a number of feasible physical devices including RRAM [10] and MRAM [11, 12]. This trend has been motivated by aggressive CMOS technology scaling in digital circuits has resulted in significant increase in transient fault rates, as well as timing violations due to process variation (PV) that consequently reduces the performance and reliability of the emerging very large scale integrated circuits. For instance, the probability of single upsets, and more realistically, multiple upsets, is projected to increase several fold at sea-level for sub-10nm technology nodes [13, 14]. By the extensions to sub-10nm regimes, error resiliency has become a major challenge for microelectronics industry, particularly mission critical systems, e.g. space and terrestrial applications. The ability of FPGAs to correctly execute the complicated tasks in harsh environments significantly relies on their fault-handling and radiation hardening techniques, such as the design approach proposed in this paper.

In addition to the radiation susceptibility, SRAM cells suffer from high static power dissipation, storage volatility requiring energy consumption even while in standby-mode, and low logic density, which has resulted in the significant gap between FPGAs and ASICs in terms of area, performance, and power consumption [15]. Therefore, innovations leveraging emerging devices within reconfigurable fabrics have been sought to bridge these gaps. The 2014 Magnetism Roadmap [16] identifies spintronic devices as capable post-CMOS candidates. Spintronic devices offer radiation immunity, non-volatility, high integration density, and incur near-zero standby energy consumption [17, 18]. Magnetic tunnel junctions (MTJs) [19, 20] and domain wall nano-magnets [21, 22] are the spin-based technologies, which have been previously proposed to be utilized within reconfigurable fabrics.

In [11], authors have provided the fabrication results of a nonvolatile FPGA providing 3,000 6-input MTJ-based LUTs under 90nm CMOS and 75nm perpendicular MTJ technologies. Leveraging non-volatile MTJs as an alternative for SRAM cells has enabled the power-gating of the LUT islands. This has resulted in 81% reduction in power consumption while achieving 56% area reduction. They have utilized the LUT design introduced in [20], in which the spin transfer torque (STT) [23] switching approach is leveraged for reconfiguration operation. STT mechanism can consume roughly ten times more energy consumption for write operation compared to conventional SRAM cells [24]. In recent years, spin Hall effect (SHE)-assisted STT approach is introduced, which consumes significantly less energy consumption compared to conventional STT [25, 26]. In [12], authors have designed a SHE-MTJ based LUT achieving more than 20% reduction in reconfiguration energy consumption.

Leveraging magnetic random access memories (MRAMs) as storage elements within LUT circuits has the potential to significantly increases their radiation immunity due to the radiation hardness characteristic of spin-based devices. However, the access and sensing circuitry for MRAM still requires transistors, and thus is still susceptible to radiation-induced faults. Therefore, circuit-level innovations are sought to achieve immunity to radiation-induced transient faults such as SEUs and double node upsets (DNUs). In recent years, various radiation hardening techniques are investigated to develop SEU-tolerant MRAM-based LUTs [27, 28]. In particular, in [29] authors have proposed a single-event double-node upset tolerant MRAM-based LUT, which provides multiple upset resiliency at the cost of increased read energy and area consumption with baseline efficacy. In this paper, we develop a nonvolatile MRAM-based LUT using SHE-MTJ devices, which can tolerate DNUs with improved area, delay, and power consumption.

The remainder of this paper is organized as follows. Acronyms used within the paper are listed in table 1. Section 2 focuses on the fundamentals and modeling of SHE-MTJ devices, as well as modeling of radiation effect on hybrid CMOS/spin based circuits. The effect of radiation on conventional MRAM-based LUTs is investigated in section 3. Moreover, section 3 provides the design and analysis of the proposed radiation-hardened MRAM-based LUT and its comparison with previous designs. Section 4 describes the impact of the process variation on the functionality of the proposed radiation-hardened MRAM-based LUT. Finally, section 5 concludes the paper and highlights our proposed design advantages and features.

Table 1. The list of the acronyms used in this paper.

Acronym	Definition	Acronym	Definition
ASIC	application specific integrated circuit	PCSA	pre-charge sense amplifier
CMOS	complementary metal oxide semiconductor	PDP	power-delay product
DNU	double node upset	PV	process variation
FPGA	field programmable gate array	SEU	single event upset
HM	heavy metal	SHE	spin Hall Effect
LET	linear energy transfer	SHIE	spin Hall injection efficiency
LUT	lookup table	SRAM	static random access memory
MNU	multiple node upset	STT	spin transfer torque
MRAM	magnetic random access memory	TG	transmission gate
MTJ	magnetic tunnel junction	TMR	tunnel magnetoresistance

2. Background

2.1. Fundamentals and Modeling of SHE-MTJ devices

MTJs consist of two ferromagnetic layers, called *fixed layer* and *free layer*, which are separated by a thin oxide barrier layer such as MgO. Fixed layer is magnetically pinned and used as a reference layer, while the free layer magnetic orientation can be readily changed and is leveraged as a storage layer [30]. The tunnel magnetoresistance (TMR) effect incurs two distinct resistance levels for MTJ devices, which are defined by the angle between the magnetization orientations of the two ferromagnetic layers, as expressed by the following relations [31, 32].

$$R(\theta) = 2R_{MTJ}.\frac{1+TMR}{2+TMR+TMR.cos\theta} = \begin{cases} R_P = R_{MTJ} & , \ \theta = 0° \\ R_{AP} = R_{MTJ}(1+TMR), & \theta = 180° \end{cases} \quad (1)$$

$$R_{MTJ} = \frac{t_{ox}}{Factor.Area.\sqrt{\varphi}} \exp(1.025 t_{ox}.\sqrt{\varphi}) \quad (2)$$

$$TMR = TMR(0)/[1 + \left(\frac{V_b}{V_h}\right)^2] \quad (3)$$

where R_P and R_{AP} are the resistance of the MTJ in parallel (P) and antiparallel (AP) configurations, respectively. V_b is the bias voltage, and V_h = 0.5 V is the bias voltage when the TMR is half of the TMR(0), which is the default TMR ratio when V_b=*0*, t_{ox} is the oxide thickness of MTJ, *Factor* is obtained from the resistance-area product value of the MTJ that relies on the material composition of its layers, *Area* is the surface of MTJ, and φ=0.4 is the oxide layer energy barrier height. The energy barrier between P and AP configurations of MTJ is in a range such that it can switch between configurations, while also retaining the thermal stability.

Figure 1 shows the structure of a three-terminal SHE-MTJ device, in which free layer is directly connected to a heavy metal (HM), e.g. β-tungsten (β-W) [33]. The free layer magnetization orientation can

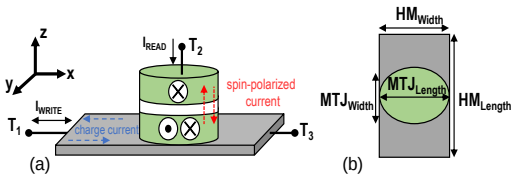

Figure 1. (a) SHE-MTJ vertical structure. Positive current along *+x* induces a spin injection current *+z* direction. The injected spin current produces the required spin torque for aligning the magnetic direction of the free layer in *+y* directions, and vice versa. (b) SHE-MTJ Top view.

be switched through the charge current applied to the HM. The spin-orbit coupling in HM deflects the electrons with distinct spins in opposite directions leading to the generation of a spin injection current transverse to the applied charge current. The spin-polarized current that flows through the MTJ free layer experiences an exchange field, which aligns the spin of the electron with the magnetization direction of the nanomagnet. The conservation of the angular momentum results in the exertion of an opposite sign torque with equal magnitude that changes the free layer magnetization direction [12, 34]. The ratio of the injected spin current to the applied charge current is called spin Hall injection efficiency (SHIE), which is normally greater than one and is defined in (4) [35].

$$SHIE = \frac{I_{sz}}{I_{cx}} = \frac{(\pi/4).w_{MTJ}.l_{MTJ}}{t_{HM}.w_{HM}}\theta_{SHE}\left[1 - \text{sech}(\frac{t_{HM}}{\lambda_{sf}})\right] \quad (4)$$

where λ_{sf} is the spin flip length in HM, and $\theta_{SHE}=J_s/J_c$ is the spin Hall angle, where J_c is the applied charge current density and J_s is the spin current density generated by SHE. Herein, SHIE value is equal to 1.73 that is obtained based on the parameters listed in table 2. An interesting feature of the SHE phenomenon that can be observed through this equation is how it can lead to spin-currents that are larger than the inducing charge currents. The critical spin current required for switching the free layer magnetization orientation is expressed by (5), where V_{MTJ} is the MTJ free layer volume [36], α is the Gilbert damping factor, M_S is the saturation magnetization, and H_k is the anisotropy field. Thus, SHE-MTJ critical charge current can be calculated using (4) and (5).

$$I_{S,critical} = 2q\alpha M_S V_{MTJ}(H_k + 2\pi M_S)/\bar{h} \quad (5)$$

The dynamic behavior of free layer in SHE-MTJ devices can be described using a modified Landau-Lifshitz-Gilbert (LLG) equation, as expressed in (6-9) [37, 38]:

$$\frac{\partial \vec{m}}{\partial t} = -\gamma\mu_0(\vec{m} \times \vec{H}_{eff}) + \alpha\left(\vec{m} \times \frac{\partial \vec{m}}{\partial t}\right) - c_{SHE}(\vec{m} \times \vec{\sigma}_{SHE} \times \vec{m}) \quad (6)$$

$$\vec{m} = sin\theta cos\varphi\vec{x} + sin\theta sin\varphi\vec{y} + cos\theta\vec{z} \quad (7)$$

$$\vec{\sigma}_{SHE} = -\vec{x} \quad (8)$$

$$\vec{H}_{eff} = H_k sin\theta cos\varphi\vec{x} - M_s cos\theta\vec{z} \quad (9)$$

where $\vec{m}$ is the unit vector of free layer magnetization, γ is electron gyromagnetic ratio, μ_0 is vacuum permeability, H_{eff} is effective magnetic field. The spin-Hall torque coefficient is $c_{SHE} = J_s\theta_{SHE}\bar{h}\gamma/(2qd)$, where, $\bar{h}$ is the reduced Planck constant, and d is the free layer thickness. The equation (6) can be solved assuming that $\vec{x}$, $\vec{y}$, and $\vec{z}$ are the unit vecors along X, Y, and Z axes of the Cartesian coordinate system, respectively. Moreover, θ and φ are polar and azimuthal angles, respectively. Substituting (7-9) into (6) results in a nonlinear system of two differential equations expressed in (10) [37, 38]:

$$\begin{cases} \frac{d\theta}{dt} = \frac{\gamma\mu_0 H_k sin\theta cos\varphi(-sin\varphi + \alpha cos\theta cos\varphi) + \alpha\gamma\mu_0 M_s cos\theta sin\theta - c_{SHE}(cos\varphi cos\theta + \alpha sin\varphi)}{(1+\alpha^2)} \\ \frac{d\varphi}{dt} = \frac{\gamma\mu_0(-H_k sin\theta cos\varphi cos\theta cos\varphi - \alpha H_k sin\theta cos\varphi sin\varphi - M_s cos\theta sin\theta) + c_{SHE}(sin\varphi - \alpha cos\varphi cos\theta)}{(1+\alpha^2)sin\theta} \end{cases} \quad (10)$$

The free layer magnetization dynamics can be described using the θ and φ coordinates which can be obtained via solving (10), in which the initial θ induced by the thermal distribution at a finite temperature can be calculated as $\theta_0 = \sqrt{k_B/2E_b}$, where $E_b=(1/2)\mu_0 M_s H_k V_{MTJ}$ is the thermal barrier of the magnet [39].

The relation between the switching time (τ_{SHE}) and the applied charge current (I_{SHE}) is shown in (11), in which v_c is the critical switching voltage, τ_0 is the characteristic time, and R_{HM} is the HM resistance, which are given by (12), (13), and (14), respectively [35]:

$$\tau_{SHE} = [\tau_0 . ln(\pi/2\theta_0)]/[(\frac{R_{HM}.I_{SHE}}{v_c}) - 1] \quad (11)$$

$$v_c = 8\rho.I_c\left\{\theta_{SHE}.\left[1 - \text{sech}(\frac{t_{HM}}{\lambda_{sf}})\right].\pi.l_{HM}\right\}^{-1} \quad (12)$$

$$\tau_0 = M_s.V_{HM}.q/I_c.P.\mu_B \quad (13)$$

$$R_{HM} = (\rho_{HM}.l_{HM})/(w_{HM}.t_{HM}) \quad (14)$$

where l_{HM} is the length of the HM, and I_C is the critical charge current for spin-torque induced switching. In this paper, the approach proposed by authors in [12, 40] is utilized to model the behavior of SHE-MTJ device, in which a Verilog-AMS [41] model is developed using the aforementioned equations. Then, the model is leveraged in SPICE circuit simulator [42] to validate the functionality of the designed circuits using experimental parameters listed in table 2.

2.2. Fundamentals and modeling of radiation effect on hybrid CMOS/spin based circuits

Among the natural sources of α, β, and γ radioactivity only alpha particles are able to incur transient errors in hybrid CMOS/spin-based circuits due to their high energy [43]. Alpha particles are able to deposit a charge along their track when striking a sensitive node of a circuit. The charge will be transported into the device and collected in the sensitive region [44]. A transient fault is generated if the injected charge (Q_{inj}) exceeds the critical charge (Q_c) of the sensitive node. The Q_c can be realized by a capacitance and a conduction component as shown below:

$$Q_c = C_N.V_{DD} + I_D.T_F \quad (15)$$

where C_N is the equivalent capacitance of the struck node, V_{DD} is the power supply, I_D is the maximum drain conduction current and T_F is the flipping time of the cell. The computation of T_F requires a 3D device simulation, therefore to simplify the circuit simulation the conduction component of the (15) is normally ignored that leads to an insignificant under-estimation [45, 46].

Radiation particles striking a microelectronic device can free some electron-hole pairs and exchange energy while passing through the semiconductor material. The energy loss per unit path length of a particle transit can be defined by a linear energy transfer (LET), which is typically normalized via the density of the target material. Meanwhile, LET is relatively independent of other attributes of the target material and is expressed using units of MeV/cm^2/mg. The charge deposition of a particle, which can impact the functionality of a struck circuit, is directly related to its LET. The most sensitive regions in microelectronic

Table 2. The parameters utilized in this paper for modeling the SHE-MRAM devices. These parameters are obtained based on the experimental measurements provided in the literature [35].

Parameter	Description	Value
HM_{Volume}	$l_{HM} \times w_{HM} \times t_{HM}$	100 nm×60 nm×3 nm
MTJ_{Area}	$l_{MTJ} \times w_{MTJ} \times \pi/4$	60nm×30nm× π/4
α	Gilbert Damping factor	0.007
P	Spin Polarization	0.52
M_S	Saturation magnetization	7.8e5 A·m^{-1}
H_k	Anisotropy Field	80 Oe
θ_{SHE}	Spin Hall Angle	0.3
μ_B	Bohr Magneton	9.27e-24 J·T^{-1}
ρ_{HM}	HM Resistivity	200 μΩ.cm
q	Electric charge	1.602e-19 C
λ_{SF}	Spin Flip Length	1.5nm
$\hbar$	Reduced Planck's Constant	6.626e-34/2π J.s

devices are reverse-biased junctions, where the high field existing in their depletion region can collect the charges induced by the radiation particles. This can happen via a drift process, which results in a transient current at the junction contact. Moreover, a significant transient current can be generated by the particles striking near the depletion region due to the carriers' diffusion into the depletion region field [47]. Investigations on the impact of alpha-particle strikes on the reverse-biased junction [48] has exhibited a transient disturbance in the junction electrostatic potential. The highly conductive nature of the charge track produced by the radiation particle can generate a funneling effect extending the junction electric field deep into the substrate, which can lead to increased charge collection at the struck node [47].

Various approaches are proposed to model the radiation-induced transient faults such as those put forth by Freeman [49], as well as diffusion collection [50] models. Herein, we have utilized a double-exponential time-dependent current source to model the radiation effect, which is the most commonly-used approach for modeling the charge collection at a junction due to the funneling or diffusion [51, 52]. The current sources are connected to the sensitive nodes of the circuit to inject current to the nodes where radiation particles are supposedly struck. The injected current pulse is given by (16), in which τ_f and τ_r are falling time and rising time of the exponentials which are typically 150ps and 50ps, respectively. Moreover, Q_{inj} values range from -200fC to 200fC which relies on the particle energy as well as its LET [53, 54]. The actual Q_{inj}, τ_f, and τ_r values depend on various factors including the ion species, ion energy, device dimensions, and the particle hit location [47]. The sign of the Q_{inj} depends on the type of the struck MOS transistor, in particular a strike in the drain of an NMOS transistor incurs a negative spike, and vice versa. Figure 2 depicts the injected current pulses for various Q_{inj} values, which are generated by hypothetical particles striking at *t=0*.

$$I(t) = \frac{Q_{inj}}{\tau_f - \tau_r}(e^{-t/\tau_f} - e^{-t/\tau_r}) \tag{16}$$

3. Design and analysis of the proposed radiation-hardened MRAM-based LUT

Figure 3 shows the structure of a conventional SHE-MRAM based LUT including *write circuitry*, *select tree*, and *read circuitry*. Transmission Gates (TGs) are leveraged within the write circuit and select tree due to their energy efficiency and process variation resiliency, as previously established by the authors in [19, 55]. Pre-charge sense amplifiers (PCSAs) [56] are widely utilized as the read circuit of the conventional MRAM-LUT designs. PCAS operation involve two steps, first in *pre-charge* state OUT and OUT′ nodes, shown in figure 3, are charged to the circuit nominal voltage (VDD). Then, in the *discharge* state the voltage source is isolated from the circuit and the pre-charged nodes start discharging with different speeds depending on the resistance of the discharge paths. The node that discharges faster connects the other node to the VDD through a PMOS transistor, i.e. MP1 or MP2, and it will be completely discharged to the

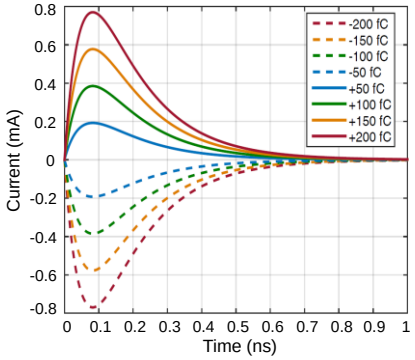

Figure 2. Transient current pulses induced by the particles striking at *t=0* with the Q_{inj} values ranging from -200 fC to +200 fC.

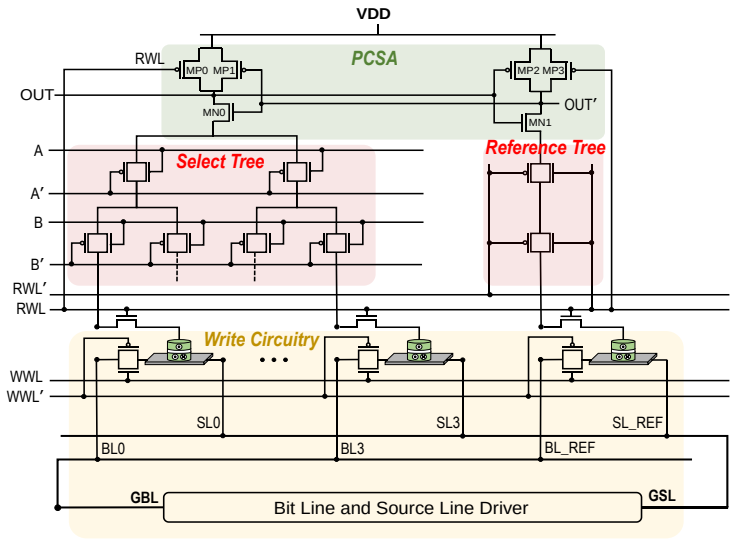

Figure 3. The diagram of a 2-input SHE-MRAM based LUT circuit consisting of: (1) *Write Circuit*, which is used in the reconfiguration operation for switching the logic states of the SHE-MRAM storage cells. (2) *Sensing Circuitry*, in which the conventional PCSA is leveraged to sense the state of the storage cell based on its resistance difference with that of the reference MRAM cell. (3) *Select Tree*, which interconnects the storage cells to the sensing circuitry according to the input signals. (4) *Reference Tree*, which compensates for the active resistance of the select tree to decrease the effect of select tree resistance on the read operation.

ground. The OUT node is linked to the LUT storage elements through the *select tree*, which enables accessing each of the storage cells through the address provided by the input signals, i.e. *A* and *B*. While, the OUT′ node is connected to a reference tree that compensates for the resistance of the select tree, as well as a reference SHE-MRAM, the dimensions of which are designed in a manner such that its resistance in *P* configuration is between the resistance of the storage cells in *P* and *AP* configurations.

Contrary to conventional SRAM cells, SHE-MRAM devices are characterized by their radiation hardness, since in MRAM cells the spin direction of electrons are leveraged to store data instead of the electron charges. The electric charges induced by the alpha particles striking the MRAM devices do not influence the spin direction of the electrons. However, the CMOS-based circuitry in hybrid CMOS/Spin circuits is still susceptible to radiation-induced transients. As investigated in [47], the radiation-sensitive nodes of a CMOS-based circuit are the surroundings of the reverse-biased drain junction of a transistor biased in the OFF state. Therefore, although the SHE-MRAM devices are immune to radiation during stand-by mode, their write circuit could be influenced by the striking particles. This leads to injecting a current to the write terminals of the SHE-MRAM, which normally cannot change their magnetic state due to the short duration of the injected current pulses. To exhibit the transient behavior of the SHE-MRAM devices in presence of the radiation-induced current pulses we have utilized the SHE-MRAM model developed by Camsari et al. in [57]. Figure 4 shows the transient response of the SHE-MRAM devices to the injected current pulses. As shown in figure 4, radiation does not have a significant effect on the LUT write operation. Thus, in this paper we have focused on the effect of radiation on the LUT read operation. During the *pre-charge* operation of the PCSA, its transistors are biased in the ON state and will not be impacted by the radiation particles. While, in the *discharge* phase, OUT and OUT′ nodes are the surroundings of reverse-biased junctions of NMOS or PMOS transistors that are biased in OFF states. Hence, OUT and OUT′ are the sensitive nodes during the read operation of the LUT circuit. Figure 5 shows the behavior of the LUT

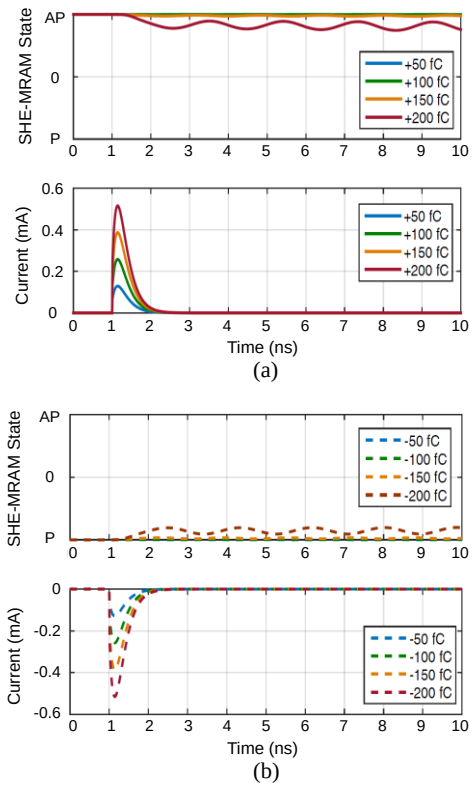

Figure 4. Transient response of the SHE-MRAM devices to the current pulses induced by the particles striking at t=1ns. (a) Switching from *AP* to *P* state with the Q_{inj} values ranging from zero to +200 fC, (b) switching from *P* to *AP* state with the Q_{inj} values ranging from -200 fC to zero. None of the injected current pulses can completely switch the state of the SHE-MRAM, since they have relatively short duration that is normally less than the switching duration required for completely changing the magnetic direction of the SHE-MRAM free layer.

circuit depicted in figure 3 in presence of SEUs. Although the MRAM cells are resilient toward SEUs, the conventional MRAM-based LUT structure is still susceptible to the charges injected by the radiation particles. Therefore, herein we build upon the previous radiation hardening techniques [27-29, 54] to develop a protected SHE-MRAM based LUT which can tolerate multiple node upsets. Our proposed approach is based on two hardening techniques: (1) leveraging feedback transistors to discharge the electric charges injected to the sensitive nodes through struck particles, and (2) increasing the critical charge (Q_C) of the sensitive nodes by increasing their equivalent capacitances while balancing tradeoffs of a corresponding increase in switching delay.

The structure of our proposed radiation-hardened 2-input SHE-MRAM LUT circuit includes 30 transistors and five SHE-MRAM cells as shown in figure 6, in which the write circuitry is abstracted for clarity. In particular, 14 transistors are utilized in the sensing and hardening circuitry, 12 transistors within select tree, and four SHE-MRAM devices to store the logic function configuration data of a 2-input Boolean function. Moreover, the reference circuitry includes four transistors to compensate for the resistance of the select tree and one SHE-MRAM cell. The hardening circuitry includes two TGs, and four NMOS transistors which are responsible for discharging the electric charge induced by the radiation particles striking the OUT and OUT′ nodes. However, the utilization of this feedback transistors introduces two new sensitive nodes to the LUT circuit, i.e. *n1* and *n2*, as shown in figure 6. Herein, the radiation-tolerance of *n1* and *n2* nodes are increased by enlarging the Q_C through increasing the equivalent capacitances of the nodes, which are

linearly proportional to the width of the transistors connected to each node. The behavior of the proposed design in presence of SEUs and DNUs is shown in figure 7 and figure 8, respectively. The simulation is performed in the condition that the LUT storage cell is in *P* state, therefore the OUT and OUT′ logic values are "0" and "1", respectively, and sensitive nodes are OUT, OUT′, and *n2*.

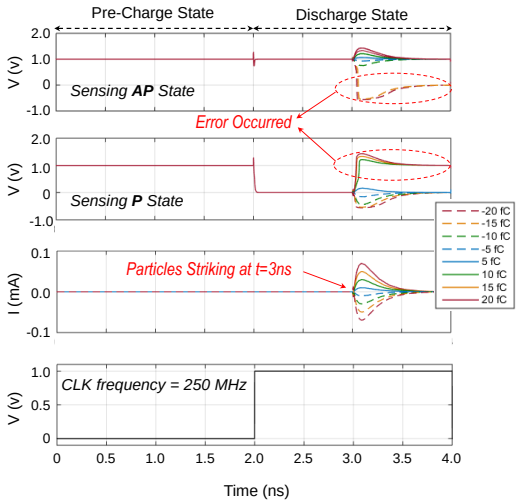

Figure 5. Transient response of the SHE-MRAM based LUT circuit to the current pulses induced by the particles striking at the discharge phase of the PCSA with the Q_{inj} values ranging from -20fC to +20fC. As depicted, the ability of the circuit to recover from the SEU relies on the amount of the injected charge, as well as the critical charge of the circuit (Q_C). If the Q_{inj} exceeds the Q_C the sensed data cannot be recovered and error occurs.

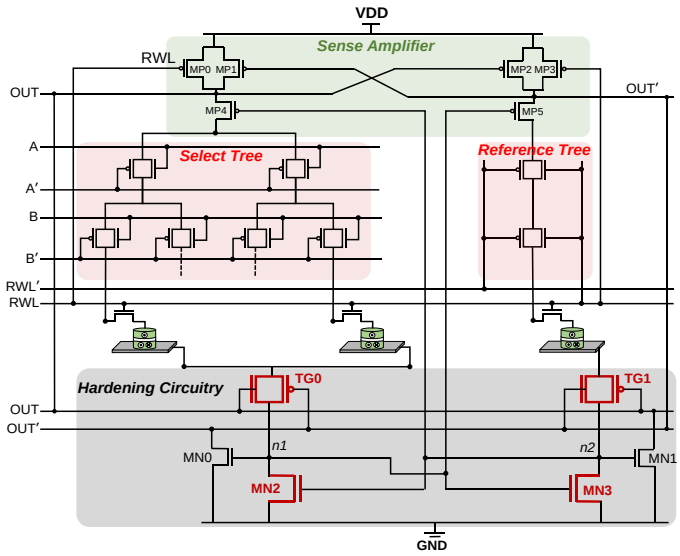

Figure 6. The structure of the proposed radiation-hardened 2-input SHE-MRAM based LUT circuit, in which four NMOS (MN0-MN3) transistors and two TGs (TG0-TG1) are utilized as feedback transistors to discharge the radiation-induced electric charge on OUT and OUT′ sensitive nodes that can impact the functionality of the LUT circuit. The functionality of the feedback circuitry can also be disturbed by the radiation particles striking *n1* and *n2* sensitive nodes. Therefore, the charge capacity of these nodes are increased by enlarging the width of the transistors connecting to these nodes.

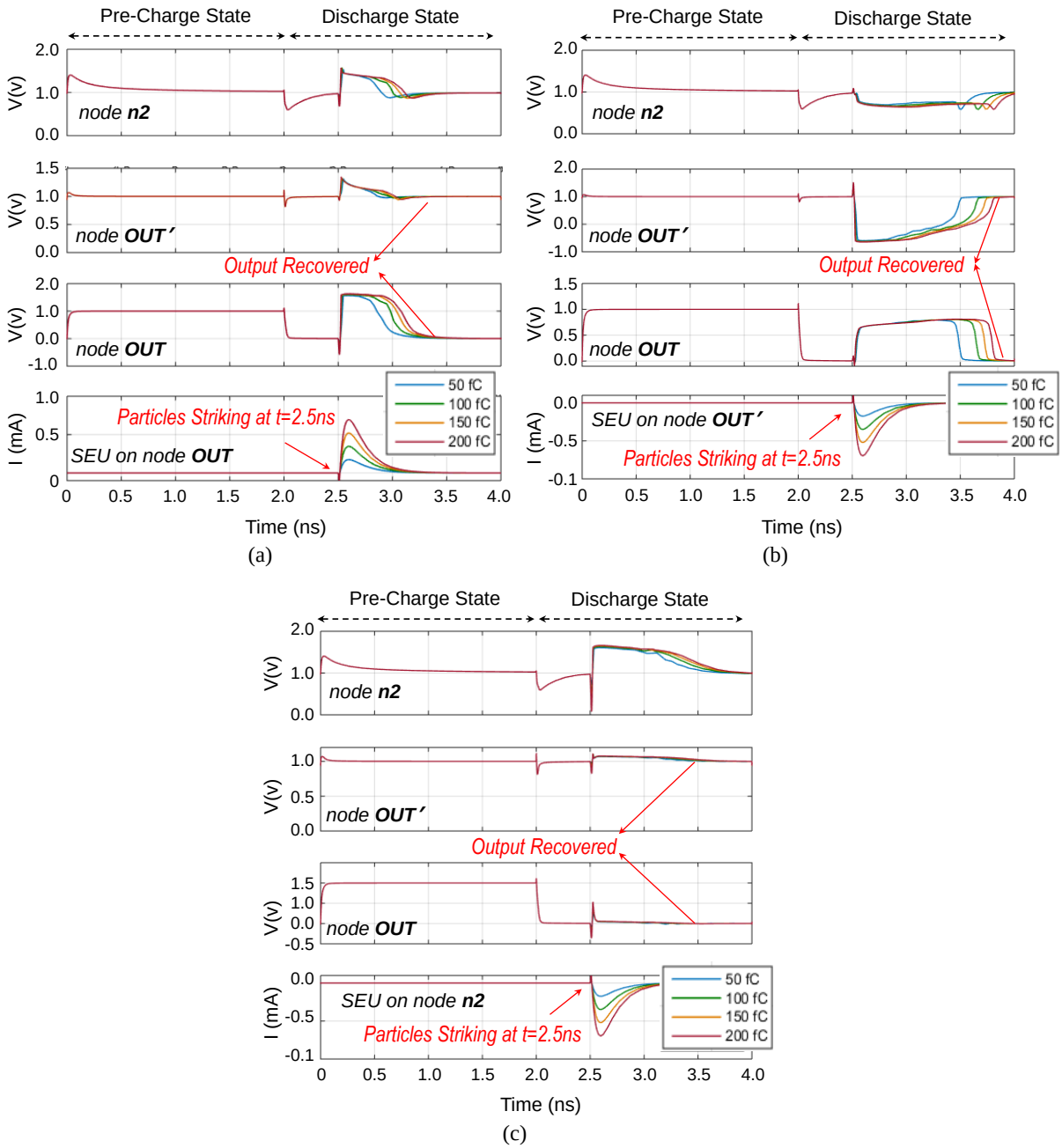

Figure 7. The transient response of the proposed radiation hardened 2-input SHE-MRAM LUT circuit to injected SEUs. (a) SEU on node OUT changes the voltage level of the node to VDD, however since the *n2* node is still near VDD, thus the MN1 transistor remains ON and the injected charge will be discharged through MN1 and the output will be recovered. (b) SEU on node OUT′ changes the voltage of the node to zero, however since OUT node is still near zero, thus the MP2 transistor remains ON and the OUT′ node will be charged to VDD through MP2 and the output will be restored. (c) SEU on node *n2* temporarily changes its voltage to zero, however it will not affect the OUT and OUT′ nodes, and TG1 and TG0 remain ON, thus the *n2* node will be recharged to VDD through TG1 and reference tree.

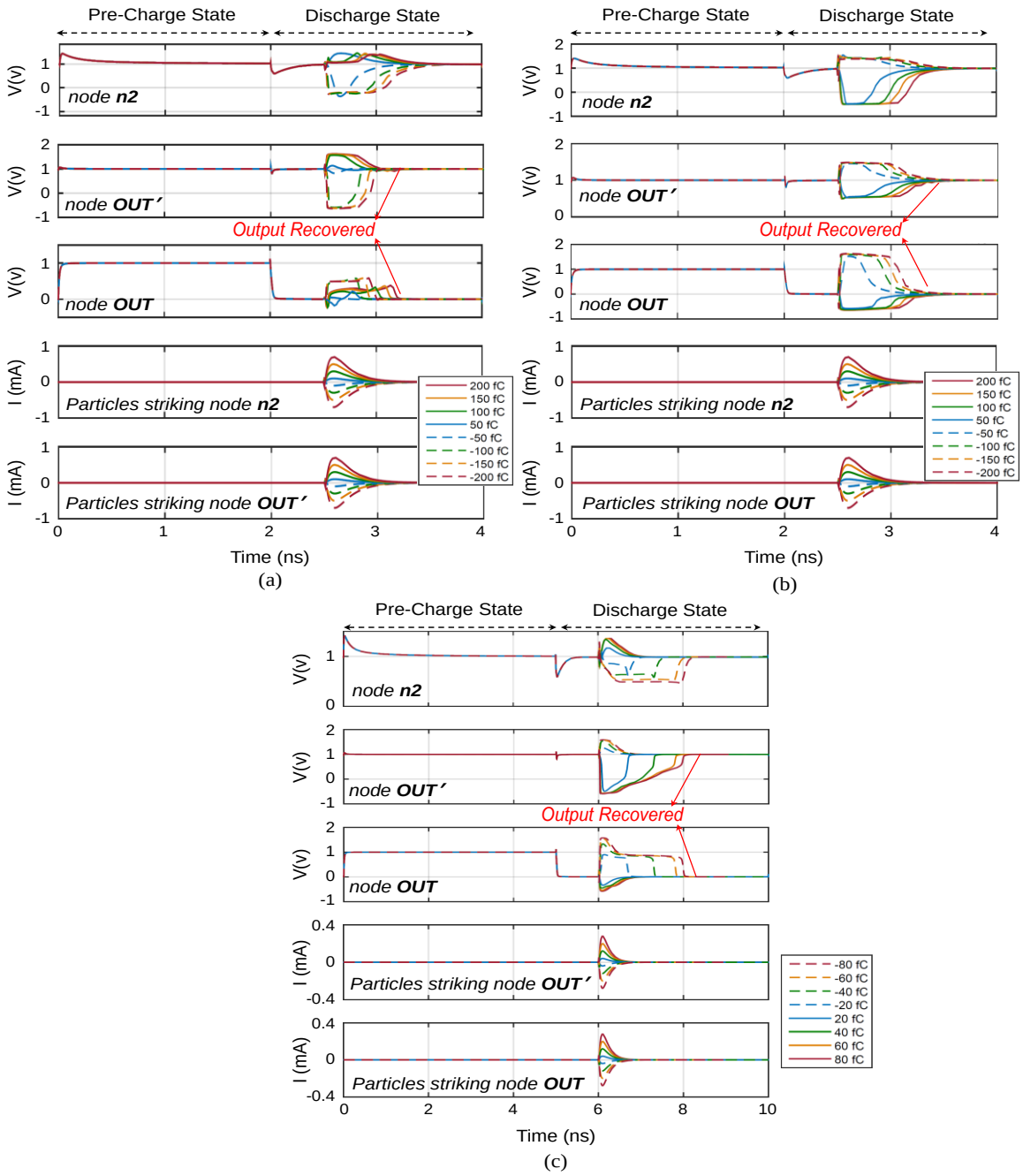

Figure 8. The transient response of the proposed radiation hardened 2-input SHE-MRAM LUT circuit under injection of DNUs. (a) DNU on nodes *n2* and OUT′: the node *n2* can tolerate the injected charge due to the increase in its $Q_{C,}$ and since the OUT node remains near zero the OUT′ node will be charged to VDD through MP2 and the output will be recovered. (b) DNU on nodes *n2* and OUT: the radiation tolerance of node *n2* is increased and will return to VDD, thus the MN1 transistor will become ON and the injected charge will be discharged through MN1 and the output will be recovered. (c) DNU on nodes OUT and OUT′: it will not significantly impact node *n2*, therefore MN1 will remain ON and the injected charge at OUT node will be discharged through MN1 leading to the OUT′ being recharged through MP2. However, since the charge capacity of OUT and OUT′ are not increased in the LUT circuit, they can tolerate the maximum charge of 80 fC that is smaller than the Q_C of the node *n2*.

A comprehensive comparison of the different SHE-MRAM LUT circuits implemented and examined in this paper is listed in table 3. Herein, to provide a fair comparison, all the LUT circuits are simulated by SPICE circuit simulator using the SHE-MRAM model introduced in section 2 along with the 45nm CMOS library with 1.0V nominal voltage. Moreover, since the focus of this paper is only on the sensing circuitry, we have utilized transmission gates (TGs) to implement both select trees and write circuits in all of the investigated LUT designs. The results obtained are listed in table 3. They indicate that the proposed SHE-MRAM LUT circuit can achieve DNU immunity with more than 38% and 60% improvement in power-delay product (PDP) as well as 26% and 50% device count improvement compared to the previous energy-efficient radiation-hardened LUT designs proposed in [29] and [27], respectively. The radiation-hardening ability is realized at the cost of increased PDP values compared to the unprotected MRAM-LUT design proposed in [20]. In [27], three PCSAs are exploited simultaneously along with a voter circuit that votes determines the majority output to return the corrected result even if one of the PCSAs fails due to a radiation-induced fault. The concurrent utilization of three PCSAs for each sensing operation results in a significant component of power consumption. In addition, the sensing delay is increased in this design compared to our proposed circuit, which is mainly caused by the delay overhead of the voter circuit. In [29], additional nodes are added to the sense amplifier circuitry to store output data, which are utilized to recover the nodes impacted by radiation. Introducing extra transistors in the sensing path has induced a significant delay overhead compared to our proposed design that only adds one TG and one NMOS transistor to the sensing path. Moreover, in our design, a higher charge capacity is achieved when increasing the widths of the transistors within the sensing path. This leads to reduced active resistance of the radiation-hardening transistors in the path that can result in reduced sensing delay.

Finally, we have measured the minimum TMR required for MRAM cells in the LUT circuits through SPICE circuit simulation using the Verilog-A model of MRAM devices. As listed in the sixth row of the table 3, the TMR values less than 700% and 400% are unable to provide the required resistive differential between the storage cells and reference cell to ensure the correct sensing operation for the designs introduced in [27] and [29], respectively. This is mainly caused by the active resistance of the extra radiation-hardening transistors added to the sensing circuitry, which can dominate the resistance of MRAM cells. While, our proposed radiation-hardened LUT can properly operate with the TMR values similar to that of the unprotected LUT circuit, due to the decreased number of transistors added to the sensing path. Alternatively, attainment of high TMR values would impose more complex fabrication processes or rely on materials still undergoing development [58].

Table 3. Comparison of the proposed radiation-hardened SHE-MRAM LUT with the previously proposed MRAM-based LUTs. All of the circuits are simulated by SPICE circuit simulator using 45nm CMOS library with 1.0V nominal voltage. The results are obtained for LUT circuits implementing a two input NAND operation when A= 1 and B=1 inputs are applied.

Features	Suzuki et al. [20]	Lakys et al. [27]	Rajaei [29]	Proposed Herein
# of MTJs	12	8	8	5
# of MOSs	30	63	42	30
Delay (ps)	21.18	43.65	51.1	32.97
Power (μW)	0.21	1.08	0.6	0.57
PDP (ps× μW)	4.45	47.14	30.66	18.79
Min. TMR (%)	100	700	400	100
SEU Immune	NO	YES	YES	YES
DNU Immune	NO	NO	YES	YES

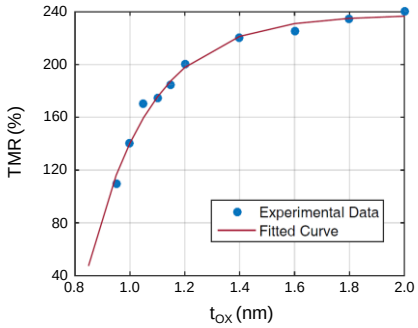

Figure 9. TMR ratio plotted as a function of MgO layer thickness.

4. Process Variation analysis of the proposed radiation-hardened MRAM-based LUT

To increase the radiation-tolerance of the LUT circuit, a number of transistors have been added in the sensing path. This can increase the error rate of the read operation caused by device mismatches due to process variation (PV). Therefore, in this section the effect of PV on various protected and unprotected LUT circuits is assessed. The impact of PV on hybrid CMOS/spin-based circuits results from a combination of systematic variations which are mostly caused by deposition and lithography aberrations, and random variations induced by random doping deviations [59, 60]. Table 4 lists the parameters utilized in this paper for analyzing the PV.

Herein, we have fitted the experimental data extracted in [61] to an exponential curve to obtain the effect of oxide thickness (t_{OX}) variation on TMR values, as shown in figure 9. The relation between the t_{OX} and TMR can be expressed by (17),

$$TMR = K1 - \frac{K2}{K3}(1 - e^{-K3.t_{ox}}) \tag{17}$$

where *K1=-8109.436*, *K2=-37145*, and *K3=4.45* are fitting parameters. The goodness of fit is 0.9718 that is calculated using (18), according to which a value closer to one indicates that the fit is more useful for prediction. N is the number of input data, x_i is the i-th input data, y_i represents its related output, and $F(x_i)$ is the corresponding fitted value for the i-th input data.

$$fit = 1 - \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{y_i - F(x_i)}{y_i}\right)^2} \tag{18}$$

To examine the behavior of LUT circuits in presence of these sources of PV, we have leveraged a Monte Carlo simulation in SPICE, and the results are obtained for 10,000 simulation points. The results exhibit that the radiation hardening is achieved at the cost of increased susceptibility to process variation. In particular, the error rate in the radiation-hardened circuits can increase up to 42.5%, while the unprotected design introduced in [20] exhibits a 12.33% error rate in presence of variations listed in table 4. This occurs

Table 4. Parameters used for a Monte Carlo simulation in SPICE to perform the PV analysis, which are extracted based on the experimental measurement provided in the literature [59, 60].

Device	Parameter	Mean	Std. Dev.
NMOS	V_{TH}	0.34V	10%
PMOS	V_{TH}	-0.23V	10%
MTJ	t_{OX}	0.95nm	5%
	Area	60nm×30nm× π/4	15%

mainly due to the hardening transistors added within the sensing path which result in reduced sensing signals due to inline resistances of the transistors. Accordingly, various methods to enhance the PV-tolerance include increasing the size of the transistors, TMR ratio, and relative resistance of SHE-MRAM devices. Moreover, the advancements in fabrication equipment and process can considerably decrease the impacts of PV, while radiation-hardening through fabrication process remains costly for commercial technologies [54]. The reader is referred to [62] for additional details regarding methods to deal with PV impacts on hybrid CMOS/spin based circuits.

5. Conclusion

In this paper, we have developed a novel radiation-hardened non-volatile LUT circuit using SHE-MRAM devices, in which feedback transistors are used to discharge the disruptive electric charge induced by the radiation particles striking the output nodes of the sense amplifier circuit. The utilization of the extra transistors in hardening circuitry introduced two new sensitive nodes in the sensing circuitry. In order to protect these sensitive nodes, we have enlarged the widths of the transistors connected to them to increase their equivalent capacitances, which is linearly proportional to the critical charge capacity of the nodes. The functionality of our proposed circuit was validated by SPICE circuit simulations using a Verilog-A model of a SHE-MRAM device that has been developed based on precise physical equations. The results obtained exhibit that the proposed LUT circuit can tolerate SEUs and DNUs with injected charge values ranging from -200 fC to +200 fC, which is a typical range that can be injected by the radiation particles striking hybrid CMOS/spin based circuits, as established in the literature. A comparison with the previous protected MRAM-based LUT circuits exhibited that our proposed design can achieve at least 38% and 26% improvements in terms of PDP and device count, respectively. Reduction in sensing delay is significant contributor to the PDP improvement, which is mainly realized by decreasing the active resistance of the hardening circuitry existing in the sensing path. In our design, fewer transistors are added to the sensing path compared to the previous protected circuits. This has resulted in increasing the sensing speed, and eventually decreasing the measured PDP values. However, a comparison with a simple unprotected SHE-MRAM LUT circuit has shown that the DNU-resiliency is achieved at the cost of somewhat higher power consumption and delay, as expected. Finally, we have investigated the behavior of our proposed LUT circuit in presence of CMOS and MTJ process variations. The results indicate a continuum exists for tradeoffs between radiation immunity and the increased susceptibility to the process variation. Taken altogether, the designs and techniques developed herein provide an ensemble of transportable physically-rooted mechanisms to evaluate these tradeoffs across a variety of present and future memory device technologies.

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