Fundamental Metrics of Memory Read Operation & Evaluation of Various Sense Amplifiers

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***Abstract*—This paper evaluates some of the fundamental metrics for memory read operation. The project's name is Fundamental Metrics of Memory Read Operation & Evaluation of Various Sense Amplifiers. A program that displays how many times a word searched by the user appear within a paragraph was created. The user provides the input, and the output is of the number of times the word appears. Of particular interest is the amount of energy used by the program when considering three various sense amplifier designs proposed by researchers. It was found that the VISA sense amplifier had the lowest total energy consumption herein of 93.4278 *fJ*.**

***Keywords*—Sense Amplifier, Energy Aware SA (EASA), Variation Immune SA (VISA), Pre-read and Write Sense Amplifier (PWSA), Body- Voltage Sensing Circuit (BVSC)**

I. PROJECT DESIGN

A program that calculates the number of occurances of a word searched by the user was created. To begin,12 strings are created in the .data segment: *string, word, userinput, colon, and newline*. *String,* contains the paragraph provided by the instructor. *Word,* contains a 10 character space for the user input. The program begins in the .text segment where *la* is used to load the addresses for each string. The first loops converts uppercase letters in the sentence and user input into lowercase. Two counter registers are created. Various loops are used. First, a loop is used to load each byte of the user input and checks if it's within the stringlength. Next, a loop is used to check if *word*, and *string* are equal characters and if the string has reached its end. Each byte of the character string is checked through iteration of the loop. When *word* and *string* are found to be equal, the loop branches to another loop that increases the counter register for the string length and the sentence and both registers are compared. If the characters are not equal, *word* is reset. Each loop is followed by a jump and Syscall performs the I/O function. Three inputs were used to test the program. First, the input provided within the project description: "knight" was utilized. Next, the letter "u" was used as an input to test if the program works for single characters. Lastly, the word "it" was used to test if the program works for other words. An important aspect of the program is the memory bit-cells, which will be discussed in the following sections.

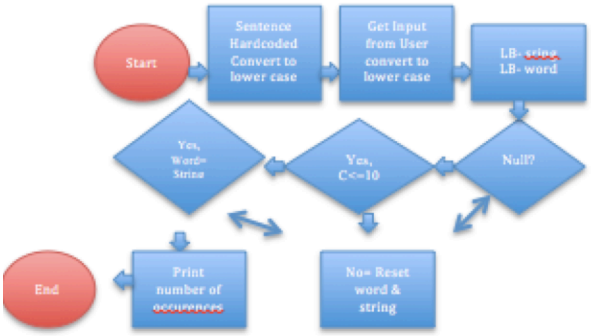

Fig.1: Flowchart of the assembly program.

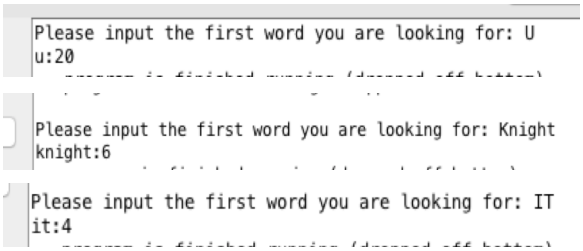

Fig.2: Sample outputs of assembly program.

II. Memory Bit-Cells

Memory cell is an important element of a computer memory. Values within the cell can be accessed by reading and writing using the bit-line, word-line and source-line. Process Variation (PV) is an issue for memory cells because it causes variance in the output performance of all circuits. Researchers have proposed various designs that increase the reliability and efficiency of memory cells. Three designs are used as references in this article in evaluating this matter.

First, in the article, *"Process variation immune and energy aware sense amplifiers for resistive non-volatile memories"* Salehi and Demara propose a method to improve the performance and reliability of separated Pre-Charge Sense Amplifier (PCSA) and Separated Pre-Charge Sense Amplifier (SPCSA). The authors suggest the use of EASA and VISA for such improvements. The key to the authors' design is in using Transmission Gates (TGs) to reduce the effect of PV on the inverters and increase reliability. This process is said to reduce the leakage energy in the path of the Magnetic Tunnel Junction (MTJ) devices. In the pre-charge stage of the design, the signal is low and the TG gates are off, to reduce the leakage energy. When the signal is high, the TG gates turn on. Inverters are important for the circuit due to the presence of PV, thus they are used to amplify the voltage difference of the bit line. Since only one TG is added to the main discharge paths of MTJs, the possibility of bit error occurrence due to PV is reduced. The next article suggests a different design for the same issue.

Second, in the article, *"Design of a Fast and Low-Power Sense Amplifier and Writing Circuit for High-Speed MRAM* by Hochul Lee *et al.*, the authors also propose a method to improve the reliability and performance of the memory cell. Lee proposes a PWSA constructed with latches and logic gates. The circuit is designed to perform a read operation and compare the current MTJ state to the incoming data, which makes the choice on if a write pulse should be applied. The intent of the design is to increase the sensing margin and make it twice as fast as a traditional approach and reduce sensing errors. The author explains that sensing margins and read disturbances are sensitive to the bias voltage applied to the bit line. To maximize the sensing margin the author proposes a current feedback circuit that contains transistors M1, M2, and M3. The design consists of a pre-charge stage during which the sense amplifier charge up both bit-lines to the same potential level while M3 is turned on. When M3 is off, the bit-line enters a discharge stage. In the end, the sensing margin improves and thus guarantees a stable logic swing. The design essentially results in low power, low error rates and high-speed function of MRAM. The PWSA attains two-nanoseconds write and read times and eight-nanoseconds for the data program time. This leads us to the final design suggestion in the third reference.

Lastly, in the article, *"A Body-Sensing-Based Short Pulse Reading Circuit for Spin-Torque Transfer RAMS (STT-RAMs)"* by Fengbo Ren *et al.*, the authors propose yet another design. Ren proposes an SPR circuit structure with a body-voltage sensing circuit for high-speed and reliable reading of scaled STT-RAMs. The author proposes a circuit implementation of a short-pulse reading (SPR) scheme where a sensing current similar in magnitude to the writing current is used to read the MTJ, but it has a shorter pulse width. At one point, the sensing current is disabled for the reading operation to cut off the sensing current thus minimizing its pulse width. The author found that the sensing circuit performs better than other designs in sensing speed for similar energy. The device has a sensing speed that is three-times faster than comparable designs in regards to the sensing margin. The author implements a second stage differential amplifier to improve the read margin and as a result, the suggested SPR circuit performs high-speed readings with the shortest current pulse. The short pulse can reduce read disturbances.

In the end, memory bit-cells are extremely important to a computer's memory. It is important that the cell be accessed in an efficient and reliable manner. Much research is being conducted to improve this task. The reference articles are three of the many proposed methods on improving this task. The next section of this article will analyze the energy consumption of the written code above using the 3 designs proposed by the authors.

III. Results and Discussion

In this section, we calculated the energy consumption of the above mentioned program using the below energy consumption per instruction values:

1) *ALU = 1 fJ*
2) *Branch = 3 fJ*
3) *Jump = 2 fJ*
4) *Memory = Read Energy (Refer to Table I) + Write Energy (50fJ)*
5) *Other = 5 fJ*

With that, the energy consumption for the various categories mentioned above for the program were found to be:

- ALU: 4351 *fJ*
- Branch: 9129 *fJ*
- Jump: 2626 *fJ*
- Other: 2595 *fJ*

The total energy consumption for the memory is listed in the table below for the various sensor amplifiers proposed by the references in section two. Based on the below calculation, the VISA design has the fastest memory read and write operation.

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [1-3].

Design	Energy Consumption For Each Bit-cell's Read Operation
EASA [1]	0.23 fJ
VISA [1]	1.86 fJ
PWSA [2]	36.0 fJ
BVSC [3]	195.5 fJ

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
EASA [1]	96893.67 fJ
VISA [1]	93.4278 fJ
PWSA [2]	1808.28 fJ
BVSC [3]	9819.965 fJ

IV. Conclusion

To conclude, many meaningful things were learned in the process of writing this project some of which are listed below in no particular order:

- How to use various loops to create a program that can search for any word within a hardcoded sentence.
- The importance of memory within a cell.
- Various designs created by researchers to increase the reliability of memory and how they operate.
- The meaning of word line and bit line.
- PV and the role it plays within a memory cell.
- The importance of energy consumption in the design of memory gates
- sense margins and its effect on a program.
- Sense Amplifiers and how it functions in a memory cell
- How to reset a program

All of the designs analyzed within this article have promising attributes, but VISA was found to be the most energy efficient for the search program created and described above.

References

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