Survey of STT-MRAM Cell Design Strategies: Taxonomy and Sense Amplifier Tradeoffs for Resiliency

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Spin-Transfer Torque Random Access Memory (STT-MRAM) has been explored as a post-CMOS technology for embedded and data storage applications seeking non-volatility, near-zero standby energy, and high density. Towards attaining these objectives for practical implementations, various techniques to mitigate the specific reliability challenges associated with STT-MRAM elements are surveyed, classified, and assessed herein. Cost and suitability metrics assessed include the area of nanomagmetic and CMOS components per bit, access time and complexity, sense margin, and energy or power consumption costs versus resiliency benefits. Solutions to the reliability issues identified are addressed within a taxonomy created to categorize the current and future approaches to reliable STT-MRAM designs. A variety of destructive and non-destructive sensing schemes are assessed for process variation tolerance, read disturbance reduction, sense margin, and write polarization asymmetry compensation. The highest resiliency strategies deliver a sensing margin above 300mV while incurring low power and energy consumption on the order of picojoules and microwatts, respectively, and attaining read sense latency of a few nanoseconds down to hundreds of picoseconds for non-destructive and destructive sensing schemes, respectively.

• **Hardware→Spintronics and magnetic technologies**

Additional Key Words and Phrases: Spin-Transfer Torque storage elements, STT-MRAM, Magnetic Tunnel Junction (MTJ), Sense Amplifier, Process Variation, Read/Write Reliability, Design, Performance, Reliability

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1. INTRODUCTION

As technology scales down along with increased demands of greater on-chip integration for larger memory capacities, researchers and designers have responded to the resulting fabrication and operational challenges by embracing new device technologies along with new memory cell designs which leverage their unique advantages. A collection of innovative methods has been developed to increase their reliability and performance. In addition to addressing scalability to technologies beyond 10nm where traditional memory elements such as Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) face significant scaling challenges [Sun, *et al.* 2012], innovations to mitigate the power wall and reduce leakage power consumption occupy the forefront of on-chip memory design considerations. [Bishnoi, *et al.* 2014; Ashraf, *et al.* 2015; Zhao, *et al.* 2009]. Power consumed by memory elements can become a significant portion of total power in active modes whereby the processing cores rely on these memory arrays that are significant contributors to standby mode power consumption [Kultursay, *et al.* 2013; Chen, *et al.* 2016].

To attain these goals and deliver the necessary operational characteristics, emerging memory devices such as Resistive RAM (RRAM), Phase Change Memory (PCM), and Magnetic RAM (MRAM) offer several potential advantages. Among promising devices, the 2014 ITRS Magnetism Roadmap identifies nanomagnetic devices such as Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM), as capable post-CMOS candidates, of which Nano Magnetic Logic (NML), Domain Wall Motion (DWM), Spin-Transfer Torque (STT)-MTJ/Spin Hall Effect (SHE)-MTJ are considered feasibly-implemented [Zand, *et al.* 2016; Roohi, *et al.* 2016; Pyle, *et al.* 2016; Shamsi, *et al.* 2015] whose attributes are depicted in Figure 1. STT-MRAM can offer low read access time, near-zero standby power consumption, and small area requirement. STT-MRAM also offers integration with backend CMOS processes. To embrace their adoption in anticipated applications, a palette of cooperating reliability techniques is identified and compared at the bit-cell level.

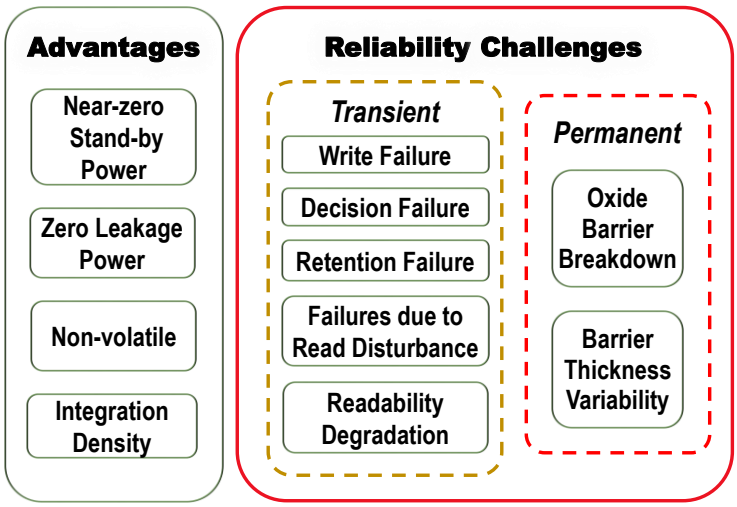

Figure 1: Advantages and reliability challenges of STT-MRAM.

In this survey, the primary focus is on reliability issues that may affect the performance of the STT-MRAM. First, an overview of STT-MRAM functionality and technology aspects is provided in Section 2. In Section 3, reliability issues of the STT-MRAM have been identified and classified. In Section 4, some potential solutions have been presented in terms of a novel taxonomy to organize approaches and their advantages, along with a detailed discussion about previous works. Finally, this review concludes in Section 5 with summary of recommended techniques and rationale.

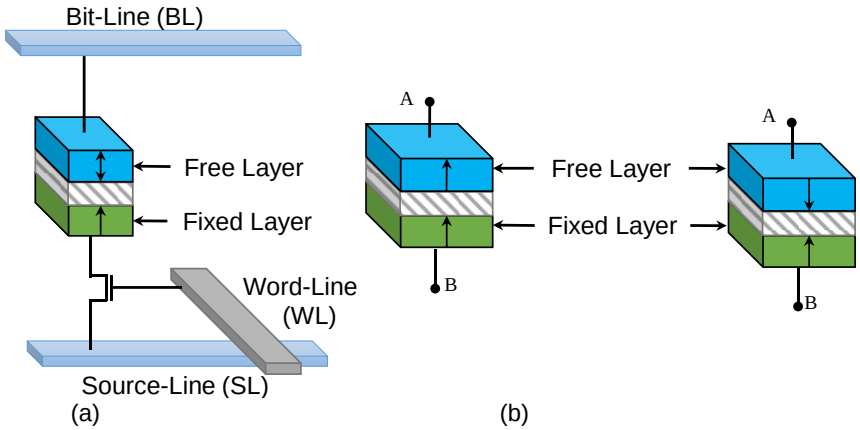

Figure 2: (a) 1T-1R STT-MRAM cell structure, (b) Right: Anti-parallel (high resistance), Left: Parallel (low resistance).

2. STT-MRAM OVERVIEW

Magnetic Tunnel Junction (MTJ) devices are constructed with layered pillars of ferromagnetic and insulating layers to leverage magnetic orientations that can be controlled and sensed in terms of electrical signal levels. Spin-Transfer Torque (STT) switching is one of the most promising alternatives for data storage. MTJ device which consists of two ferromagnetic layers called the reference layer and the free layer and one tunnel barrier oxide layer, is used in STT-MRAM cells to store data as binary values 0 or 1 [Sun, *et al.* 2012] as shown in Figure 2. Figure 2a shows an STT-MRAM cell which has an access transistor that connects the storage device and the bit-line which is the same as DRAM cell, however, an STT-MRAM cell differs from DRAM since the other end of the storage device is connected to the sense line or source line instead of ground. This STT-MRAM cell structure is being known as "one-transistor-one-MTJ (1T-1R)" [Kang, Zhang, Wang, *et al.* 2015; Fong, *et al.* 2016].

As mentioned the stored data in an MTJ can be represented as the magnetic orientation of the free layer compared to fixed layer which these two layers introduce a resistance that shows either 0 or 1. As shown in Figure 2b, identical magnetic orientation results in parallel configuration which introduces a low resistance that can be represented as logical "0" and opposite magnetic orientation results in anti-parallel configuration which introduces high resistance that can be represented as logical "1". Since in STT-MRAM, relative resistance values are used to determine the bit value, then reliable sensing schemes are utilized in order to read the stored data compared to DRAM in which the data is the charge stored in a capacitor and the data is sensed using voltage sensing circuitry. In order to read the stored data, we need to apply a small voltage between source and bit-lines, and using a Sense Amplifier (S.A.) to sense the amount of current flow. Large write amplifiers are used since writing a data to an MTJ, requires significantly larger current than reading the stored value. In order to write into an MTJ cell, we need to apply a large current through the MTJ to change the magnetic orientation of its free layer to form a parallel or an anti-parallel configuration compared to the fixed layer [Fong, *et al.* 2016].

Maintaining lower critical current while having faster speed as well as large energy barrier for high-density device, researchers have proposed data storage using Perpendicular Magnetic Anisotropy (PMA) instead of conventional In-plane Magnetic Anisotropy (IMA) in order to achieve high anisotropy field H_k. This will result in better integration of STT-MRAM into logic circuits [Zhao, *et al.* 2012]. Detailed information about STT-MRAM circuit design and operation can be found in [Sun, *et al.* 2012] and [Kultursay, *et al.* 2013].

STT-MRAM writing has three different operating regions for switching which include Thermal Activation Region where the write current is less than eighty percent of the critical current, Dynamic Reversal Region wherein the write current is greater than eighty percent of the critical current and less than the critical current itself, and Precessional Region where the write current is greater than

the critical current [Kang, Zhang, Wang, *et al.* 2015]. We normally operate this in either the Thermal Activation Region or the Precessional Region. If fast switching is required Precessional Region is a better option compared to Thermal Activation Region since the latter will cause slower switching.

3. RELIABLITY ISSUES OF STT-MRAM

STT-MRAM has several advantages over other emerging memory technologies, however, it faces some distinct reliability challenges involving read and write failures [Bishnoi, *et al.* 2014; Kang, Li, Klein, *et al.* 2014] as listed in this Section. STT-MRAM scalability is greatly influenced and limited due to thermal fluctuations and issues such as MTJ process variations and the CMOS access transistor have had negative effects on STT-MRAM devices. Also, as a result of these issues, demand for an advanced sensing circuit which can provide required sensing margin along with low power operation has been increased as will be addressed in Section 4.

STT-MRAM bit errors can be significantly influenced due to process variations [Emre, *et al.*], which precipitate another important issue that STT-MRAM suffers from as well as suffering from its unique intrinsic thermal randomness. These variations include variation in the access transistor sizes, variation in threshold voltage (V_{th}), MTJ geometric variation, and initial angle of the MTJ. Whereas the effect of variation involving the access transistor on system performance has been investigated in [Eken, *et al.* 2014; Alghareb, *et al.*], here we focus on the process variation of the MTJ cell. The difference between the sensed bit-line voltage and the reference voltage which is known as the Sense Margin will be small due to the wide distribution of MTJ resistance which can also result in a false detection scenario [Zhang, *et al.* 2013]. On the other hand, write speed can be affected and may vary due to the thermal fluctuations during MTJ switching in write operations and this will further aggravate by process variation-induced variability of the switching current [Eken, *et al.* 2014].

Errors due to the STT-MRAM physical nature's failures will be categorized into transient faults and permanent faults as depicted in Figure 3. Transient faults, which can also be described as an incorrect signal condition, is mostly caused by the parameters of free layer such as current density (J_c) and thermal stability factor denoted by Δ. Permanent faults, which can be precipitated by destructive device damage, are initially caused by susceptibility to the sensitive parameters of oxide barrier such as barrier's thickness (t_{ox}) and Tunnel Magneto-Resistance (TMR) ratio [Zhao, *et al.* 2012] which have been expanded with additional parameters in Table 1.

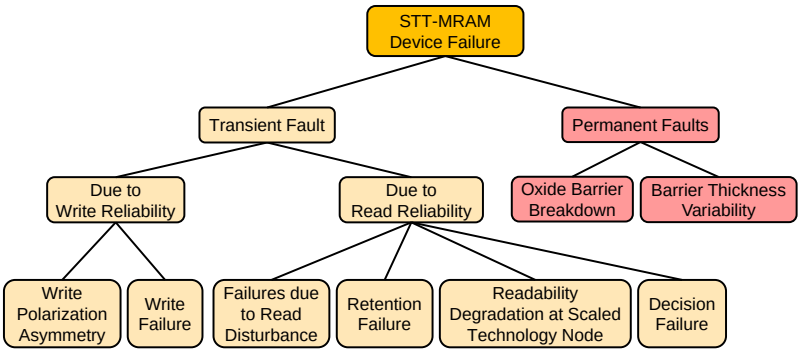

Figure 3: Taxonomy of STT-MRAM Device Failures.

4. RELATED WORKS

Several studies have shown that exposures to permanent and transient faults can be mitigated in various device technologies by employing spatial hardware redundancy, temporal operational redundancy, error correcting codes, and resiliency via active reconfiguration. In order to make reliable STT-MRAM cells which are less vulnerable to alpha-particle-induced transient faults, a variety of design strategies and different considerations have been proposed in [Zhao, *et al.* 2009; Lakys, *et al.* 2012; Zhao, *et al.* 2011; Kawahara, *et al.* 2012; Li, *et al.* 2010]. For instance, in [Kawahara, *et al.* 2012], concept of '1'/'0' dual-array equalized reference is proposed that reduces the error rate by lowering the read current which introduces a precise reference for stable read operation. Research studies have

shown that STT-MRAM memory devices are vulnerable to radiation induced transient faults due to their CMOS peripheral circuit used to read and write in the MTJ cells [Chabi, *et al.* 2014; Yang, *et al.* 2016; Kang, Zhao, *et al.* 2014]. It has been proven experimentally in [Kang, Zhao, *et al.* 2014] that the MTJ device itself is resilient to radiation induced transient faults. In order to reduce the vulnerability of the STT-MRAM devices to radiation induced transient faults caused by elements such as alpha particle, Kang, et al, have designed and examined a novel area and power efficient sensing circuit in [Tsiligiannis, *et al.* 2013]. They have experimentally shown that their design increases the robustness of memory and logic devices using hybrid CMOS/STT-MRAM to radiation induced transient faults such as Single Event Upsets (SEUs) and Multiple Bit Upsets (MBUs) [Tsiligiannis, *et al.* 2013].

Table 1: STT-MRAM Reliability Issues.

Type			Description	Possible Solution(s)
Transient Faults	*Write Reliability Issues*	***Write Failure***	▪ Due to stochastic nature of write process in STT-MRAM ▪ MTJ cell does not switch properly in order to store the required value within write time period	▪ Possible solution can be increasing the write duration ▪ Another possible solution can be increasing write current ▪ These solutions may cause significant amount of power dissipation and area overhead as well as speed degradation
		Write Polarization Asymmetry	▪ P to AP needs higher switching current and suffers from more error rate compared to AP to P switching	▪ Reversed MTJ Connection results in a larger I_{MTJ} for the P to AP switching which alleviates the effect of the I_c asymmetry (I_c (P→AP)/I_c (AP→P) > 1)
	Read Reliability Issues	***Failures due to Read Disturb***	▪ Read and Write share the same path ▪ Unwanted bit-flip during a read operation ▪ Growing with technology scaling ➢ thermal stability factor Δ decreases ➢ critical switching current decreases	▪ Possible solution can be increasing the margin between read and write currents ▪ Increasing the write current is one of the solutions which may not be feasible since write current maintains a high value in STT-MRAM devices. ▪ Also can be done by decreasing the read current which will Increase the read latency and may result in another reliability issue called decision failure ▪ Error Correction Codes (ECC)
		Readability Degradation at Scaled Technology Node	▪ Due to reduction in switching current which will become a greater concern in scaled technology node ▪ Reduction in switching current will limit the upper-bound of sensing current	▪ High read current is required in order to: ➢ Provide enough sense margin ➢ Ensure reliable sensing by excluding the device variation of the sense amplifier ➢ Maintain fast read and reduce read latency ▪ Low read current is required in order to: ➢ Prevent stored data from being upset
		Decision Failure	▪ When reading an MTJ cell, not being able to distinguish whether the stored bit is zero or one	▪ Possible solution can be increasing the read duration ▪ Another possible solution can be increasing read current
		Retention Failure	▪ STT-MRAM had an intrinsic thermal instability which can result to a bit-flip of an MTJ cell's content	▪ One solution at the device-level is exploiting the thermal stability factor Δ ▪ Increasing Δ results in longer read duration, larger current amplitude and increase in number of bits per word during parallel reading
Permanent Faults		***Oxide Barrier Breakdown***	▪ Switching current and switching duration are inversely proportional to each other ▪ High current density J_c is normally required in order to achieve high speed based on: $V = R.A \times J_c$ ▪ In order to have a better switching probability we have to provide a large sensing margin and in order to maintain high current density we can reduce the Resistance Area product (*R.A*) or thickness of the oxide or increase the bias voltage *V* ▪ Each of these solutions can result in the oxide barrier breakdown and shorten the MTJ lifetime	▪ Using Modular Redundancy ▪ In order to prevent permanent faults, oxide thickness variation is required to be less than 5% ▪ Using a low bias voltage for sensing is suggested since the real *TMR* ratio decreases during the sensing operation
		Barrier Thickness Variability	▪ Maintaining low *R.A* value, favorably ultra-thin insulator or oxide barrier is required ▪ MTJ's resistance is proportional to the oxide thickness exponentially. Increase in bias voltage will result in decrease in *TMR* ratio and *TMR* ratio may become less than the resistance Variation Ratio (*VR*) ➢ In this case, sensing margin will be upset by *VR* and permanent faults will occur as a result	

Furthermore, in order to tolerate permanent faults, two solutions have been proposed in [Zhao, *et al.* 2012]. One option is Triple Modular Redundancy using a majority voter and the other option is to resize the active transistors. However, both options introduce area overheads whereas Triple Modular Redundancy requires two additional S.A.s along with a voting circuit, and meanwhile the second option utilizes a larger transistor. While Triple Modular Redundancy is a popular approach for masking soft errors and providing single-fault coverage in various circuits, it incurs roughly three-fold increases in area and energy. In a recent research study in [Kang, Zhao, Wang, *et al.* 2013], Kang et al. have proposed a novel area efficient and high speed Error Correcting Code (ECC) circuit utilizing Orthogonal Latin Square Code (OLSC) in order to increase the reliability of STT-MRAM with the option of adaptability that enables the system to adapt the error correction based on its needs. Moreover, in order to increase the yield of STT-MRAM devices, Kang et al. have introduce an innovative method to sustain permanent and transient faults using an integration of ECC along with Fault Masking (FM) methods which they address as sECC [Kang, Zhang, Zhao, *et al.* 2015]. In addition, in their study by combining sECC method with Redundancy Repair (RR) method, they have successfully managed to further improve and optimize the performance of the emerging STT-MRAM devices. Kang et al. in [Kang, Zhang, Zhao, *et al.* 2015] have managed to repair the permanent faults in the system using redundant elements so called RR, mask transient faults and Single Isolated Faults (SIFs) using sECC.

Alternatively, results of the study in [Zhao, *et al.* 2012] have shown that only resizing the transistors is sufficient for increasing the reliability of the conventional applications, however, for those applications which require extreme sensing reliability, Triple Modular Redundancy technique can be more useful. Considerable amount of research has been performed on improving reliability and performance of STT-MRAM memory devices. In [Xu, *et al.* 2011] the write and read performance of STT-MRAM as last-level on-chip cache have been estimated and analyzed over the processor performance. Moreover, in [Zhou, *et al.* 2009] an early-write-termination scheme was proposed in order to enhance STT-MRAM reliability and reduce STT-MRAM write energy. Furthermore, in [Wang, *et al.* 2008] an implementation of STT-MRAM under different technology nodes has been discussed in which the corresponding process technology and scaling parameters were presented. Furthermore, in order to reduce the probability of accidental bit-flipping and loss of data caused by the current applied during read period, a disturbance-free read scheme was proposed in Gigabit scale STT-MRAM design in [Ono, *et al.* 2009], which, due to process variations of MTJs, this scheme is unable to solve the read failures.

In order to reduce the read disturb probability, [Raychowdhury 2013] has proposed the pulsed read method and [Takemura, *et al.* 2010] has proposed the disruptive reading and restoring scheme. Furthermore, in [Bishnoi, *et al.* 2014], in order to alleviate the read disturb reliability issue, some bit-cell architectures are proposed. Moreover, it has been shown that by increasing the thermal stability factor we can reduce the read disturb rate. However, all of these techniques introduce large area overhead and/or large power dissipation and large delays as mentioned in [Bishnoi, *et al.* 2014].

In general, sensing schemes can be classified into two categories, Destructive and Non-Destructive [Motaman, *et al.* 2015]. Based on the definition presented in this research, Destructive Schemes are more vulnerable to read reliability failures. Non-Destructive Schemes are more tolerant to process variation of reference cell, however, Destructive Schemes, typically, provide smaller read/sense latency as described in the following Sections.

A) Destructive Sensing Schemes

The first category of strategies to mitigate the cost of self-referencing is through consecutive accesses that restore the destroyed value once it has been reliably read. Several self-reference sensing schemes were proposed to overcome reliability concerns due to process variations of MTJs in STT-MRAM. In [Sun, *et al.* 2012] Sun, et al. have analyzed the Conventional Sensing Scheme (CSS) which compares the bit line voltage to a reference voltage to read the value of a memory bit cell under certain conditions. However, as technology shrinks process variation will be increased and will result in significant standard deviations of sense margin that will lead to large read failure probability. As a result, the chip yield in STT-MRAM design is highly limited due to poor robustness of CSS. As

mentioned in [Tanizaki, *et al.* 2006; Jeong, *et al.* 2003], original value stored in an MTJ cell in Conventional Self-Reference Sensing Scheme (CSR), will be compared to a reference value which is stored in the same MTJ in a different write cycle. As it can be found in [Tanizaki, *et al.* 2006; Jeong, *et al.* 2003], CSR consumes a large amount of power and also introduces long latency. Sun, et al. also analyzed CSR in [Sun, *et al.* 2012], which needs two write operations that results in long latency and will lead to large power overhead and can also be destructive to the stored value. Comparing CSR to CSS we can conclude that CSR maintains a higher sense margin with the cost of sacrificing the reliability and performance.

One of the destructive sensing strategies that has been recently used in [Zand, *et al.* 2016] was proposed by Zhao, et al. called Pre-Charge Sensing in [Zhao, *et al.* 2009; Zhao, *et al.* 2012] which uses a Pre-Charge Sense Amplifier (PCSA) and minimizes the read current value and read duration compared with conventional static data sensing. As a result of this action, high reliability will be provided for the STT-MRAM while maintaining the same thermal stability factor. This method, which is called Dynamic Sensing Scheme (DSS) [Zhao, *et al.* 2011], has solved the sensing problem utilizing Dynamic Sensing [Zhao, *et al.* 2012]. In order to reduce the read current required, Lakys, et al. in [Lakys, *et al.* 2012] have used Dynamic Sensing Scheme using two word selection transistors for each MTJ cell in order to perform read operations and switching operations. Also with this method the size of the reading transistor can minimized which can lead to reduction of read current far below the disturb margin down to 10μA. This method introduces some area overhead compared to conventional 1T-1R STT-MRAM cell designs, however, this area overhead is negligible to implement cross-point memories since in these designs the selection transistors are shared among several MTJs within the same word [Lakys, *et al.* 2012]. Lakys, et al. also suggest a method called Self-enable Switching Circuit (SSC) to decrease the impact of stochastic switching in [Lakys, *et al.* 2012] which operates based on relaxing the bias voltage stress on the oxide barrier and utilizing short duration write pulse sequence instead of fixed long writing pulse within switching and sensing operations. This method reduces the probability of oxide breakdown and allows short write pulse durations which will result in reduction in the number of switching operation and this will improve the oxide barrier lifetime [Zhao, *et al.* 2012]. Later in 2012, Ren, et al. have proposed Body Voltage Sensing Circuit (BVSC) in [Ren, *et al.* 2012], which like SSC utilizes a short pulse reading scheme that enables fast sensing operations. They have shown that their design provides improved speed at the cost of sacrificing sense margin and also improves reliability of the read operation against read disturbance.

In order to increase the sensing margin while reducing the latency and improving device variation tolerance of the STT-MRAM cell, Zhang, et al. in [Zhang, *et al.* 2013] have analyzed Regular Differential STT-MRAM Cell Structure (RDAMS). This method uses a differential STT-MRAM cell design including two separate 1T-1R cells which the resistance state of these two are always opposite. This design doubles the maximum sense margin compared to the one of 1T-1R cells (CSS), however, RDAMS capacity is half of the one of the two 1T-1R cells used in this design. In the same research publication, Asymmetric Differential Cell Structure (ADAMS) have been proposed in order to improve the read and write performance of STT-MRAM and also increase the transient fault tolerance compared to RDAMS. This method uses a differential STT-MRAM cell design like RDAMS including two separate 1T-1R cells that one of the MTJ cells is reversely connected to the NMOS transistor. Write latency of ADAMS is the same as RDAMS while maintaining smaller cell area compared to other previous sensing schemes such as CSS, CSR, etc. ADAMS has improved the read latency and has reduced the write error rate [Zhang, *et al.* 2013].

In an extension to a previous research on PCSA, Kang, et al. proposed Separated Pre-Charge Sense Amplifier (SPCA) [Kang, Deng, *et al.* 2014]. Based on their simulation result, SPCA has a similar performance in terms of latency and power and provides better reliability with a small area overhead compared to PCSA proposed in [Zhao, *et al.* 2009]. In another interesting research study proposed in 2014, Eken, et al. in [Eken, *et al.* 2014] introduce a novel strategy called Field-Assisted STT Self-Referencing Scheme (FA-STT) which utilizes an external magnetic field to generate the self-reference sensing signal. This method offers improved process variation resilience and thermal fluctuation tolerance in STT-MRAM and MTJ switching respectively. It also provides a much better read

Table 2: Destructive Sensing Schemes and their attributes.

#	Reference(s)	Approach	Area per Cell (device count)				S.A. Type	Cycle(s) or Stage(s)	Sense Margin ($V_{P/AP}$-V_R)	Read Latency or Sensing Latency	AVG. Energy or Power consumption	Simulation-based or Theoretical
			MTJ	CMOS	Cap	Other						
1	[Tanizaki, *et al.* 2006]	Self-Reference Scheme (SRS)	1	17	2	0	Conventional	2	N/A	Large (130ns)	N/A	Simulation-based TSMC 240-nm
2	[Sun, *et al.* 2012]	Conventional Sensing Scheme (CSS)	1	1	0	0	Conventional	2	Small (~20mv)	Small (2.5ns)	Low (0.8937pJ)	Theoretical
3	[Sun, *et al.* 2012]	Conventional Self-Reference Sensing Scheme (CSR)	1	1	2	0	Conventional	2	Large (76.6mv)	Large (40ns)	High (22.05pJ)	Theoretical
4	[Zhao, *et al.* 2012],[Zhao, *et al.* 2009]	Dynamic Sensing Scheme Using Pre-Charge Sense Amplifier (PCSA)	2	7	0	0	Pre-Charge Sense Amplifier	2	Large (N/A)	Small (~164ps)	Low (~3.17fJ)	Simulation-based TSMC 65-nm
5	[Ren, *et al.* 2012]	Body Voltage Sensing Circuit (BVSC)	3	21	2	1 Res	Conventional	1	Large (195mv)	Small (1ns)	Low (195.5fJ & 300uW)	Simulation-based TSMC 65-nm
6	[Lakys, *et al.* 2012]	Self-enable Switching Circuit (SSC)	2	13	0	0	Pre-Charge Sense Amplifier	2	N/A	Small (<200ps)	Low (N/A)	Simulation-based TSMC 65-nm
7	[Zhang, *et al.* 2013]	Regular Differential STT-MRAM Cell Structure (RDAMS)	2	4	0	0	Conventional	1	Large (N/A)	Small (321.8ps)	N/A	Simulation-based TSMC 45-nm
8	[Zhang, *et al.* 2013]	Asymmetric Differential STT-MRAM Cell Structure (ADAMS)	2	4	0	0	Pre-Charge Sense Amplifier	1	Large (N/A)	Small (266.7ps)	N/A	Simulation-based TSMC 45-nm
9	[Kang, Deng, *et al.* 2014]	Separated Pre-Charge Sense Amplifier (SPCSA)	2	7	0	0	Pre-Charge Sense Amplifier	2	Large (N/A)	Small (~187ps)	Low (~3.84fJ)	Simulation-based TSMC 65-nm
10	[Eken, *et al.* 2014]	Field-Assisted STT Self-Referencing Scheme (FA-STT)	1	5	2	External B-Field	Conventional	2	Large (>20mv)	N/A	N/A	Simulation-based TSMC 45-nm
11	[Motaman, *et al.* 2015]	Slope Detection Sensing Scheme	1	20+4	3	1 Current Source & 2 Switches & 1 Res	Pre-Charge Sense Amplifier	2	Large (N/A)	Large (6.8ns)	Low (150uW)	Simulation-based TSMC 22-nm
12	[Jun-Tae Choi 2016]	Parallel Reading Sense Amplifier (PRSA)	1	18+2	2	1 Switch	Conventional	2	Large (N/A)	Large (<20ns)	N/A	Simulation-based TSMC 180-nm

reliability by improving read sense margin compared to conventional self-reference sensing schemes (CSS, CSR, NDSR, and VDRS) and it significantly reduces the write error rate. Furthermore, Slope Detection Sensing Scheme was suggested by Motaman, et al. in [Motaman, *et al.* 2015] which will also be categorized as destructive scheme in which they have claimed makes the STT-MRAM cell design more reliable against device mismatch and variations. They have discussed that their design has a high sensing robustness due to eliminating the reference comparison. Finally, in a recent research published in 2016, Parallel Reading Sense Amplifier (PRSA) is proposed [Jun-Tae Choi 2016]. This sense amplifier has two sensing steps that the first read step can be performed in parallel with the write operation which reduces the read latency. Authors in [Jun-Tae Choi 2016] have claimed that PRSA offers large sensing margin.

B) Non-Destructive Sensing Schemes

The second category of strategies to mitigate the cost of destructive sensing are being discussed in this Section. Two different design methods that have been demonstrated in [Au, *et al.* 2004] are Low-Power Simple Sensing Circuit and High-Sensitivity Switched-Current Sensing Circuit. It has been exhibited that if low power operation is a priority, then Low-Power Simple Sensing Circuit can offer better performance. On the other hand, if a better magneto-resistance ratio and faster reading is required, then High-Sensitivity Switched-Current Sensing Circuit would be preferred. Even though, High-Sensitivity Switched-Current Sensing Circuit faces challenges compared to Low-Power Simple Sensing Circuit in terms of power consumption, it can provide better performance in terms of speed. Reducing the sensing latency and read disturbance faults are of significant importance when designing a sensing circuit. In order to maintain low read latency while improving the device performance, an Adequate-Reference Scheme is proposed in [Tsuchida, *et al.* 2010] that increases the sense margin of STT-MRAM cells which results in read latency reduction. However, the read disturbance error rate might be increased due to increase in the magnitude of the sensing current. Negative-Resistance Read Scheme (NRRS) which is a current-based sensing scheme has been proposed, fabricated, and tested in [Halupka, *et al.* 2010], and authors have analyzed the non-destructive read operation performed.

Moreover, in [Chen, *et al.* 2010] taking advantage of the different current dependences of the high and the low resistance states of an MTJ, another sensing scheme was proposed called Nondestructive Self-Reference Sensing Scheme (NDSR) [Chen, *et al.* 2010] NDSR utilizes a characteristic of MgO-

based MTJ which is the difference between the current roll-off slope of high and low resistance states. Based on this characteristic we can see that if the MTJ has a high resistance state, the current roll-off slope will be steeper than the low resistance state. It has been proven in [Chen, *et al.* 2010] that although, this method has two read steps, NDSR has reduced the power consumption and significantly improved the read latency by removing the two write operation and performing one write operation instead. However, compared to CSR, NDSR has a smaller sensing margin. Furthermore, in [Chen, *et al.* 2012] they have improved the sensing margin of NDSR utilizing combined magnetic and circuit level enhancements. Researchers have introduced a dual-voltage row decoder with a charge sharing scheme in [Kim, *et al.* 2011]. This scheme has shown reduced read disturbance while providing short sensing latency, resulting in increase in the yield of STT-MRAM devices.

Device variation tolerance and large sensing margin are other important considerations in designing sensing circuits. In a recent research study published in 2012, a sensing scheme have been proposed and discussed [Kim, *et al.* 2012], which can tolerate the process variation in the scaled technology nodes. In order to overcome the issues due to process variation and asymmetry of Read Access Pass Yield (RAPY) of the memory cells, respectively they have developed a Source Degeneration Scheme (SDS) and a Balanced Reference Scheme (BRS). Furthermore, Non-Destructive Variability Tolerant Differential Read Scheme was proposed in [Das, *et al.* 2012] which is targeting the device variation while improving other reliability aspects of the device. This design has the advantage of complimentary inputs as well as providing large sense margin along with better reliability by reducing error rate as mentioned in [Das, *et al.* 2012]. Later in 2012, due to the small sensing margin of the NDSR proposed in [Chen, *et al.* 2010], Sun, et al. came up with a circuit to provide a better sensing margin [Sun, *et al.* 2012]. This method, which is called Voltage-Driven Non-Destructive Self-Referencing Sensing Scheme (VDRS), is more robust than NDSR and maintains a better tolerance on variation of MTJ devices as well as providing a high sense margin. VDSR has low read latency and low power consumption compared to NDSR. In [Sun, *et al.* 2012] authors shown that this method demonstrates the highest STT-MRAM array yield among all existing sensing schemes of STT-MRAM design. In another research to improve the STT-MRAM reliability, Offset-Tolerant Triple-Stage Sensing Circuit has been proposed by Kang, et al. in [Kang, Zhao, Klein, *et al.* 2013]. They have verified that their design can reduce the device errors due to process variation and read disturbance which increases the STT-MRAM reliability in scaled technology nodes while providing large sense margin.

In 2014, Kim, et al. in another research have introduced Split-Path Sensing Circuit (SPSC) [Kim, Na, *et al.* 2014] and have shown that using variable reference voltage, their design consumes less energy compared to Highly-Symmetric Cross-Coupled Current Mirror (HSCC) proposed in [Maffitt, *et al.* 2006], SDSC [Kim, *et al.* 2012], and BVSC [Ren, *et al.* 2012] while providing a large enough sensing margin. Another sensing scheme which can tolerate the process variation in the scaled technology nodes and improve the reliability of STT-MRAM, has been proposed and discussed in [Na, *et al.* 2014]. In this research study, authors have suggested an Offset-Canceling Triple-Stage Sensing Circuit (OCTS) in order to overcome the issues due to process variation and asymmetry of RAPY of the memory cells that can operate with low currents which will result in avoiding read disturbance. Moreover, in [Kim, Ryu, *et al.* 2014] Self-Body Biasing Sensing Circuit (Self-BB) is proposed, which is thought to also tolerate issues due to process variation and asymmetry of RAPY of the memory cells while providing better sensing margin compared to conventional sensing schemes and performing fast sensing operations.

Read disturb faults and device variation are highly relative to the scaling of the technology node which both can affect the device reliability in a negative way. The first step in order to prevent the read disturb faults effectively is to detect them. In [Bishnoi, *et al.* 2014], a circuit has been proposed that has the ability to detect the read disturb fault utilizing a self-test mechanism that is supposed to validate its behavior which is called Read Disturb Detection Scheme (RDD). It has been shown that using this method, up-to 95% of the total read disturb faults can be detected while maintaining negligible area and power overhead. In order to reduce device variation effect on STT-MRAM reliability, a variation-tolerant high-reliability sensing scheme has been introduced and designed which is shown to increase the sensing margin with the cost of more delay and loss of speed [Kang, Li,

Table 3: Non-Destructive Sensing Schemes and their attributes.

#	Reference(s)	Approach	Area per Cell (device count)				S.A. Type	Cycle(s) or Stage(s)	Sense Margin ($V_{P/AP}$-V_R)	Read Latency or Sensing Latency	AVG. Energy or Power consumption	Simulation-based or Theoretical
			MTJ	CMOS	Cap	Other						
1	[Au, *et al.* 2004]	Low-Power Simple Sensing	5	15+ 2×SA	0	0	Conventional	2	N/A	Large (28ns)	High (6.23mW)	Simulation-based TSMC 600-nm
2	[Au, *et al.* 2004]									Large (16ns)	High (1.75mW)	Simulation-based TSMC 180-nm
3	[Au, *et al.* 2004]	High-Sensitivity Switched-Current Sensing Circuit	5	31+ 2×SA	0	0	Conventional	2	N/A	Large (16ns)	High (8.99mW)	Simulation-based TSMC 600-nm
4	[Au, *et al.* 2004]									Large (12ns)	High (5.70mW)	Simulation-based TSMC 180-nm
5	[Maffitt, *et al.* 2006],[Kim, Na, *et al.* 2014]	Highly Symmetric Cross-Coupled Current Mirror (HSCC)	5	16	0	0	Conventional	1	N/A	Small (3ns)	Low (0.76pJ)	Simulation-based TSMC 45-nm
6	[Tsuchida, *et al.* 2010],[Chankyung Kim, *et al.* 2015]	Adequate-Reference Scheme (ARS)	6	26	0	1 Current Source	Conventional	1	N/A	Large (11ns)	N/A	Simulation-based TSMC 65-nm
7	[Halupka, *et al.* 2010]	Negative-Resistance Read Scheme (NRRS)	1	14+ 2×SA	0	1 Res	Conventional	1	N/A	Large (8ns)	N/A	Simulation-based TSMC 130-nm
8	[Chen, *et al.* 2010],[Chen, *et al.* 2012]	Nondestructive Self-Reference Sensing Scheme (NDSR)	1	5	1	2 Res	Conventional	2	Large (>20mv)	Large (15ns)	Low (1.04pJ)	Simulation-based TSMC 130-nm
9	[Kim, *et al.* 2011]	Disturbance-Free Scheme	3	25+SA	0	0	Conventional	1	N/A	Large (8ns)	N/A	Simulation-based TSMC 45-nm
10	[Kim, *et al.* 2012]	Source Degenerating Scheme and Balanced Reference Scheme (SDSC)	3	19	0	0	Conventional	1	N/A	Small (1.9ns)	Low (134.4fJ)	Simulation-based TSMC 65-nm
11	[Das, *et al.* 2012]	Non-Destructive Variability Tolerant Differential Read Scheme	4	11+SA	0	0	Conventional	1	N/A	N/A	N/A	Simulation-based TSMC 22-nm
12	[Sun, *et al.* 2012]	Voltage-Driven Non-destructive Self-Reference Sensing Scheme (VDRS)	1	9	2	0	Conventional	2	Large (>45mv)	Large (15ns)	Low (12.08pJ)	Simulation-based TSMC 130-nm
13	[Kang, Zhao, Klein, *et al.* 2013]	Offset-Tolerant Triple-Stage Sensing Circuit	5	8+2×SA	2	0	Conventional	3	N/A	Small (4.3ns)	Low (40fJ)	Simulation-based TSMC 40-nm
14	[Kim, Na, *et al.* 2014]	Split-Path Sensing Circuit (SPSC)	5	16	0	0	Conventional	1	N/A	Small (3ns)	Low (0.21pJ)	Simulation-based TSMC 45-nm
15	[Kim, Ryu, *et al.* 2014],[Kang, Li, Klein, *et al.* 2014]	Offset-Canceling Triple-Stage Sensing Circuit (OCTS)	5	15+14	3	7 Switches	Conventional	3	Large ~45.21mv	Large (6.4ns)	Low (395.5fJ)	Simulation-based TSMC 45-nm
16	[Kim, Ryu, *et al.* 2014]	Self-Body Biasing Sensing Circuit (Self-BB)	3	15	0	0	Conventional	1	N/A	Small (2ns)	N/A	Simulation-based TSMC 45-nm
17	[Bishnoi, *et al.* 2014]	Read Disturb Detection Scheme (RDD)	6	37	0	0	Pre-Charge Sense Amplifier	1	N/A	Small (1.2ns)	Low (N/A)	Simulation-based TSMC 65-nm
18	[Kang, Li, Wang, *et al.* 2014]	Variation-Tolerant High-Reliability Sensing Scheme	5	17+14	3	7 Switches	Conventional	3	Large (~227.54mv)	Small (3ns)	N/A	Simulation-based TSMC 40-nm
19	[Kang, Li, Klein, *et al.* 2014]	Variation-Tolerant and Disturbance-Free Sensing Circuit	5	17+14	3	7 Switches	Conventional	3	Large (~102.14mv)	Small (3ns)	N/A	Simulation-based TSMC 40-nm
20	[Chankyung Kim, *et al.* 2015],[Yang, *et al.* 2016],[Tsiligiannis, *et al.* 2013]	Covalent-Bonded Cross-Coupled Current-Mode Sense Amplifier (CBSA)	3	31+SA	0	0	Conventional	2	N/A	Large (9.1 ns)	N/A	Simulation-based TSMC 65-nm
21	[Lee, *et al.* 2015]	Pre-Read and Write Sense Amplifier (PWSA)	1	46	0	1 Res	Conventional	4	Large (360mv)	Small (2ns)	Low (18uW)	Simulation-based TSMC 65-nm
22	[Yang, *et al.* 2015]	Body-Biasing Feedback Circuit	3	12+SA	0	0	Conventional	1	Large (N/A)	Small (N/A)	N/A	Simulation-based TSMC 40-nm
23	[Kang, Pang, *et al.* 2015]	Dynamic Referencing Sensing Scheme (DRS)	5	11	0	0	Conventional	1	Large (~22.31mv)	N/A	N/A	Simulation-based TSMC 40-nm
24	[Ran, *et al.* 2015]	Read Disturb Detection Scheme (RDD)	5	23	0	0	Latch-type Voltage Comparator	1	N/A	Small (4ns)	N/A	Simulation-based TSMC 28-nm
25	[Kyungmin Kim, *et al.* 2015]	Degenerated Cross-coupled Sensing Circuit (DCCSC)	3	33	0	0	Degenerated Cross-coupled Sensing Circuit	1	Large (>495.3mv)	Small (2ns)	Low (0.195pJ)	Simulation-based TSMC 65-nm

Wang, *et al.* 2014]. This design includes three stages of sensing. One of these stages is a pre-amplifying stage which utilizes a charge transfer amplifier to amplify the voltage difference between the reference MTJ cell and main MTJ cell. In another research publication, Kang, et al. [Kang, Li, Klein, *et al.* 2014] utilized a modified charge transfer stage and a source follower amplifier which makes the design more reliable against device mismatch and variations, prevents read disturbance, and further improves the sense margin. In a recent research publication, Covalent-Bonded Cross-Coupled Current-Mode Sense Amplifier (CBSA) has been proposed and fabricated in [Chankyung Kim, *et al.* 2015]. In this design the source lines are merged throughout the whole memory array in order to make the design more compact in terms of area efficiency. Authors have shown that this design reduces the mismatch sensitivity of the cross-coupled latch in the sense amplifier design.

Providing reliable solutions are valuable, however if the power consumption of a reliable design is high, then that design cannot be a good alternative. In an effort for maintaining low power while having a reliable design, Lee, et al. have recently proposed Pre-Read and Write Sense Amplifier (PWSA)

which they have shown that due to its pre-read stage, then the write error rate can be controlled. Based on their result shown in [Lee, *et al.* 2015], their design provides a fast reading circuit that consumes a small amount of power and increases the reliability through controlling and reducing the write error rate.

Another source of reliability exposure that results in read disturbance or read failure, is the thermal instability. In [Yang, *et al.* 2015], a Body-Biasing Feedback Circuit is proposed to improve the sensing margin and reliability of the STT-MRAM against thermal instability which will further reduce read failures and disturbance. In [Kang, Pang, *et al.* 2015], authors have introduced Dynamic Referencing Sensing (DRS) scheme in order to prevent read disturb reliability issue. Based on their design the area overhead is negligible due to the fact that the sensing circuitry is shared among the memory cells along the bit-line or word-line. In their design they manipulate the sensing circuit with regards to the sensed signal and adaptively configure the resistance of the load transistor's resistance. In a recent research [Ran, *et al.* 2015], another RDD circuit has been demonstrated and examined. Based on the fact that if a read disturb occurs, then the read current will have a sudden change due to change in the resistance of the MTJ and also knowing that this change will be in a unidirectional fashion either from P to AP or from AP to P, they have designed a circuit that can detect the read disturb fault. However, they have also mentioned that there exists a small latency before activation of the RDD circuit which if any read disturb fault occurs within the duration of the latency it will not be detected. They have also exhibited that the probability if detecting the read disturb will increase in their design if TMR ratio increases and/or if the detection time increases. The area overhead of this RDD design is negligible compared to the area of the chip as claimed in [Ran, *et al.* 2015]. Finally, a Degenerated Cross-Coupled Sensing Circuit (DCCSC) is been proposed in [Kyungmin Kim, *et al.* 2015] which is proven to have wide sense margin while consuming small amount of energy with a fast sensing time. They have designed a new reference cell that exhibited increased reliability against device mismatch and variations, and ameliorates read disturbances.

5. CONCLUSION

Each of the solutions to the reliability problems of the STT-MRAM leverage different properties of the MTJ switching behavior. Figure 4 depicts the Read/Sense latency vs. Sensing Margin of STT-MRAM Destructive Sensing Schemes which have been proposed as time progressed from the initial designs on the left side of the plot to current designs on the right side of the plot. Recent preferred designs are able to achieve less than 5ns read sensing latency while maintaining wide sensing margins. Figure 5 depicts these values for Non-Destructive Sensing Schemes. Non-Destructive schemes have emphasized lower energy consumption as opposed to maintaining sensing margins. These offer a feasible guide to the circuit designer seeking to trade-off the range of approaches available based on these important parameters of reliability, performance, and energy.

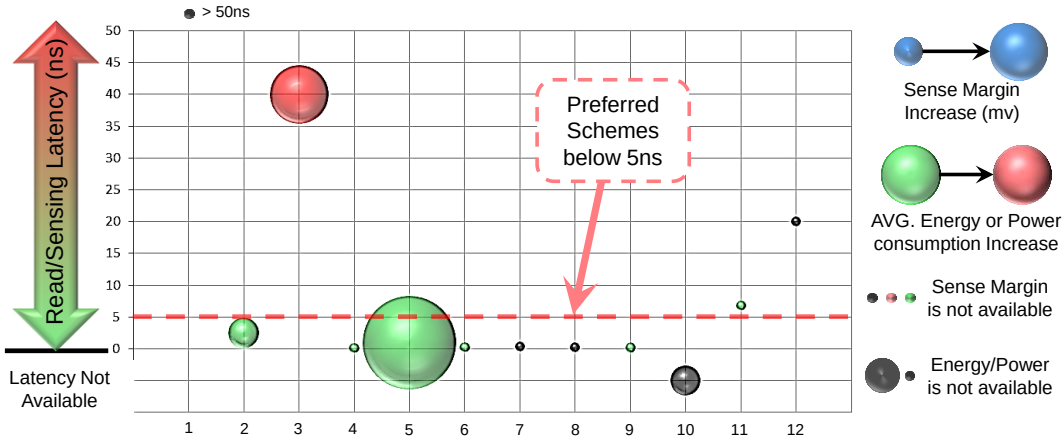

Figure 4: Read Sense Latency vs. Sensing Margin of STT-MRAM Destructive Sensing Schemes and Circuit Designs (with the same order as listed in # column in Table 2).

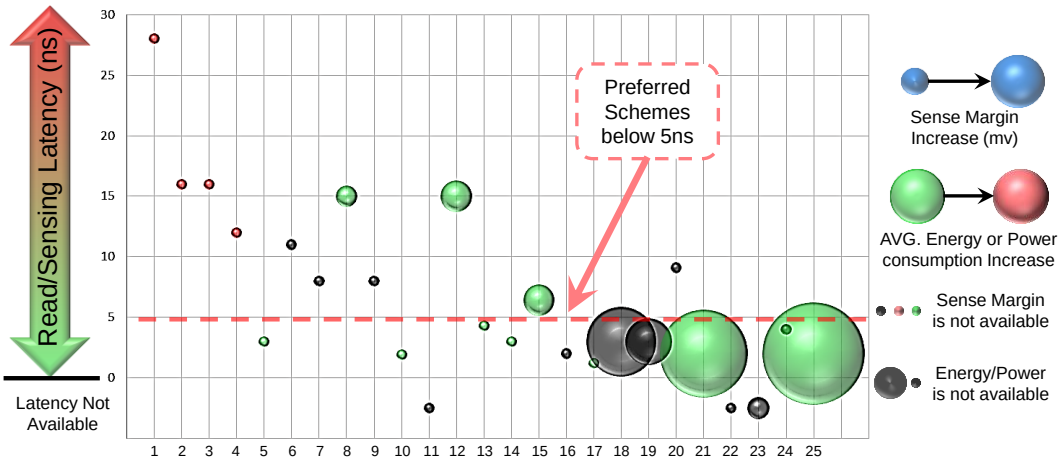

Figure 5: Read Sense Latency vs. Sensing Margin of STT-MRAM Non-Destructive Sensing Schemes and Circuit Designs (with the same order as listed in # column in Table 3).

Table 2 and Table 3 list detailed numerical values for all of the schemes reviewed in this paper and also a description of qualitative attributes. Performance is seen to span in three different ranges across all proposed design strategies. The highest resiliency strategies deliver a sensing margin above 300mV while incurring low power and energy consumption on the order of picojoules and microwatts, respectively, with read sense latency of a few nanoseconds down to hundreds of picoseconds for non-destructive and destructive sensing schemes, respectively.

Some notable inflection points between reliability and performance occur based on whether tolerating process variation is of primary importance. In that case, destructive techniques such as [Eken, *et al.* 2014; Zhang, *et al.* 2013; Motaman, *et al.* 2015; Kim, *et al.* 2012; Das, *et al.* 2012; Na, *et al.* 2014; Kim, Ryu, *et al.* 2014; Kang, Li, Wang, *et al.* 2014; Chankyung Kim, *et al.* 2015; Kang, Li, Klein, *et al.* 2014; Kyungmin Kim, *et al.* 2015] are recommended. On the other hand, if tolerating read disturbance is a governing requirement then [Bishnoi, *et al.* 2014; Na, *et al.* 2014; Ren, *et al.* 2012; Lakys, *et al.* 2012; Kang, Li, Klein, *et al.* 2014; Halupka, *et al.* 2010; Kyungmin Kim, *et al.* 2015; Kim, *et al.* 2011; Kang, Zhao, Klein, *et al.* 2013; Yang, *et al.* 2015; Ran, *et al.* 2015] techniques are believed to be more promising. Furthermore, if wide sensing margin is required techniques such as [Eken, *et*

Table 4: Suggested Sensing Schemes based on their attributes.

Attribute	***References***
Process Variation Tolerant	[Eken, *et al.* 2014],[Zhang, *et al.* 2013],[Motaman, *et al.* 2015],[Kim, *et al.* 2012],[Das, *et al.* 2012],[Na, *et al.* 2014],[Kim, Ryu, *et al.* 2014],[Kang, Li, Wang, *et al.* 2014],[Kang, Li, Klein, *et al.* 2014],[Chankyung Kim, *et al.* 2015],[Kyungmin Kim, *et al.* 2015]
Read Disturb Reduction	[Bishnoi, *et al.* 2014],[Lakys, *et al.* 2012],[Ren, *et al.* 2012],[Halupka, *et al.* 2010],[Kim, *et al.* 2011],[Kang, Zhao, Klein, *et al.* 2013],[Na, *et al.* 2014],[Kang, Li, Klein, *et al.* 2014],[Yang, *et al.* 2015],[Ran, *et al.* 2015]
Wide Sense Margin	[Sun, *et al.* 2012],[Zhao, *et al.* 2012],[Eken, *et al.* 2014],[Zhang, *et al.* 2013],[Zhao, *et al.* 2009],[Motaman, *et al.* 2015],[Chabi, *et al.* 2014],[Ren, *et al.* 2012],[Kang, Deng, *et al.* 2014],[Jun-Tae Choi 2016],[Tsuchida, *et al.* 2010],[Chen, *et al.* 2012],[Das, *et al.* 2012],[Kang, Zhao, Klein, *et al.* 2013],[Kang, Li, Klein, *et al.* 2014],[Kyungmin Kim, *et al.* 2015]
Write Polarization Asymmetry Reduction	[Eken, *et al.* 2014],[Zhang, *et al.* 2013],[Lee, *et al.* 2015]
Yield Increase	[Sun, *et al.* 2012],[Kim, *et al.* 2011],[Kim, *et al.* 2012]

al. 2014; Zhang*, et al.* 2013; Sun*, et al.* 2012; Motaman*, et al.* 2015; Zhao*, et al.* 2009; Zhao*, et al.* 2012; Das*, et al.* 2012; Ren*, et al.* 2012; Tsuchida*, et al.* 2010; Kang, Li, Klein*, et al.* 2014; Kyungmin Kim*, et al.* 2015; Kang, Deng*, et al.* 2014; Chen*, et al.* 2012; Jun-Tae Choi 2016; Kang, Zhao, Klein*, et al.* 2013] could be a preferable, despite increased energy dissipation of some of the approaches. In addition, for robust and reliable designs to reduce write polarization asymmetry, sensing schemes such as [Eken*, et al.* 2014; Zhang*, et al.* 2013; Lee*, et al.* 2015] can be good candidates. Finally, if increasing the yield is the main goal then [Sun*, et al.* 2012; Kim*, et al.* 2012; Kim*, et al.* 2011] techniques can be promising alternatives for conventional sensing schemes. These criteria are also summarized in Table 4 along with the approaches that correspond with each objective.

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