In-Depth Analysis of the Optimization in Memory Write Operations between years 2004-2017

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Abstract—

In this paper, several energy-efficient Memory Write circuit designs are discussed from different articles that were published between the years 2004-2017. The overall purpose of this paper is to analyze the fundamental circuits proposed for the memory bit-cells in these designs. These designs are based on relative modern efficient circuits to reduce the energy consumption in memory access-related operations. Additionally, this paper explores fundamental concepts such as Magnetic Tunnel Junctions (MJTs), non-volatile memory and Spintronic-based memory cells, which are used in the memory block as storage elements. The design number 3 provided the least energy consumption at 369980 fJ for the implemented code.

Keywords— Memory Write; Static Random-Access Memory (SRAM); Magnetic Random-Access Memory (MRAM); Spin-Hall Effect (SHE); Magnetic Tunnel Junction (MTJ); Spin-based Memory; Spin-Transfer Torque; Non-Volatile Memory.

I. PROGRAM DESIGN

The program design in this project required the implementation of a program able to count the occurrences of specific uppercase and lowercase letters in a given string. Initially, the test string was saved under the label string: in .data section along with the space reserved for 10 characters inserted by the user. First, the counter (in register $t0) was initialized to 0. Next, the base address value of string was loaded into register $t1 with 0 offset and the base address value of the input into register $t2. Furthermore, the loop process started by verifying if $t1 was equal to 0; if it was found to be true, then it exits the loop and outputs the result; if it was found to be false, then the loop starts. The next step was to check if $t2 was equal to 10; if yes, it jumps to label counter where the counter is incremented by 1 and the input is restarted. If not; the loop continues and the code proceeds to lowercase and uppercase possibilities between the characters present in the string and the characters from the input word by the user. If a match is found, the string (in register $t1) is incremented by 1, as well as the word (in register $t0). If a match is not found, the string (in register $t1) is incremented by 1 and the input is restarted. If none of the checks are satisfied, it means the null terminated character has been

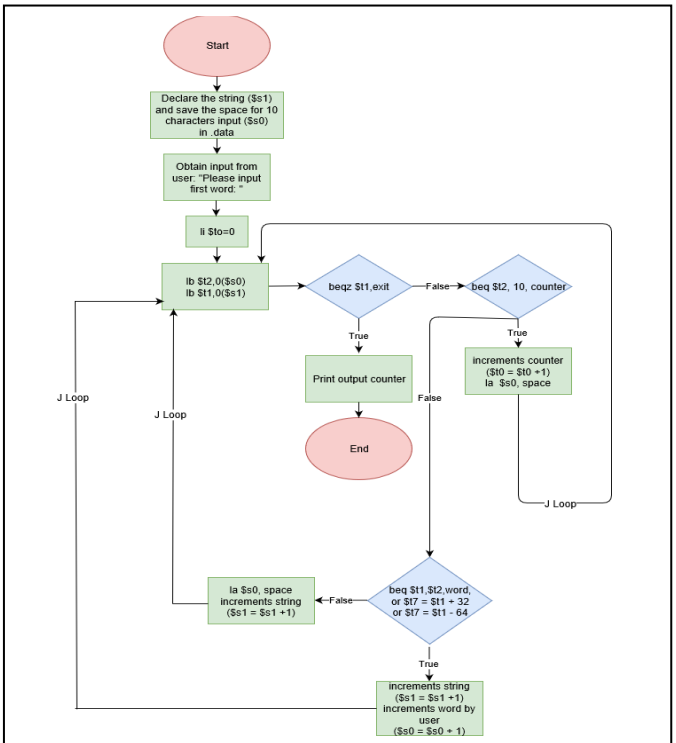

Fig.1: Flowchart of the assembly program.

```
Please input first word: KNIGHt

 KNIGHT: 6
-- program is finished running (dropped off bottom) --
```

```
Please input first word: sTudeNTS12

 KNIGHT: 0
-- program is finished running (dropped off bottom) --
```

```
Please input first word: U c F

 KNIGHT: 0
-- program is finished running (dropped off bottom) --
```

Fig.2: Sample outputs of the assembly program.

reached where the program exits the loop and prints out the number of the input occurrences in the sample string.
In order to properly test the functionality of the implemented code in Project 3, three different test strings were selected as follows:

Words	Purpose and Outcome
KNIght	Test word with uppercase and lowercase letters; which the implemented program correctly identified the six occurrences.
sTudenTs12	Test word with numbers. As expected, the program is uppercase and lowercase sensitive; but outputs zero due to the numbers.
U c F	This word is present in the string twice. However, by adding the two spaces; the program outputs the number of occurrences as zero.

II. Memory Bit-Cells

Memory Write is a type of memory-access operation that enables a user to write to specific memory bit-cells (storage locations) within a device. Various circuits designs have been proposed throughout the years to reduce the energy consumption and time to process a memory write operation. For instance, [1] discusses an energy-efficient write scheme for a Spin-hall effect magnetic tunnel junction (SHE-MTJ); a transmission gate (TG) design is proposed because of its symmetric switching behavior due to both nMOS and pMOS transistors being ON during write operations. The results in this paper show a higher clock frequency, while providing a significant energy consumption reduction. In contrast, [2] analyzes the feasibility of minimizing the overall switching current through SHE-MRAMs for large cache memories. A proposed model was implemented to conduct the read and bidirectional write circuitry where the SHE-MRAM was found to have a 4.7x shorter write time than a standard STT-MRAM, despite the cache size [2].

Furthermore, [3] discusses a circuitry design for the experimental non-volatile memory device Racetrack memory (RM) with the usage of thin films MJTs due to the high and low resistance values [8] and an industrial CMOS design kit. Both serial and parallel operations of the RM were achieved. Another noteworthy optimization design for on-chip caches is the Spin-transfer torque magnetic RAMs (STT MRAMs), which was two bit-lines and one source-line. [4] proposes an optimal and detailed analysis of this layout where the access transistor width (WFET), a critical parameter in a design, was incremented to a maximum value in the metal pinch limited (MPL) region. This increment along with a reduction in the read voltage, allowed a 2X improvement in the memory write margin [4].

A considerable factor was the cell area since the cell characteristics are deeply related to the (WFET) [5]. Therefore, several cases were considered in the STT MRAM cell optimization and the effects in the read disturb margin (RDM). Similarly, a non-volatile memory called spin-RAM also uses the Spin-transfer torque magnetic effect (STT) in a MJT [6] where outstanding results were obtained, specifically in memory-access operations such as read/write. A write current as low as 200 muA was accomplished at a relatively low power.

Finally, [7] is a patent registered in by the United States Patent and Trademark Office (USPTO) in 2004, which comprises a circuit to optimize the power consumption present in the memory write operations through thinly capacitively-coupled thyristor (TCCT)-based memory cells. This invention provides an emerging technology method to optimize read-over write operations and other memory access-related operations.

III. Results and Discussion

In this section, the energy consumption per instruction in femtojoules (fJ) values are displayed to calculate the overall energy consumption for the assembly program implemented using the designs provided in [1-4].

1) *ALU = 1 fJ*
2) *Branch = 3 fJ*
3) *Jump = 2 fJ*
4) *Memory = Read Energy (1 fJ) + Write Energy (Refer to Table I)*
5) *Other = 5 fJ*

Table I: Energy consumption for a single bit-cell write operation in the designs provided in [1-4].

Design	Energy Consumption For Each ALU Instruction
[1]	360 fJ
[2]	300 fJ
[3]	280 fJ
[4]	420 fJ

The total energy consumption of the assembly code is calculated with the following formula:
Total Energy Consumption = (ALU × ALU Instructions) + (Branch × Branch Instructions) + (Jump × Jump Intructions) + (Memory × Memory Intructions)+(Other × Other Intructions).
By utilizing the MARS assembly “Instruction statistics” tool, the number of instructions for each component was found.

The total Energy Consumption for designs [1-4] are reflected in Table II as seen below:

Table II: Total Energy consumption for the assembly program using designs provided in [1-4].

Design	Total Energy Consumption
[1]	471260 fJ
[2]	395300 fJ
[3]	369980 fJ
[4]	547420 fJ

From this table, it is observed that design [4] provides the highest energy consumption for the assembly program; whereas, design [3] proved to be the most energy efficient design. Even though, design [4] achieved a 2X improvement in the memory write margin through the incrementation of the access transistor width (WFET), this design came at the cost of degradation in the **c**ell tunneling magneto-resistance (CTMR) and resulted as the least efficient design with an energy consumption of 420 fJ per single bit-cell write operation.

Design [3] did a complex analysis on the Racetrack Memory (RM) compact model based on magnetic domain walls (DW) motion where three main aspects were considered: voltage source for current generation, as an efficient current is a critical part of RM, current sources for current generation to optimize the stability of the generation and the material resistivity optimization. The functional simulation of this proposed integration shows it to be the most energy efficient with an energy consumption of 280 fJ per single bit-cell write operation

IV. Conclusion

In this paper, several innovative circuit designs were analyzed to reduce the energy consumption in memory write operations. The designs were contrasted by implementing a code in MARS assembly and comparing the overall energy consumption for designs [1-4]. The energy consumption for a single bit-cell write operation in the designs [1-4] varied slightly with design [3] being the lowest and most-efficient. This design discussed the implementation of circuitry design based on the non-volatile memory device Racetrack memory (RM), where this implementation resulted in a high density and fast speed RM.

The learning coverage in this paper includes:

1. Spin Hall Effect (SHE) in the implementation of the designs to optimize memory-access operations.

2. nMOS and pMOS transistors effect in the symmetry – switching currents in the MJTs.

3. Bit-line and Source-line scheme to optimize the time of the information written to/from memory cell.

4. Spin-Transfer Torque (STT) effect in MRAMs energy-efficient designs

5. Models using TCCT-based memory cells to optimize memory-access operations.

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