Comparing Post-CMOS Sense Amplifiers to Determine Design with Lowest Energy Consumption

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***Abstract*— Explore the designs of four different Sense Amplifiers in an effort to determine the most efficient design for memory read. With the increased scaling that has occurred in technology SA's are crucial to assisting with making Spin-Transfer Torque Magnetic Random Access Memories (STT-MRAM) more reliable. The SA's are compared to a test bench created by writing a program in MARS 4.5 and using that to calculate the energy consumption for each of the different designs. The test bench determines the number of times a word appears in a sentence hard coded to the memory and displays the output to the user. EASA had the best energy consumption of the SA's studied with 74695.42fJ consumed.**

Keywords—Sense Amplifier, MTJ, Memory Read, EASA, VISA, PWSA, BVSC, energy leakage, Sense Margin, STT-MRAM

I. Program Design

A program was designed with the function of finding the number of times a word input by the user is found in a hardcoded sentence. The code begins with the ".data" section which contains the hardcoded sentence at the label "S:", space allocated for the word inputted by the user at label "W:" and the string prompting user input at the label "prompt:". Following this is the ".text" section which holds the body of the code. The code begins by displaying the prompt to receive user input. Next, the address of the sentence is loaded. The address of the word is loaded as well as specification for the maximum number of characters to read. The code continues with three cases to check to see if the word entered by the user is a match within the sentence. The first case is at the label "NoMatch" which begins with loading the bytes of both the "S" and "W". The branch statement checks for the null character which will branch to the end of the code if the end of the sentence has been reached. The registers "$t3" and "$t4" are initialized at zero, then the branch statements check different cases to see if the character matches and if a character match has been met, the code branches to the label "yes". If the branch statement does not branch it will add one to address of the sample string. The loop "yes" has a similar method of checking to see if a character is a match, the only difference is the branch statement that branches if it is equal to a newline, ascii value for newline is 10, meaning that the word input by the user is a word found in the sentence. The label "reset" allows for the word inputted by the user to be set back to the beginning to be used again within the program. The label "Match" increments the counter that is displayed as the output

Fig.1: Flowchart of the assembly program

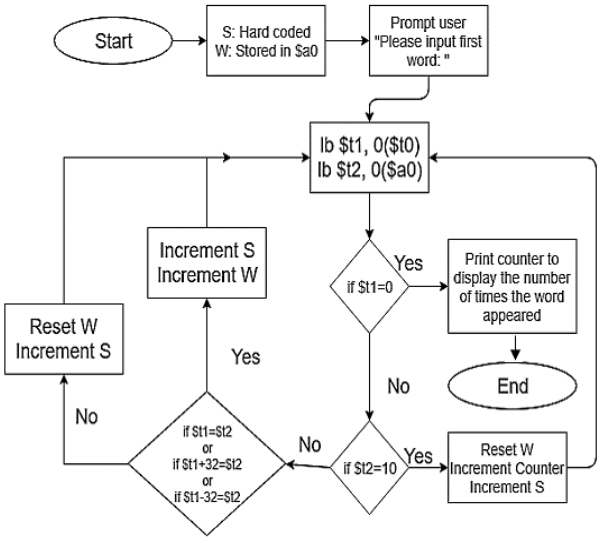

Fig.2: Sample outputs of assembly program

Test 1: Lowercase

```
Please input first word: knight
knight
6
-- program is finished running --
```

Test 2: Uppercase

```
Please input first word: TO
TO
2
-- program is finished running --
```

Test 3: Combination of uppercase and lowercase

```
Please input first word: Ucf
Ucf
3
-- program is finished running --
```

of the program. Label "end" prints the word inputted by the user, displays the number of times the word appears in the hardcoded sentence, and exits the program properly.

Three different test cases were implemented to ensure that the program runs correctly. The first case is using a word that is all lowercase. In this case the word chosen was "knight" and the output of six agrees with the number of times it appears in the sample sentence. The next case is an all uppercase, using the word "TO" which appears twice. The third case is a combination of uppercase and lowercase testing the input "Ucf" which appeared three times.

II. Memory Bit-Cells

Using the code described above four different designs available for memory read operation will be analyzed. Table I lists the energy consumption for the memory read operation of each design. In Table II the total energy consumption of the written assembly code is calculated for each of the designs. Before explaining the four designs analyzed, it is crucial to understand a sense amplifier (SA). When data is read from the memory, the part of read circuitry that is used is known as a SA. A SA works by sensing low power signals from the bitline value that represents data stored within a memory cell. This signal is then amplified so the data within the cell can be interpreted properly by logic outside the memory. SA's allow for an increased reliability in Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) as it is affected by the shrinkage as technology advances [1].

The first design that is mentioned is the Energy Aware Sense Amplifier (EASA) which makes use of Transmission Gates (TGs) that selectively block or pass a signal to reduce the leakage energy and Process Variation (PV) [1]. Leakage energy causes the consumption of power within the circuit. PV is the predictable variance in output performance that is more pronounced at smaller process nodes, these nodes are referenced on the International Technology Roadmap for Semiconductors (ITRS). A disadvantage to this design is the possibility of read errors due to the additional TGs that are placed in the path of Magnetic Tunnel Junction (MTJ) devices cause an added resistance, which in turn affects the (sense margin) SM and PV [1]. A MTJ is two ferromagnets that are separated by a thin insulator that acts as the tunnel barrier that allows for the passage of electrons from one ferromagnet to the other [5].

The second design considered is the Variation Immune Sense Amplifier (VISA). When design is considered, a big difference between the VISA and the EASA is the inclusion of inverters in the design of the VISA. PV effects on the inverters is reduced by the use and placement of the TGs and a reduction of leakage energy is seen in the path of the MTJ devices [1]. Placing the MTJs in parallel allows for the resistances to become the average of the upper and lower values, allowing for an increase in SM [1]. The values of the equation referenced in [1] are referring to MTJ_P and MTJ_{AP} as the resistance for parallel and antiparallel magnetizations arrangement within the two ferromagnets [5]. The design for the EASA and VISA were introduced to improve PV of existing SA's such as the Pre-charged SA (PCSA) and Separated Pre-Charge SA (SPCSA). [1]

The next design to be considered is the preread and write sense amplifier (PWSA). The PWSA combines both read and write into one circuit. This circuit is capable of faster read and write operations which in turn decreases the bit error rate [2], the number of bit errors per unit that occur in the transmission of data. Due to the configuration of the circuit, consisting of two read steps, one write step, and a pass/fail check step, the SM is twice as high [2].

Finally, the Body-Voltage Sensing Circuit (BVSC) is examined and compared with the previous three designs. The main goal of the BVSC is to maximize the SM [3]. In this circuit the focus is on the resistance load when trying maximize the SM. It is important to note that if the resistance load is increased past a certain point, then the SM will begin to deteriorate [3]. When having a large load resistance, the sensing speed becomes limited. Finding the proper balance in a high or low load resistance is key to allowing the sensing to remain at a useful level. Limiting the power usage should be considered with the construction of the circuit as a large read margin (RM) effects this.

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [1-3].

Design	Energy Consumption For Each Bit-cell's Read Operation
EASA [1]	0.23 fJ
VISA [1]	1.86 fJ
PWSA [2]	36.0 fJ
BVSC [3]	195.5 fJ

III. Results and Discussion

The energy consumption is calculated by using the values found by running the "Instruction Statistics" located under tools in MARS4.5 when the program design is ran for the input 'knight'. The dynamic instruction count for the program analyzed is 7451 instructions. The written program has 3150 ALU instructions each ALU instruction requires 1fJ of energy for a total of 3150 fJ. For Jump there is 596 instructions consuming 2fJ of energy for a total of 1192 fJ. Branch has a total of 2445 instruction with 3fJ of energy consumed resulting in 7335 fJ. Other requires 6 instructions each consuming 5fJ of energy for a total of 30fJ. The memory energy for each design type is calculated using the equation Memory = Read Energy + 50 fJ (Write Energy), the values for read energy are located in Table I. Memory had a total of 1254 instructions, once the memory energy for each of the designs is calculated the total energy is found and stored in Table II.

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
EASA [1]	74695.42 fJ
VISA [1]	76739.44 fJ
PWSA [2]	119551.00 fJ
BVSC [3]	319564.00 fJ

When considering the energy consumption for each of the designs, power is inherently interrelated. Power, energy over a certain time interval, is mentioned throughout the sources when explaining the designs. Total power is calculated using dynamic power and static power shown in the following equation: $P_{Total} = P_{\text{Dynamic}} + P_{\text{Static}}$ [4]. Static power is pertinent to consider in the devices studied as it is the result of the leakage current while the transistor is off and the reduction of leakage energy was considered with the SA's. The static power is composed of the product of the supply voltage and the device leakage current.

A main concern when selecting one design as opposed to another is the energy consumption. The lowest energy value is the one that is preferred. Based on the calculated values in Table II, the design that has the lowest energy consumption is the EASA. Reliability and sense margin were also taken into consideration when comparing the different SA's as there is different tradeoffs to acknowledge for each type. EASA is the preferred SA for the given task as it has a reduced power consumption but has an effect on SM and PV.

Another point of consideration for these designs is nondestructive versus destructive sensing schemes which plays a part in reliability and sense margin, upon which these SA's are being compared. The following SA's are considered destructive sensing schemes: SPCSA, PCSA, and BVSC [6]. A destructive scheme is more susceptible to read reliability issues. These read reliability issues are seen in the EASA which may have a higher susceptibility to read errors. PWSA falls under the category of non-destructive sensing schemes [6]. Non-destructive schemes focus on lower energy consumption as opposed to maintaining sensing margins [6].

IV. Conclusion

A program is designed as a testbench to compare various SA's based on energy consumption, while taking other factors into consideration. When determining whether a SA design was effective, reliability, SM, and PV were examined closely. PV is important to keep within the specifications of the circuit at hand because it can lead to a decrease in the expected output. Reliability is taken into consideration because there are several factors that could lead to the failure of a device. MTJ's play a part in allowing for these SA's to have an increased reliability. MTJ's are a useful post-CMOS technology to make use of when configuring the design of the SA's. STT-MRAM makes use of SA's to solve some of the reliability issues associated with this type of memory [1][2][3]. EASA is the best design based on having the lowest energy consumption of 74695.42 fJ compared to the other SA's. This shows that EASA would be the most useful SA for memory read using the program above as the reference point.

References

[1] S. Salehi and R. F. DeMara, "Process variation immune and energy aware sense amplifiers for resistive non-volatile memories," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, 2017, pp. 1-4.

[2] H. Lee *et al*., "Design of a Fast and Low-Power Sense Amplifier and Writing Circuit for High-Speed MRAM," in *IEEE Transactions on Magnetics*, vol. 51, no. 5, pp. 1-7, May 2015.

[3] F. Ren, H. Park, R. Dorrance, Y. Toriyama, C. K. K. Yang and D. Marković, "A body-voltage-sensing-based short pulse reading circuit for spin-torque transfer RAMs (STT-RAMs)," Thirteenth International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, 2012, pp. 275-282.

[4] S. Salehi and R. F. DeMara, "Energy and area analysis of a floating-point unit in 15nm CMOS process technology," *SoutheastCon 2015*, Fort Lauderdale, FL, 2015, pp. 1-5

[5] S. Ikeda *et al*., "Magnetic Tunnel Junctions for Spintronic Memories and Beyond," in *IEEE Transactions on Electron Devices*, vol. 54, no. 5, pp. 991-1002, May 2007.

[6] Soheil Salehi, Deliang Fan, and Ronald F. DeMara. 2016. Survey of STT-MRAM cell design strategies: Taxonomy and sense amplifier tradeoffs for resiliency. J. Emerg. Technol. Comput. Syst. 13, 3, Article 48 (April 2017), 16 pages.