Designs for Energy Consumption Optimization under a Non-Volatile condition

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***Abstract*—** The demand for new technologies that improve time optimization for mass production and energy consumption for non-volatile programmable circuits is a real competitive war in the market. Emerging technology that improve the design for semiconductors is needed. One of the different approaches is the (MTJ) magnetic tunnel junction embedded in CMOS (Complementary Metal Oxide Semiconductor) radiation tolerance. A different approach for the Optimization of Energy consumption is (STT-MRAM) Spin transfer torque magnetic random access memory which has been a promising alternative because of their applications that generate energy consumption, latency and endurance. Another approach for reliability is the introduction of the TMR (Triple Modular Redundancy) structure as a stable model of reliability which is effective fault tolerant to resist (SEU) the single event upset.

Keywords*—MTJ, CMOS, STT-MRAM, non-volatile, TMR, SEU.*

I. Introduction

The code used for this report is in MIPS assemble language under Mars4_5 Jar application. The program functionality is to search for two random words in a preselected statement included inside the code, the output will provide the number of occurrences of these two inputs in the statement. Also, it prints out the indexes of the searched words on the statement.

This program is not case sensitive so the two inputs provided by the user can actually mix upper-letter and lower-letter. Another characteristic is that the input character has a length limit per word of 10 characters' maximum. The way that program achieves the matching for the occurrences is by converting the searched word and the word from the original statement in lower-case letter in order to match and to count the occurrences. Then, it will search the index position and storage them in array to be printed out after the number of occurrences in the output of each word searched.

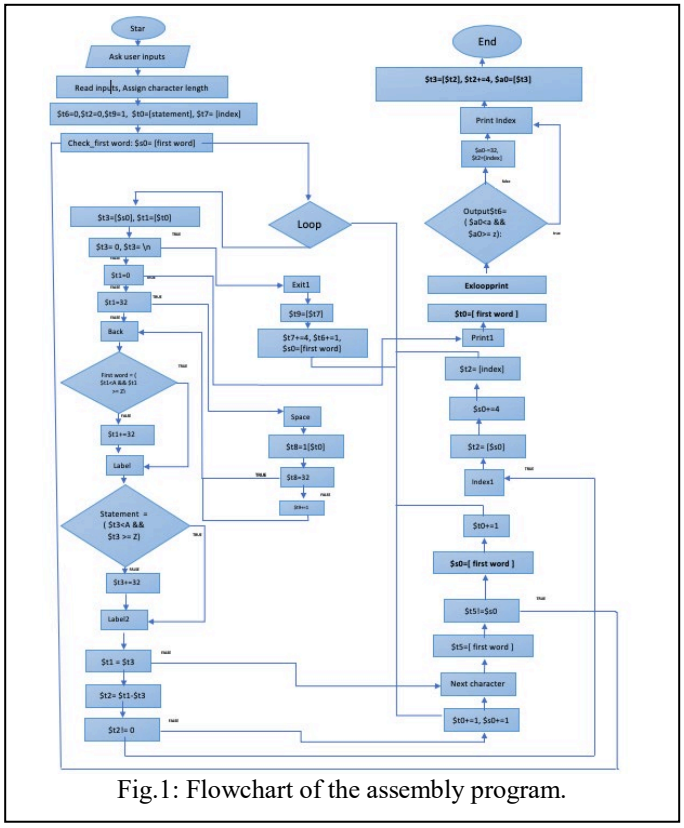

Fig.1: Flowchart of the assembly program.

A. Project Design

The design first read both inputs from the user, after the initialization of the main registers, the program looping the input and compare to a couple of fundamental conditional branches in order to find a match between the searched word versus the statement. The way the program matches the words is taking the searched characters and converted them to a lower-case word by adding 32 to its ASCII code. Then, it repeats the process for the matching word on the statement inside the code. If both words converted are not equal the counter will read the next character. The program detects a space which determines the beginning and the end of each word. Once the program match both words the index register is now subtracted from the main string source. This arithmetic

function finds the index positions. Then, the counters are incremented for the searched characters and the index. These index position are storage on an array to be printer out later. Every block of code jumps to the main loop to repeat the process. The whole process will repeat for the second input entered by the user.

B. Test Cases

Test one: input 1 is kNight and the second input is ucf. The words were chosen to prove the functionality of the code in comparasion with the sample output provided by the Computer Organization Tutor assistant.

Test 2: input 1 degREE, this word was chosen because it has a punctuation mark at the end of the word and input 2 is Know, this input was chosen because in a compose word on the statement presented as well-know.

Test 3 inputs were Pay and input 2 is grant words were chosen randomly.

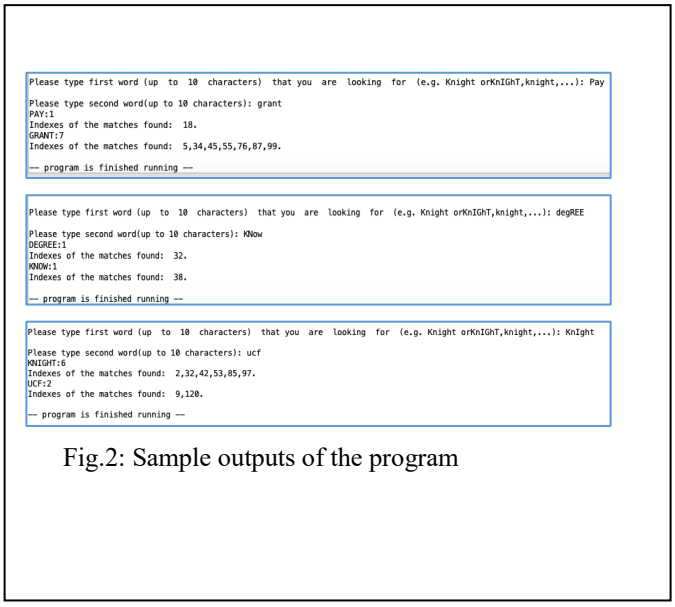

Fig.2: Sample outputs of the program

II. RELAVILITY OF THE NEW DESIGNS FOR ENERGY COMSUMPTION OPTIMIZATION

The Triple Modular Redundancy (TMR) is the fault-tolerant form of N-modular redundancy. One of its structures is the three logic circuits that compute a three outputs in a close-loop. If any of these three systems fails for any reason the 2 left systems with mask the fault. TMR redundancy technology can resist SEU which can change latches in a logic circuit and may modify the data stored on RAM. TMR structure also can be an open-loop SISO (single input and single output) this design works through the implementation of internal RAM and hamming code correction which avoid single event transient which could change the next state trigger due to a single ionizing particle.

Another method of this structure is the Synchronous-Feedback based triple modular redundancy which reset the input signal in case of a fault by SEU in one of the tree systems. The synchronization between the systems reset the signal and reestablish communication allowing to come back to the starting point of the task. This last design is more efficient to save hardware resources. A critical data path is required otherwise the fault cannot be recover by vote and the communication between the systems can be lost. If the 2 modules fail then all the system fail and the corrupted output from the two failed system could overwrite or corrupt the output from the third module. In general, the three latches with one voter will return most of the results correctly even if a fail is detected in one of them.

The bigger challenge for the emerging technologies it to extended the Moore's Law projections. According to "Reliability-Enhanced Separated Pre-Charge Sensing Amplifier for Hybrid CMOS/MTJ Logic Circuits" journal one possibility for achieve lower power, high speed, endurance, scalability is the addition in the hybrid CMOS/MTJ of a separated pre-charge sensing amplifier (RESPCSA) which results will improve the dynamic resistance difference on the MTJ discharge phase by adding two data paths and two transistors between its discharge and evaluation terminal is possible to achieve a larger sensing margins, variation tolerance and low sensing power. Other aspect that can improve MTJ/CMOS can be the adiabatic design which uses AND/NAND, XOR/XNOR and 1-bit Full Adder this method proposes to reduce the power consumption seven times mores than the traditional MTJ/CMOS full adder.

STT-MRAM technology promises innovation for future designs. Its methodology is to switch the electromagnetic course of the MTJ. This change of magnetization is pernicious for real applications but it may be achievable without the use of magnetic field to change the magnetization orientation. So voltage controlled magnetic anisotropy (VCMA) is used instead. Some studies mark the dynamic scaling voltage in the context of STT-MARM which results reduce write energy by 30 % by tuning all possible bit cell parameter in to a numerical procedure saving power supply as highlighted on the conference "STT-MRAM write energy minimization via area optimization under dynamic voltage Scaling".

III. Results and Discussion

In order to analyses the MIPS program energy consumption of the program before mention using the below energy consumption per instruction values.

1) *ALU = 1 fJ*
2) *Branch = 3 fJ*
3) *Jump = 2 fJ*
4) *Memory = Refer to Table I*
5) *Other = 5 fJ*

Energy= (Code ALU%*(1fJ)) +(Code Jump%*2fJ) +(Code Branch%*3fJ) +(Code Memory%*memory) +(Code Other%*5fJ).

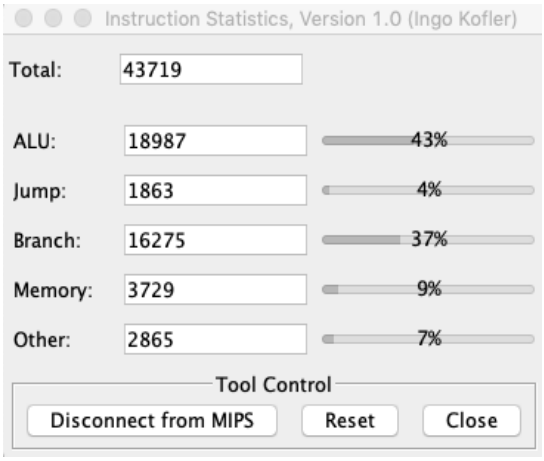

Figure 3 Mips Instructions statistics

The energy consumption for a single bit-cell memory in the design provided in [1-3] on table 1. Values and the dynamic instruction count obtained from Mips tool Instruction Statistics above are used to find the Memory energy consumption.

Table I: Energy consumption for a single bit-cell memory in the designs provided in [1-3].

Design	Energy consumption of a Single Bit-Cell Memory
SEU-Latch [1]	0.88 fJ
DNU-Latch [1]	0.28 fJ
[2]	6.96 fJ
[3]	1.51 fJ

The different data are assigned for the memory energy consumption parameters in which SEU- latch and DNU-latch (Double node upset) "resilient CMOS-based circuit which utilize the interceptive feedback loops with the clock-gating Muller C-element at the output stage to mask soft errors induced by the particles striking the sensitive nodes of the circuit." [5]

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
SEU-Latch [1]	7.93 fJ
DNU-Latch [1]	2.52fJ
[2]	62.64fJ
[3]	13.59 fJ

Total Energy Consumption Single Bit-Cell Memory= 86.68 fJ, so the total energy consumption of the program is 88.65 Fj.

Instructions	ALU (1)	Jump(2)	Branch (3)	Memory (table.1)	Other (5)	Units (fJ)
Energy consumption	0.43	0.08	1.11	86.68	0.35	88.65

IV. Conclusion

There are new designs that can be productive to the energy optimization under Non-volatile conditions. Those mentioned in this report are the improvements in hybrid CMOS/MTJ, TMR redundancy design, and the STT-MRAM technology. The introductions of RESPCSA for hybrid CMOS/MTJ circuits witch in comparation with the traditional CMOS can increases the sensing margins and improve the radiation tolerance. Other improvement for CMOS/MTJ can be the diabetic designs circuits with also targets to the low energy consumption. This report also explains about the benefits of the "STT-MRAM bit-cell optimization technology which improve the performance under dynamic voltage scaling." [4], and finally the TMR redundancy that provides reliability and to save hardware resources.

References

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