Analyzing Energy Efficiency of Memory Bit Cell Designs

Sean Dillon
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816-2362

***Abstract*— This paper aims to estimate the energy consumption of different non-volatile memory designs of memory bit-cells. The designs that are analyzed are MSA-PCSA, MSA-SPCSA, Dynamic Latched Comparator, and STT-MRAM using asynchronous read termination. By using the known energy consumption of the read operation in these designs, the total energy consumption can be calculated by simulating a MIPS assembly program. The program used counts the occurrences of an inputted word from the user in an inputted string also from the user. Using the MIPS software, the dynamic instruction count can be found which is used to find the total energy consumption of each of the designs. The results show that the MSA-PCSA design has the lowest overall energy consumption.**

Keywords— non-volatile memory, memory bit-cell, Merged Sense Amplifier, STT-MRAM, Dynamic Latched Comparator, PCSA, SPCSA,, Self Organized Sub-banks

I. INTRODUCTION

A. Project Design

The code starts by taking the input string and input word that is trying to be found by the user. The input word can only be 10 characters long. The code has 3 loops that are used to where the inputted word appears in the inputted string. The first loop is named the main loop. This loop is used to move through each character of the input string. The main loop also resets the word loop which is needed whenever the characters of the string and word do not match. Once this loop is complete it moves to the word loop which moves through the characters of the input word. This loop has a branch that adds 1 to a counter when the character of the word equals null. The third loop is the next character loop which moves to the next character in both the string and the word without resetting the word string. This loop is used when the characters of both string and word are the same. To make this program work for both upper- and lower-case letters there would need to be additional loops to convert either the word or string to the upper case and lowercase values by adding or subtracting 32 to the ASCII value of each character. To name the index where each word is found there would need to be a counter that counts the amount of spaces in the string and saves the space number when a word is found.

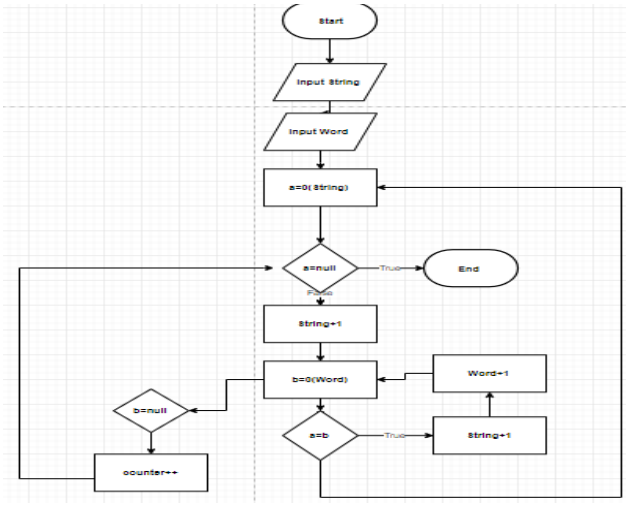

Fig.1: Flowchart of Assembly Program

B. Test Cases

There are 3 test cases that are used to test the program. Each of the test cases will use differing lengths for the input string, long, medium and short. The first test case is the long test where word to be found is UCF and the input string is “UCF, its athletic program, and the university's alumni and sports fans are sometimes jointly referred to as the UCF Nation, and are represented by the mascot Knightro. The Knight was chosen as the university mascot in 1970 by student election. The Knights of Pegasus was a submission put forth by students, staff, and faculty, who wished to replace UCF's original mascot, the Citronaut, which was a mix between an orange and an astronaut. The Knights were also chosen over Vincent the Vulture, which was a popular unofficial mascot among students at the time. In 1994, Knightro debuted as the Knights official athletic mascot.”. This should give an ouput of 3. The second case is the medium case where the input word is bee and the input string is “According to all known laws of aviation, there is no way a bee should be able to fly. Its wings are too small to get its fat little body off the ground.” This should give an output of 1. The last case is the short case where the input word is UCF and the input string is “UCF is good at football”. This should give an output of 1. The outputs of these test cases are shown in figure 2.

II. Memory Bit-Cells

The design of the Memory-Bit Cell for the read operation in [1] using a Self Organized Sub-banks (SOS) design. This design uses Merged Sense Amplifiers (MSA) within the design to function. This design uses two Sense Amplifiers (SA) that are assigned to sub banks. There are two kinds of SAs needed for this one that is energy efficient and one that is high in resilience. The energy efficient SA that is used is a PCSA and the high resilient SA that is used is a SPCSA. The MSA uses both the PCSA and the SPCSA as outputs which improves energy consumption. The SOS design uses the MSA by sending different signals depending on the SEN signal from the SAs. Four inverters in a row are used in this design to drive the bit-line and the word-line.

Most of the memory bit cell designs found in each of the documents rely on non-volatile memory to lower energy consumption. For example in [3] the design uses nonvolatile memory in STT-MRAM which is Spin Transfer Torque Magnetic Random Access Memory. This type of Random Access Memory is useful due to CMOS compatibility, resistivity to errors from radiation, and sharing some of the advantages that DRAM and SRAM have. One problem with this nonvolatile memory is that it needs a large current to run which gives it a high energy consumption. To reduce this high energy consumption this document attempts a design where the read and write signals are done asynchronously so that power is only consumed when it is actively operating. The design of the Memory-Bit Cell in [2] used a new dynamic latched comparator which is supposed to have fast speed and low power consumption. This design showed improvement over the old comparator design with a higher gain.

III. Results and Discussion

Using the first test case mentioned in the introduction, where the input statement is the longest and the input word is UCF, the energy consumption of the program is calculated. This is done by using the instruction tools in MIPS to measure the amount of ALU, Branch, Jump, Memory and other instructions are used during assembly. Each ALU instruction uses 1 fJ, each branch instruction uses 3fJ, each jump instruction uses 2 fj each memory instruction uses read energy which can be found in Table I for each design used plus the write energy which is assumed to be 50 fJ, and each other instruction uses 5 fJ.

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
MSA-PCSA [1]	87.3523 pJ
MSA-SPCSA [1]	88.5003 pJ
[2]	140.806 pJ
[3]	87.5819 pJ

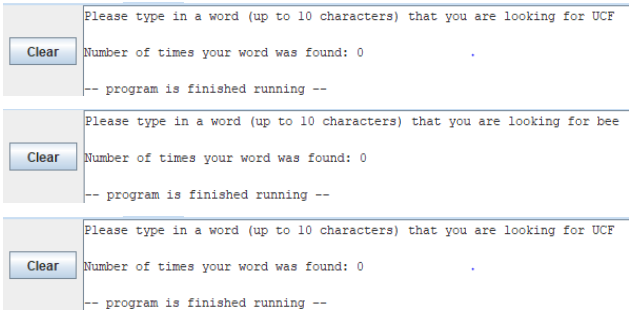

Fig.2: Sample outputs of assembly program.

The results showed that the MSA-PCSA bit-cell from [1] had the lowest energy consumption of all the designs, while the design from [2] using the dynamic latched comparator was the least energy efficient using almost double the energy of all the other designs. It makes sense that this design would have the highest energy consumption since it had the highest energy consumption for each bit cell's read operation as shown in Table I. All the other designs had very similar total energy consumptions with only a difference of about 1 pJ between them. The results of the energy consumption for each design can be found in Table II.

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [1-3].

Design	Energy Consumption For Each Bit-cell's Read Operation
MSA-PCSA [1]	0.35 fJ
MSA-SPCSA [1]	1.15 fJ
[2]	37.6 fJ
[3]	0.51 fJ

IV. Conclusion

In conclusion, nonvolatile memory is a useful tool to reduce overall energy consumption in memory bit cell design. The design using the MSA PCSA from [1] was the most energy efficient design and is the best of the four designs analyzed. This is mostly because it had the lowest energy consumption from the each read operation. The worst design was the dynamic latched comparator method from [2]. While this method may have been an improvement from using a regular comparator, it does not compare well to the other designs using non-volatile memory. This design had the highest energy consumption from the read operation, which most likely is due to the lack of non-volatile memory being used in the design. Some technical topics learned from this project include, understanding of arrays in MIPS, knowledge of memory read energy consumption, how to reduce

energy consumption using non-volatile memory, understanding of different techniques used in improving memory-bit cells, understanding of the use of Sense Amplifiers in Self Organized Sub-banks.

REFERENCES

[1] S. Salehi, N. Khoshavi, R. Zand, and R. F. DeMara, "Self-Organized Sub-bank SHE-MRAM-based LLC: an Energy-Efficient and Variation-Immune Read and Write Architecture," Integration, The VLSI Journal, accepted and in-press.

[2] HeungJun Jeon and Yong-Bin Kim. 2010. A low-offset high-speed double-tail dual-rail dynamic latched comparator. In Proceedings of the 20th symposium on Great lakes symposium on VLSI (GLSVLSI '10). ACM, New York, NY, USA, 45-48.

[3] R. Bishnoi, F. Oboril, M. Ebrahimi and M. B. Tahoori, "Self-Timed Read and Write Operations in STT-MRAM," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 5, pp. 1783-1793, May 2016.

[4] Huai, Yiming. "Spin-transfer torque MRAM (STT-MRAM): Challenges and prospects." *AAPPS bulletin* 18.6 (2008): 33-40.

[5] Eitan, Boaz, et al. "NROM: A novel localized trapping, 2-bit nonvolatile memory cell." *IEEE Electron Device Letters* 21.11 (2000): 543-545

[6] Zhao, Weisheng, et al. "Spin transfer torque (STT)-MRAM--based runtime reconfiguration FPGA circuit." *ACM Transactions on Embedded Computing Systems (TECS)* 9.2 (2009): 14.