Single Bit-Cell Memory design impact on Case Insensitive Word Instances and Index Counter Energy Consumption

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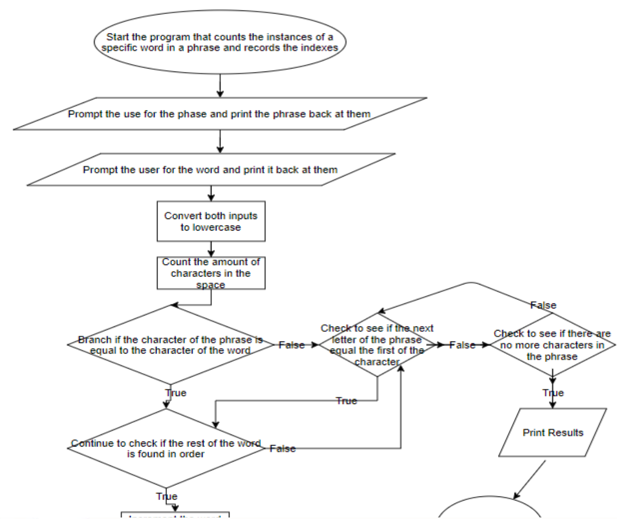
***Abstract*—**The objective of this paper is to observe the impact of different designs aimed at increasing reliability and their impact on energy consumption. The program accepted input for a phrase wanting to be searched and a word wanting to be searched for by the user with disregard for case. The program would output the location of the word being searched for along with the instances of the word in the sentence. Because there were many parts of this program that had to be stored and then changed the dynamic instruction count for memory was relatively high. Considering that much of the sacrifice for creating hardware that is more reliable is that it uses more energy, the total energy used for this program depending on the different single-bit memory design cases allows them to be compared. Throughout this research it was observed that the DNU- latch was the most efficient in terms of energy consumption for dynamic memory instructions.

Keywords—single bit-cell memory; triple modular redundancy, NRAM; DNU latch; SEU latch; double node SEU tolerant latch; MRAM;SRAM; energy consumption

I. INTRODUCTION

A. Project Design

This program receives input from the user. The input is a phrase or paragraph that the user wants to search. The user is then prompted to enter the word they wish to locate. The program then converts both the phrase and the word to lowercase so that it is not case sensitive. The program counts the length of the word. It then tests if the first letter of the phrase is the same as the word. If it is not the same, it increments the phrase without incrementing the word. If it is the same it goes on to increment both the phrase and the word and check until the counter is either the length of the word, the phrase is finished, or the characters of the phrase and the word are no longer the same. If the counter goes up to the length of the word than the instance counter of the word is incremented by one and the space that the word was counted at is recorded. If the characters of the phrase and the word are no longer the same, then the word is reset, and the first character of the word is then compared to the current character of the phrase. If the phrase no longer has any more characters than the program ends, and the indexes and instances of the word are printed.




```
# Please type in your input statement:Will this one work?
Will this one work?
# Please type in a word(up  to  10  characters) that you are looking for (e.g. Knight orKnIGhT,knight,...):am
am
# Indexes of the matches found:
# Number of times the word was found in the input statement:0
-- program is finished running --
```

```
# Please type in your input statement:CaN YoU ReAd UPPer aND LowerCaSWE?
CaN YoU ReAd UPPer aND LowerCaSWE?
# Please type in a word(up  to  10  characters) that you are looking for (e.g. Knight orKnIGhT,knight,...):A
A
# Indexes of the matches found:1,3,5,6,
# Number of times the word was found in the input statement:4
-- program is finished running --

# Please type in your input statement:UCF, its athletic program, and the university's alumni and sports fans are sometis
UCF, its athletic program, and the university's alumni and sports fans are sometimes jointly referred to as the UCF Nati
# Please type in a word(up  to  10  characters) that you are looking for (e.g. Knight orKnIGhT,knight,...):KnIGhT
KnIGhT
# Indexes of the matches found:27,29,42,75,96,100,
# Number of times the word was found in the input statement:6
-- program is finished running --
```

B. Test Cases

The first test input was the phrase "Will this one work?" The word that was being searched for was "am". The reason this sentence was chosen was to make sure the output was zero if a word was not contained in the phrase. The second test input was the phrase "CaN YoU ReAd UPPer aND LowerCaSWE?". They word being searched for was "A". This input was chosen because it tests whether or not the program is case sensitive. The third test input was the phrase "UCF, its athletic program, and the university's alumni and sports fans are sometimes jointly referred to as the UCF Nation, and are represented by the mascot Knightro. The Knight was chosen as the university mascot in 1970 by student election. The Knights of Pegasus was a submission put forth by students, staff, and faculty, who wished to replace UCF's original mascot, The Citronaut, which was a mix between an orange and an astronaut. The Knights were also chosen over Vincent the Vulture, which was a popular unofficial mascot among students at the time. In 1994, Knightro debuted as the Knights official athletic mascot."The word we were looking for was "KnIGhT". This test case was chosen because it stressed the program's ability to find the index and increment of a long sentence that had both upper- and lower-case inputs.

II. Memory Bit-Cells

Triple modular redundancy is a technique to enhance reliability. It utilizes three different paths for a single outcome so that if one fails two will still be able to carry out the instruction [4]. While this approach is more reliable it does require more energy than a single approach as you are triplicating a single approach. One method that is used to reduce the energy consumption is to only triplicate critical data paths [1]. It is important that the voter for a crucial data path is reliable because the outcome of that one Datapath has a compounding effect through the circuit. In other words, if one voter is wrong in a data path that does not have any reliability techniques, all the outputs following the data path will also be corrupted.

Different latches have been implemented to reduce the delay time and energy consumption in TMR approaches. For examples, SEU latches have allowed for only critical data path to be triplicated meaning there are only delays for critical data path. DNU latches have also been implemented using to multiple SEU latches to further optimization [1]. Issues often occur in SEU latches where multiple nodes are charge. For example, when a voltage is sent to a node it unintentionally triggers sensitives nodes nearby in SRAM [3]. Nano random access memory experiences reliability issues due to defects in the nanolayers. Way to make this more reliable involve finding cluster where failure is likely and then implementing TMR in these areas [2].

Some solution to the obstacles faced in TMR approaches to reliability include changing the thickness of the CMOS in SRAM. This allows the SRAM to accept lower voltages, which uses less energy and is less likely to set of sensitive nearby nodes [5]. DNU latches using SEU latches, which triplicate critical data paths, and DICE latches, which are able to withstand many nodes upset, are energy efficient in terms of energy consumed per dynamic memory instruction [1]. Minimizing bit line voltage in MRAM is also promising in regard to providing reliable nonvolatile memory on a large-scale basis [6].

III. Results and Discussion

Using the third case, which was the most demanding in terms of overall dynamic instruction count, we found the total energy consumption in femto joules. We were able to calculate the total energy values as it was given the ALU instruction required 1 fJ per instructions, Branch 3 fJ, Jump 2fJ, Memory depending on the single bit design, and other instruction required 5 fJ. The total energy in fJ was equal to the 2578 memory instructions multiplied by the energy consumption of different memory design plus 24351 fJ which was the energy of the rest of the instructions. We found the total consumption for four different single bit memory designs described in the reference papers. Looking at the results in Table II it is easy to see that the DNU latch was the least demanding in terms of energy whereas the NRAM was the most demanding.

Table I: Energy consumption for a single bit-cell memory in the designs provided in [1-3].

Design	Energy consumption of a Single Bit-Cell Memory
SEU-Latch [1]	0.88 fJ
DNU-Latch [1]	0.28 fJ
[2]	6.96 fJ
[3]	1.51 fJ

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
SEU-Latch [1]	26619.64 fJ
DNU-Latch [1]	25072.84 fJ
[2]	41597.82 fJ
[3]	28243.78 fJ

IV. Conclusion

It was observed that NRAM required the most energy for dynamic memory instruction, the double node SEU tolerant

latch, followed by SEU latch, and finally the DNU- Latch required the least amount of energy. DNU only required 25072,84 fJ when the energy without memory instruction was calculated to be 24351 fJ. Throughout my research I learned about triple modular redundancy and it application for reliability, SEU latches and how they can reduce energy consumption of traditional TMR techniques, DNU latches and why they are superior in some ways to SEU latches in terms of energy consumptions, NRAM and how its speed sacrifices efficiency, and finally MRAM which is more energy efficient but almost as speedy as SRAM.

References

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